AN97798

Migrating From I²C EEPROM to Cypress's I²C F-RAM™

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Associated Code Examples: None
Related Application Notes: AN96578, AN87352

AN97798 provides an overview of the advantages of Cypress's I2C F-RAM™ solution and the differences to be considered when migrating from an I2C EEPROM. It also describes the benefits of the migration.

Contents

1 Introduction

EEPROMs are frequently used for the nonvolatile storage of a system's data. However, the EEPROM's slow nonvolatile write performance and limited write endurance limit its effectiveness in systems that need to execute frequent writes to the nonvolatile memory at bus speed. Many system designs have tried to resolve issues associated with EEPROMs by using a wear-leveling technique to increase the effective endurance, but this has been at the cost of increased EEPROM density and software overhead. Another alternative to save critical system data is to store data in the scratchpad RAM and then transfer it into nonvolatile memory, such as EEPROM or flash, at power down by using a backup power source. Both methods, however, are highly inefficient because of the increase in components, board space, hardware design complexities, and software overhead.

Cypress's I²C F-RAM is a serial nonvolatile memory that employs an advanced ferroelectric process and offers an energy-efficient, high-performance, and high-reliability nonvolatile RAM solution. It is available in both industrial and automotive grade temperatures.

Cypress's F-RAM has fast SRAM cells and provides virtually infinite (10^{14}) read/write endurance cycles, orders of magnitude higher than an EEPROM. The F-RAM performs write operations at the bus speed without incurring any write delays (NoDelay™), unlike serial EEPROMs and flash memories. Data is written directly into the F-RAM array, and the next bus cycle can start immediately, without checking the readiness of the device.

Serial I²C F-RAM devices are available as drop-in replacements for standard I²C EEPROM devices. This application note shows the differences between an industry-standard I²C EEPROM and an I²C F-RAM. These differences need to be considered when migrating from an I²C EEPROM-based solution to Cypress's I²C F-RAM solution.

For more details on I²C F-RAM designs, refer to the application note AN96578 – Designing with I²C F-RAM.

For more details on the benefits of Cypress's F-RAM over a serial EEPROM, refer to the application note AN87352–F-RAM for Smart E-Meters.

2 F-RAM Advantages

2.1 Faster Memory

- Random access: No page reads/writes needed
- Full memory write at bus speed without any internal page program delay after each page write

2.2 Easier Design

- No software overhead for managing page boundary
- Virtually infinite (10^{14}) read/write endurance cycles that do not require wear leveling
- Availability in industry-standard packages

2.3 Data Security

- Reliable, advanced ferroelectric process
- No requirement for a battery or capacitor backup to store the last moment data

2.4 Additional Features

- Energy-efficient, fast nonvolatile RAM
- 151 years of data retention at 65 ºC
- Pb-free technology

3 Migrating from I²C EEPROM to I²C F-RAM

Cypress's I²C F-RAM is available in two industry-standard packages: 8-pin SOIC and 8-pin DFN. These standard and versatile package options make I²C F-RAM drop-in replacements available for the majority of EEPROMs in the same package option and footprint without compromising system performance. In addition, the F-RAM solution provides performance advantages such as higher data throughput, NoDelay write, and energy-efficient operation.

The following sections highlight the key differences and compatibilities between an I²C EEPROM and an I²C F-RAM.

3.1 Pin and Package Compatibility

The ²C F-RAM is pin and package compatible with the I²C EEPROM. Table 1 shows the pin mapping, and Table 2 shows a package comparison of I²C EEPROM and I²C F-RAM.

Table 1. I²C EEPROM and I²C F-RAM Pin Mapping

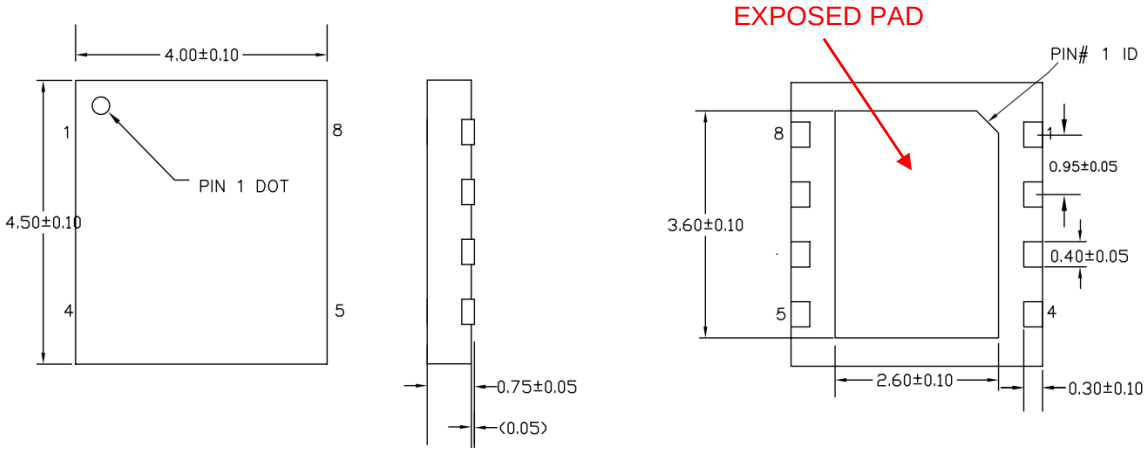
Pin Description	Pin Name	
	I²C EEPROM	I²C F-RAM
Device select address	E2, E1, E0 or A2, A1, A0	A2, A1, A0
Serial data/address input and serial data output	SDA	SDA
Serial clock input	SCL	SCL
Write protect input	WP or $\overline{WC}$	WP
Power supply	V_{DD}/ V_{CC}	V_{DD}
Ground	V_{SS}/GND	V_{SS}

Table 2. I²C EEPROM and I²C F-RAM Package Comparison

Feature/Function	I²C EEPROM	I²C F-RAM	Comments
Package options	8-pin DFN 8-pin SOIC 8-pin PDIP 8-pin TSSOP 8-pin UDFN 8-WLCSP 8-pin MSOP	8-pin DFN 8-pin SOIC	EEPROMs in the standard 8-pin DFN and 8-pin SOIC packages can be replaced by the I2C F-RAM. Other I2C EEPROM packages are incompatible with the I2C F-RAM and will require changes to the PCB. The EXPOSED PAD of F-RAM in the 8-pin DFN package is an NC (no connect) pad, as shown in Figure 1.

Note: This list shows the total package options available across all densities, but not necessarily all packages that are supported for all densities. Refer to the respective device datasheet to learn more about package differences before the migration.

Figure 1. I²C F-RAM 8-pin DFN (4 mm × 4.5 mm × 0.75 mm) Package Outline



The I²C F-RAM EXPOSED PAD is not connected to the die and hence should be left floating. Ensure that the EXPOSED PAD of the I²C F-RAM DFN package is not soldered on the PCB when migrating to I²C F-RAM. Soldering it will cause the I²C F-RAM die to be exposed to excessive heat, which can result in bit failures and margin loss.

3.2 Parameter Compatibility

Table 3 summarizes the key parameters that need to be evaluated for system-level compatibility when migrating from an I²C EEPROM to an I²C F-RAM.

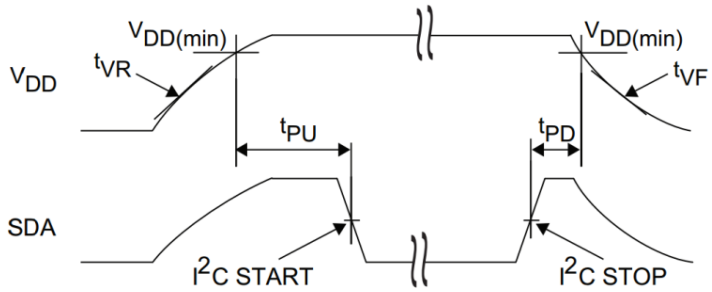
Table 3. Key Parameters Checklist

Parameter	Description	I²C EEPROM	I²C F-RAM	Comments
DC Parameters				
V_{DD}	Power supply voltage	1.5 V to 3.6 V 1.7 V to 5.5 V	2.0 V to 5.5 V	I²C EEPROMs support a wider operating voltage range. When migrating to I²C F-RAM, the system must ensure that the I²C F-RAM operating voltage is within the operating range of the host controller accessing the I²C F-RAM.
V_{IH}	Input HIGH voltage	Varies	0.7 × V_{DD} to V_{DD} + 0.3 V	The I²C F-RAM follows the CMOS logic standard. The system must ensure that the logic levels are within the operating range of both the host and the I²C slave for proper operation.
V_{IL}	Input LOW voltage	Varies	–0.3 V to 0.3 × V_{DD}	
V_{OL}	Output LOW voltage	Varies	Varies 0.6 V (max), I_{OL} = +6 mA 0.4 V (max), I_{OL} = +3 mA 0.4 V (max), I_{OL} = +2 mA 0.2 V (max), I_{OL} = +150 µA	The I²C F-RAM output driver supports standard output drive strength, making it compatible with the majority of host controllers. The system must ensure that the logic levels are within the operating specification of both the I²C master (host) and the I²C F-RAM for proper operation.
AC Parameters				
f_{SCL}	I²C clock frequency	Up to 1 MHz	Up to 3.4 MHz	Both devices follow the NXP specification for I²C access. Therefore, migrating from I²C EEPROM to I²C F-RAM does not require any system update for the same bus speed. A few crypto I²C EEPROM devices can support an I²C bus speed up to 5 MHz. The I²C F-RAM cannot replace these special devices due to incompatible features and access speed.
C_b	Total capacitance of one I²C bus	Varies (rated to NXP standard load or below)	Follows the NXP standard I²C bus load	Migrating to I²C FRAM does not require any change or adjustment to the bus load.

Parameter	Description	I²C EEPROM	I²C F-RAM	Comments
Other I²C AC parameters	All other AC parameters of the device	Compatible with NXP I²C specification	Compatible with NXP I²C specification	Since I²C EEPROM and I²C F-RAM are both compatible with the NXP I²C specification, migration to I²C F-RAM does not require any change. It is always recommended to compare all AC parameters for any differences and evaluate their impact before migrating.
t_W/ t_{WC}/ t_{WR}	Write cycle time (time to write data from page buffer to EEPROM memory)	Varies, 5 ms to 10 ms	Not applicable	With I²C F-RAM, a data byte is written directly into an intrinsic nonvolatile F-RAM cell. Therefore, the write cycle time is not applicable, and the device is immediately ready for the next access.
Power Parameters				
t_{VR}	V_{DD} power-up ramp rate	Varies	30 µs/V 50 µs/V (minimum spec)	When migrating to the I²C F-RAM, the system must ensure that the V_{DD} power ramp rate is within the specification of the I²C F-RAM, as shown in Figure 2. Systems must ensure that the I²C F-RAM V_{DD} power supply ramp rate is slower than the minimum specification. For example, the V_{DD} power supply should not rise or fall 1.0 V in less than 30 µs (for a 30-µs/V ramp rate).
t_{VF}	V_{DD} power-down ramp rate	Varies	30 µs/V 100 µs/V (minimum spec)	
t_{PU}	Power-up V_{DD} (minimum) to first access (START condition)	Not specified	1 ms	I²C F-RAM needs to wait 1 ms to complete its bootup sequence and get ready. All devices have a finite bootup time, but some of them do not specify because their bootup time is not observable in a real system. When migrating from I²C EEPROM to I²C F-RAM, this parameter should be evaluated, and if necessary, the controller firmware should be modified to match the t_{PU} time delay (for the first access only).

Note: Other device parameters such as device current in different operating modes, ESD profile, latch-up current profile, soldering profile, and packages that differ between the I²C EEPROM and I²C F-RAM can warrant some system-level analysis before replacing the I²C EEPROM with the I²C F-RAM.

Figure 2. I²C F-RAM Power Cycle Timing



3.3 Feature and Access Protocol Compatibility

Table 4 compares the I²C EEPROM and the I²C F-RAM protocols and features and discusses key points to be considered when migrating from an I²C EEPROM to I²C F-RAM.

Table 4. I²C EEPROM and I²C F-RAM Protocol and Feature Comparison

Feature	I²C EEPROM	I²C F-RAM	Comments
I²C START	Standard I²C START		No change required when migrating to the I²C F-RAM.
I²C STOP	Standard I²C STOP		
Data input	Device samples SDA on SCL rising edge		
Data output	Changes SDA when SCL is LOW		
Device addressing	7-bit addressing		
Memory addressing	2-byte or 1-byte, depending on the memory density		No change required when migrating to the I²C F-RAM. The most significant address byte is sent first followed by the least significant address byte. In a byte, the most significant address bit is transmitted first.
Single-byte write	Single byte write into page memory, followed by nonvolatile write cycle time. The next access can start only after the write cycle time (t_{WC}).	Byte write into nonvolatile memory at bus speed. The next access can start immediately.	No change required when migrating to the I²C F-RAM. However, the system can take advantage of the I²C F-RAM by reducing the write delay and increasing the bulk write size, which can significantly improve the system's nonvolatile write performance.
Bulk write	The maximum size of the bulk write is limited to the page size, followed by the nonvolatile write cycle time. Continuing to write beyond the page boundary will roll over to the beginning of the page and overwrite previously written data. The next access can start only after the write cycle time (t_{WC}).	The maximum size of the bulk write is the memory array. Continuing to write beyond the array size will roll over the address counter to the beginning of the memory array. The next access can start immediately.	

Feature	I²C EEPROM	I²C F-RAM	Comments
Random address read	A dummy write cycle is performed to load this (random) address into the address register, followed by a read.		No change required when migrating to the I²C F-RAM.
Current address read	Reads from the current address, which is set after executing the write or read access in the previous cycle.		
Sequential read	This can be used after a random or current address read. After the first successful read, the address counter auto-increments to the next address and sends data at the output. This continues until the I²C master sends NACK or generates a STOP condition.		
Write protect pin configuration	Varies. Most devices have an internal weak pull-down resistor to keep this pin low when floating (not connected).	All I²C F-RAM devices have an internal weak pull-down resistor to keep this pin low when floating (not connected).	
Slave select pin (A2, A1, A0) configuration	Varies. Most devices have an internal weak pull-down resistor to keep these pins low when floating (not used).	All I²C F-RAM devices have an internal weak pull-down resistor to keep these pins low when floating (not used).	
Software reset	Some I²C EEPROMs define software reset by implementing one or all of the following protocols: ▪ Generate START condition ▪ Generate nine dummy clocks on SCL ▪ Generate START followed by STOP	I²C F-RAM does not require this feature. However if implemented, it will have no impact on the device operation.	No change required when migrating to the I²C F-RAM. Usually this feature is defined by the NXP I²C specification to bring the device out of a bus hang situation, which can arise when the I²C communication is terminated abruptly.

4 Firmware Compatibility

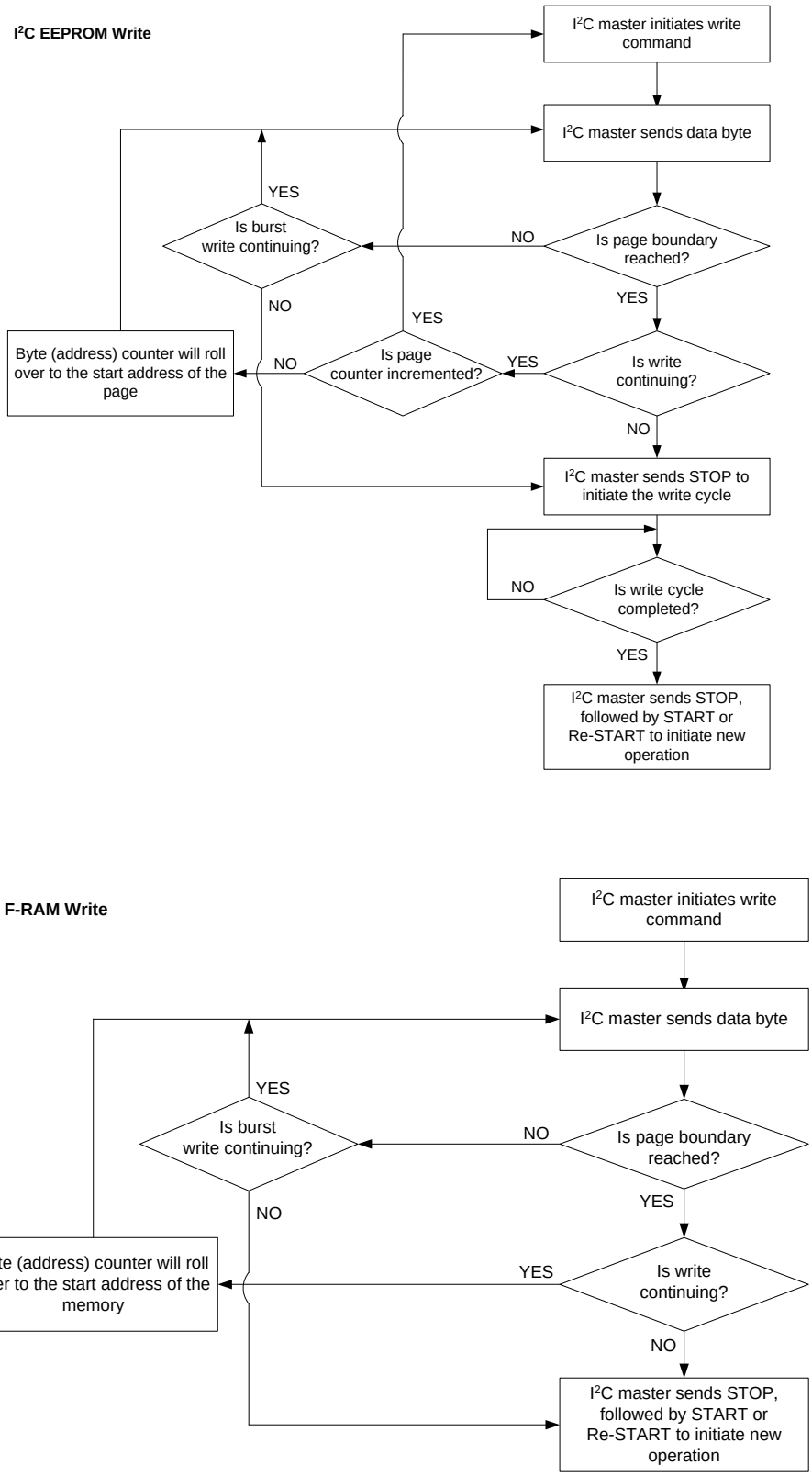
The I²C master firmware for the I²C EEPROM access will work as-is for the I²C F-RAM. This section discusses various operations in the system that can be improved by firmware updates when migrating from I²C EEPROM to the I²C F-RAM solution.

4.1 Multiple Pages in EEPROM versus Single Page in F-RAM

EEPROMs are written or programmed on a page-by-page basis. A typical page size of a 1-Mb EEPROM device is 256 bytes (2 Kb). This means that to write the full EEPROM memory, the host controller needs to initiate 512 page-write operations. It also needs to track the count of the total data bytes written in an individual page to prevent address counter rollover.

F-RAM does not use the page architecture; therefore, the entire memory array can be treated as one page. The entire F-RAM array can be written in the burst mode with a single write command. Once the internal address counter reaches the last F-RAM location, the counter rolls over to the start address, 0h. Because the I²C F-RAM contains a single page, the host controller is required to keep track of only one counter, as opposed to tracking two counters for the page count and the byte count in a page. The I²C F-RAM simplifies firmware design by reducing the number of execution steps. Figure 3 demonstrates writing in I²C EEPROM versus writing in I²C F-RAM.

Figure 3. Write Operation in I²C EEPROM and I²C F-RAM



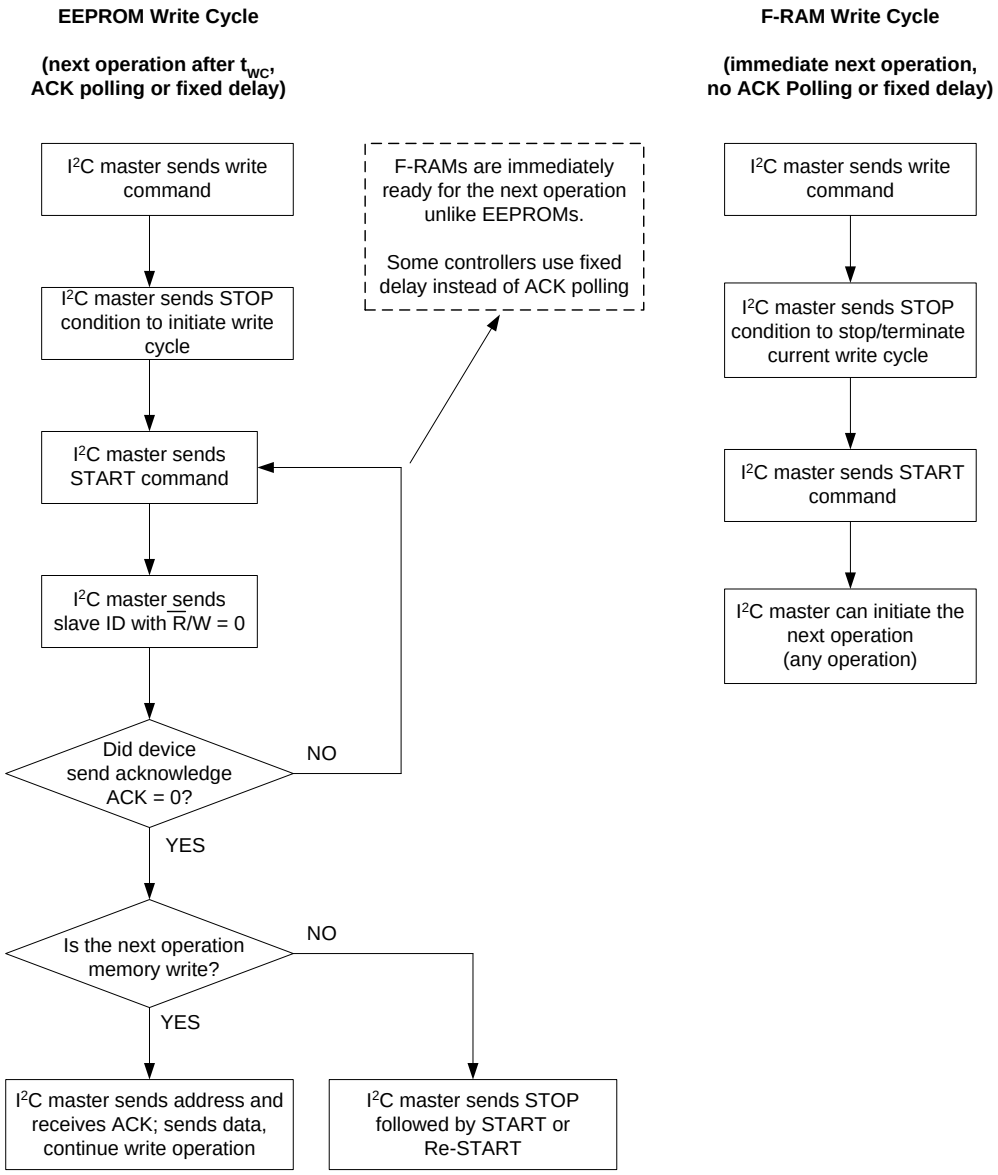
4.2 Page Write Delay

EEPROMs require a page write delay, t_{WC} (typically 5 ms), to transfer buffer data into the nonvolatile EEPROM. EEPROM shows busy and returns NACK during t_{WC} time. Firmware can either wait for a fixed write cycle delay, t_{WC}, or implement acknowledgement (ACK) polling. Figure 4 shows the ACK polling method to complete the EEPROM write cycle.

The EEPROM page size varies between densities or between different vendors' products for the same density. The system firmware must be designed to accommodate the page size variation and the page write delay between different EEPROM parts.

The page write delay is not required in the I²C F-RAM; therefore, the write delay can be eliminated in the firmware to improve the system's nonvolatile write performance.

Figure 4. EEPROM versus F-RAM Write Cycle



5 Benefits of Migrating to I²C F-RAM

This section describes the benefits of migrating from an I²C EEPROM to an I²C F-RAM solution.

5.1 Zero Clock Cycle Write Latency

A typical EEPROM requires a 5-ms write cycle to transfer its page data to a nonvolatile EEPROM cell. This results in a long write time when several kilobytes of data need to be written. In contrast, with F-RAM, all writes occur at the bus speed, with no memory-based latency. The following Example demonstrates the F-RAM nonvolatile write performance improvement over an EEPROM due to zero clock cycle write latency. Figure 5 illustrates the impact of the write latency.

5.1.1 Example

Equation 1 determines the total time to write in I²C EEPROM.

Equation 1 $$T1\ (EEPROM) = \frac{Nx8}{f} x1000 + \frac{N}{PS} x\ Twc$$

Where:

T1 – Total time to write in EEPROM (ms)

N – Number of data bytes to be transferred over I²C bus

f – I²C frequency (Hz)

PS – EEPROM page size

Twc – EEPROM write cycle time (ms)

Equation 2 determines the total time to write in I²C F-RAM.

Equation 2 $$T2\ (F\text{-}RAM) = \frac{Nx8}{f} x1000$$

Where:

T2 – Total time to write in F-RAM (ms)

N – Number of data bytes to be transferred over I²C bus

f – I²C frequency (Hz)

EEPROM Write Time Example

A 1-MHz I²C EEPROM with a 128-KB (1-Mb) density, 256-byte page, and 5-ms page write cycle time (t_{WC}) takes about 28 ms to back up 8 Kb (4 pages) of data:

$$T1\ (EEPROM) = \frac{1024x8}{1000000} x1000 + \frac{1024}{256} x\ 5\ = 28.192\ ms$$

Similarly, it takes 3.608 seconds to back up 128-KB (1-Mb) of data in I²C EEPROM:

$$T1\ (EEPROM) = \frac{128x1024x8}{1000000} x1000\ + \frac{1024x128}{256} x\ 5\ = 3608\ ms\ or\ 3.608\ seconds$$

F-RAM Write Time Example

A 1-MHz I²C F-RAM with a 128-KB (1-Mb) density takes about 8 ms to back up 8 Kb of data:

$$T2\ (F\text{-}RAM) = \frac{1024x8}{1000000} x1000 =\ 8.192\ ms$$

Similarly, it takes 1.049 seconds to back up 128 Kb (1 Mb) of data in I²C F-RAM:

$$T2\ (F\text{-}RAM) = \frac{1024x128x8}{1000000} x1000 = 1049\ ms\ or\ 1.049\ seconds$$

In addition, EEPROM can have varying page sizes for the same density; in this example, considering a lower page size EEPROM will require more page write operations and hence a longer time to complete the write cycle. The result will be additional write delays. Because F-RAM is not paged memory, the time to write a given set of data to it remains the same across all memory density options.

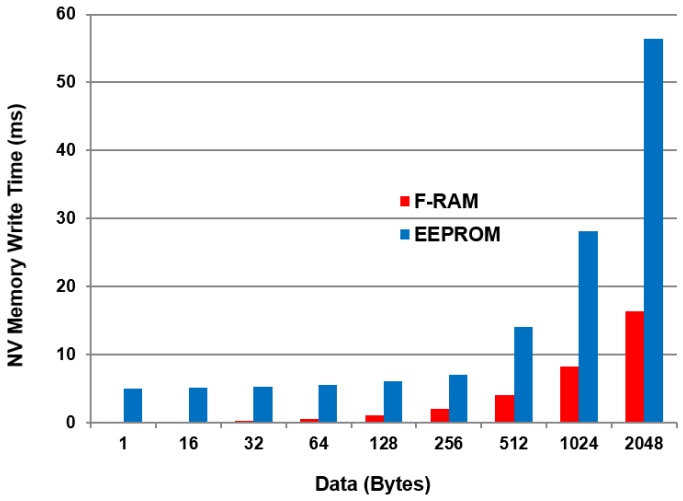
Table 5 and Figure 5 illustrate the time to write to nonvolatile memory in F-RAM and EEPROM.

Table 5. Time to Write to EEPROM and F-RAM using 1-MHz I²C Interface

Data Bytes	Time to Write (ms) to Nonvolatile Memory	
	F-RAM	EEPROM
1	0.008	5.008
16	0.128	5.128
32	0.256	5.256
64	0.512	5.512
128	1.024	6.024
256	2.048	7.048
512	4.096	14.096
1024	8.192	28.192
2048	16.384	56.384

Note: The calculation in Table 5 does not include the overhead for sending the control and address bytes before sending the data bytes to be written. A multipage write operation in the I²C EEPROM requires a new I²C write command to be sent for every page write.

Figure 5. Write Performance in EEPROM versus F-RAM



5.2 Low-Power Design

F-RAM devices consume about one-third of the active current of EEPROM, while the standby/sleep current specifications of F-RAM are almost equal to those of EEPROM. This difference in active current has a huge impact on power consumption, especially when applications such as smart e-meters are write intensive due to frequent data logging. In addition to higher active current, EEPROM incurs an additional page write delay that causes the device to remain in active mode for an extended period, increasing power consumption.

The amount of energy required to write to I²C F-RAM and I²C EEPROM is calculated using the Energy Calculation Example. Table 6 compares the energy consumption of F-RAM and EEPROM, as shown in Figure 6. This comparison demonstrates energy consumption.

5.2.1 Energy Calculation Example

Equation 3 determines the energy consumed by F-RAM and EEPROM during a write cycle:

Equation 3 $E = V \; x \; I \; x \; t$

Where:

V – Operating voltage

I – Active current during write

t – Total time to write data to nonvolatile memory

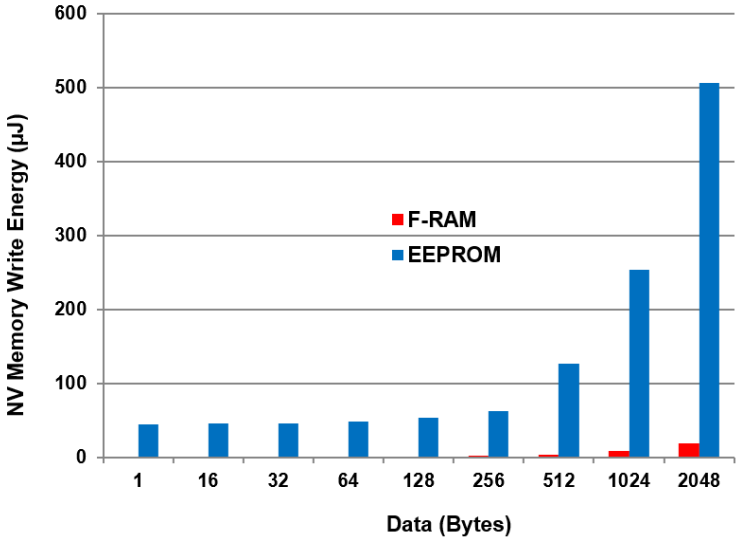
Table 6. Energy to Write to EEPROM and F-RAM

Write Data Bytes	Nonvolatile Memory Write Energy (µJ)	
	F-RAM	EEPROM
1	0.0096	45.072
16	0.1536	46.152
32	0.3072	47.304
64	0.6144	49.608
128	1.2288	54.216
256	2.4576	63.432
512	4.9152	126.864
1024	9.8304	253.728
2048	19.6608	507.456

Notes:

1. A typical 3-V, 1-Mb I²C EEPROM consumes 3 mA of active current during the write operation. Therefore, the amount of energy an I²C EEPROM will require to write 128 bytes (1 Kb) of data is 54.22 µJ (3.0 V x 3 mA x 6.024 ms).
2. A typical 3-V, 1-Mb I²C F-RAM consumes 0.4 mA of active current during the write operation. Therefore, the amount of energy an I²C F-RAM will require to write 128 bytes (1 Kb) of data is 1.23 µJ (3.0 V x 0.4 mA x 1.024 ms).

Figure 6. Energy Consumption during Data Write to EEPROM versus F-RAM



5.3 No Multidevice Design Required

The EEPROM write operation has two stages of data transfer. Data is written to the page buffer, and then a nonvolatile memory write cycle occurs. During the write cycle, EEPROM access is disabled; therefore, the next access cannot start until the ongoing write cycle is complete.

The I^2C F-RAM, on the other hand, writes data at the bus speed. Therefore, it does not require pipeline implementation, simplifying the system firmware architecture and reducing the development cycle time and associated test overhead.

5.4 No Page Size Restriction

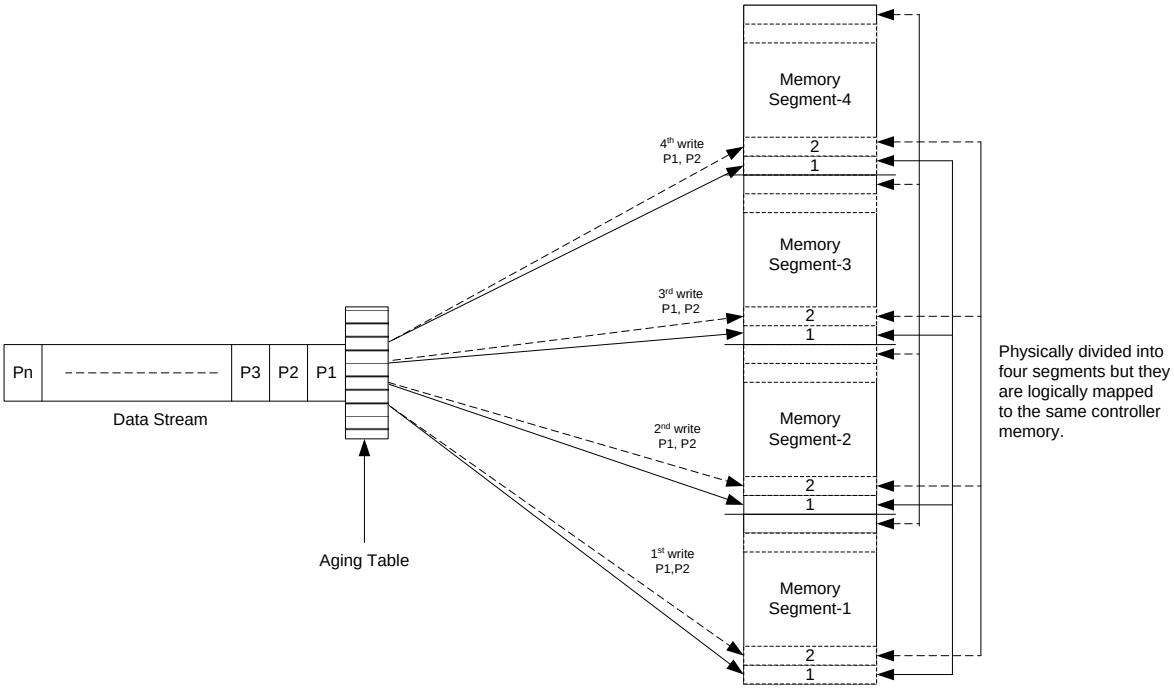
The EEPROM page size can vary by density. So, the firmware program to interface to an EEPROM must be written flexibly and tested over a range of density options to support varying densities for different product versions. F-RAM imposes no page size restriction, enabling you to write arbitrarily sized blocks of data, independent of the total size of memory in use.

5.5 No Wear Leveling or Age Tracking Required

All systems that require frequent write to EEPROM use careful address management. This method, called “wear leveling,” aims to equalize the number of times each page is written.

Wear leveling is used in EEPROM to increase the effective endurance limit. In a wear-leveling implementation, the entire memory array is divided into multiple segments that are mapped to identical addresses of a microcontroller or processor. For example, if a write happens to some address location(s) in the current memory segment, the subsequent write to the same address location(s) will be executed in a different segment. The wear-leveling implementation is illustrated in Figure 7.

Figure 7. Wear-Leveling Mechanism in EEPROM



Wear leveling requires a fairly sophisticated driver routine in the controller, through which all nonvolatile accesses are managed. This routine translates the internal addressing of data structures into a physical addressing scheme for the memory. Usually, an “aging table” on the memory array tracks how the device is being used. This consumes a significant amount of code space in a miniature filing system. During an architectural change, it increases the design cycle time when migrating to a new processor family.

A typical EEPROM device offers an endurance cycle of 10^6, whereas the endurance count for the F-RAM device is 10^{14}, which is orders of magnitude higher (100 million times) than the typical EEPROM endurance cycle. Therefore, to match the F-RAM endurance, a system would require 100 million EEPROM devices or an EEPROM device with 100 million times the F-RAM density, which is virtually impossible.

5.6 No Action Required After Power Failure

Data immediately becomes nonvolatile after it is written to F-RAM. This is one of the key benefits of using an F-RAM device: It increases confidence in system data integrity under extreme fault conditions. All writes happen directly to the nonvolatile memory. Therefore, no power backup or extended power supply is needed to save the data after a power failure.

In contrast, to save valuable data in an EEPROM-based system, the controller must initiate and execute a complete write cycle to the desired data block size when a power fault is detected. The main power supply must store sufficient energy to reliably power the controller and its peripherals throughout this process. The controller must be protected against crashes caused by a rapid transition on the power supply during power failure. The system firmware must be thoroughly tested over a range of error conditions to ensure that the correct action is carried out at whatever system state existed before the power failure.

6 Summary

Migrating from the I^2C EEPROM to Cypress's I^2C F-RAM improves system performance, reliability, and energy-efficiency. The I^2C F-RAM industry-standard pin and package configuration and electrical compatibility simplify the migration. There are a few differences between devices, highlighted in this application note, that need to be considered. However, these differences typically do not preclude migration in most applications.

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