AN96841

Getting Started with EZ-BLE™ Creator Modules

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Associated Project: Yes

Associated Part Family: CYBLE-XXXXXX-XX

Software Version: PSoC® Creator™ 4.1 and higher

Related Application Notes: For a complete list of the application notes, click here.

AN96841 introduces you to Cypress's EZ-BLE Creator family of Bluetooth Smart modules. EZ-BLE modules are fully qualified and certified Bluetooth Low Energy (BLE) solutions. EZ-BLE Modules provide a complete BLE solution, integrating a BLE radio system, two crystals, antenna, and passive components required for BLE operation. This application note helps you explore the EZ-BLE Module architecture and development tools and shows you how to create your first project with an EZ-BLE Module and PSoC Creator, the development tool used for all EZ-BLE Modules. This application note also guides you to more resources to accelerate in-depth learning about the Cypress EZ-BLE solutions.

Contents

1 Introduction

Bluetooth Low Energy (BLE) is an ultra-low-power wireless standard defined by the Bluetooth Special Interest Group (SIG) for low-power, short-range communication. It features a physical layer, protocol stack, and profile architecture, all designed and optimized for the lowest power consumption. BLE operates in the 2.4-GHz ISM band, with a data rate up to 1 Mbps.

BLE is used in a wide range of applications. The use of BLE in these applications also varies widely in production volume, from very low- to high-volume end products. The use of fully qualified, certified, BLE modules removes time-consuming RF board design and costly qualification/certification processes. As such, modules have quickly become the design preference.

The Cypress EZ-BLE Module family provides fully integrated, qualified, and certified programmable systems that integrate 32-kHz and 24-MHz crystal oscillators, passive components, on-board chip or trace antennas, and a Cypress BLE chip, which includes the BLE radio, programmable analog and digital blocks, memory, and an ARM® Cortex®-M0 microcontroller. Cypress EZ-BLE modules offered in footprints as small as 10 mm × 10 mm × 1.8 mm.

EZ-BLE Modules enable quick time-to-market and eliminates time-consuming and costly RF hardware development, certification, and qualification processes, offering an effective alternative to completing a BLE system design from the ground up. In addition to reducing the cycle time and certification and qualification expenses, the programmable architecture and GPIOs allow great flexibility by using the PSoC Creator IDE, the schematic-based design tool for designing applications with EZ-BLE Modules, and a speedy time-to-market.

The BLE stack library is integrated with PSoC Creator and is free-of-cost. It can be easily configured using a simple graphical user interface allowing you to jumpstart your BLE design in minutes.

EZ-BLE Modules offer a best-in-class current consumption of 150 nA while retaining the SRAM contents and the ability to wake up from an interrupt. The EZ-BLE Module consumes only 60 nA while maintaining the wakeup capability in its nonretention power mode. The capacitive touch-sensing feature in the EZ-BLE Module, known as CapSense®, offers an unprecedented signal-to-noise ratio, best-in-class waterproofing, and a wide variety of sensor types such as buttons, sliders, and proximity sensors. These sensors are gaining increased popularity in wearable electronic devices such as activity monitors and health and fitness equipment.

The EZ-BLE PSoC Module products provide the most cost-effective solution for sensor-based Internet of Things (IoT) solutions, allowing maximum integration of external ICs used for sensor interface, thereby reducing the overall BOM cost and size. In addition, programmable analog and digital subsystems allow optimized battery life by offloading tasks traditionally completed by the main MCU.

2 More Information

Cypress provides a wealth of data at www.cypress.com to help you accelerate the learning on the EZ-BLE Modules, as well as Cypress's PSoC family of silicon devices. If you are a first-time user of Cypress's PSoC family of products, it is recommended that you read Appendix A: Cypress Terms of Art for a list of commonly used terms. If you are seeking an overview of the Bluetooth Low Energy (BLE) standard, read AN91267 - Getting Started with PSoC® 4 BLE. The following is an abbreviated list of resources for the EZ-BLE Module family:

- **Datasheets** describe and provide electrical specifications for each of the EZ-BLE Module.
- **3D Models and Drawings** for each EZ-BLE module are located in KBA218122.
- **Application Notes and Code Examples** cover a broad range of topics. Many application notes include code examples. PSoC Creator provides additional code examples – see Appendix D: Code Examples.
- **Technical Reference Manuals (TRMs)** provide detailed descriptions of the architecture and registers for the PRoC BLE and PSoC 4 BLE device families.
- **CapSense Design Guide** describes how to design capacitive touch-sensing applications with the EZ-BLE Modules.
- **Development Tools**
  - PSoC Creator is a state-of-the-art, easy-to-use IDE that offers a unique combination of hardware configuration and software development based on standard schematic entry.
  - CySmart BLE Host Emulation Tool for Windows is an easy-to-use GUI that enables you to test and debug your BLE Peripheral applications. iOS and Android applications are also available.

- **Development Kits**
  - CY8CKIT-042-BLE Bluetooth Low Energy (BLE) Pioneer Kit is an easy-to-use and inexpensive development platform for BLE. This kit includes connectors for Arduino™ compatible shields.
  - CY8CKIT-042-BLE-A Bluetooth Low Energy (BLE) 4.2 Compliant Pioneer Kit enables customers to evaluate and develop Bluetooth 4.2 compliant solutions using the PSoC® 4 BLE and EZ-BLE module products.
  - Each EZ-BLE Module offers a low-cost Evaluation Board to provide an evaluation vehicle for the EZ-BLE Modules without requiring custom hardware design. These Evaluation Boards are compatible with the CY8CKIT-042-BLE and CY8CKIT-042-BLE-A Bluetooth Low Energy (BLE) Pioneer Kits. See Development Kits and Evaluation Boards for an overview of kits for the EZ-BLE Modules.
- **Technical Support**
  - Frequently Asked Questions (FAQs): Learn more about our BLE ecosystem.
  - BLE Forum: See if your question is already answered by fellow developers on the PSoC 4 BLE and PRoC BLE forums.
  - Still have questions? Visit our support page and create a technical support case or contact a local sales representative. If you are in the United States, contact our technical support team by calling our toll-free number: +1-800-541-4736. Select option 8 at the prompt.

3 EZ-BLE Module Overview

If you are looking for a detailed overview of the Bluetooth Low Energy standard or the Cypress BLE Component, see AN91267 - Getting Started with PSoC 4 BLE.

EZ-BLE Modules offer fully integrated and fully certified BLE solutions allowing rapid development and deployment of your BLE product. This section provides an overview of the EZ-BLE Modules available today. For detailed information on each module referenced in this section, see Appendix B: EZ-BLE Module Product Details**.**

All EZ-BLE Modules ship with the components required to achieve full BLE functionality, including:

- PCB substrate: Footprints as small as 10 mm × 10 mm × 0.5 mm
- Cypress BLE IC (PRoC BLE or PSoC 4 BLE)
  - See the PRoC BLE 128-KB Flash device datasheet for detailed information on the Cypress PRoC BLE IC with 128-KB Flash
  - See the PSoC 4 BLE 128-KB Flash device datasheet for detailed information on the Cypress PSoC 4 BLE IC with 128-KB Flash
  - See the PRoC BLE 256-KB Flash BT 4.1 device datasheet for detailed information on the Cypress PRoC BLE IC with 256-KB Flash. For detailed information on Cypress's BT 4.2 compliant silicon devices, download the PRoC BLE BT 4.2 datasheet.
  - See the PSoC 4 BLE 256-KB Flash BT 4.1 device datasheet for detailed information on the Cypress PSoC BLE IC with 256-KB Flash. For detailed information on Cypress's BT 4.2 compliant silicon devices, download the PSoC 4 BLE BT 4.2 datasheet.
- Crystal oscillators
  - 32.768-kHz watch crystal oscillator (WCO)
  - 24.0-MHz external crystal oscillator (ECO)
- Chip or Trace antenna
- External Power Amplifier (PA) and Low-Noise Amplifier (LNA) on select modules
- Passive components (resistor, capacitor, inductor)
- RF Shield, unless otherwise noted

3.1 EZ-BLE Module Family Features

Table 1 summarizes the features and capabilities of every EZ-BLE Module available from Cypress.

Table 1. EZ-BLE Module Features and Capabilities

Features	Details
BLE Subsystem	BLE radio and link-layer hardware blocks with BLE 4.1 or BLE4.2- compatible protocol stack
CPU	3-MHz to 48-MHz ARM Cortex-M0 CPU with single-cycle multiply
Flash Memory	128-KB or 256-KB
SRAM	16-KB or 32-KB
GPIOs	Up to 25 (module-dependent)
CapSense	Up to 25 sensors (module-dependent)
CapSense Gestures	Supported
ADC	12-bit, 1-Msps SAR ADC with sequencer
Opamps	Up to four available on select EZ-BLE Modules
Comparators	One available on select EZ-BLE Modules
Current DACs	One 7-bit, and one 8-bit
Power Supply Range	1.9 V to 5.5 V
Low-Power Modes	Deep-Sleep mode at 1.3 µA Hibernate mode at 150 nA Stop mode at 60 nA
Serial Communication	Two independent serial communication blocks (SCBs) with programmable I^2C, SPI, or UART
I^2S Communication Interface	Yes
Timer/Counter/Pulse-Width Modulator (TCPWM)	4/4/8
Universal Digital Blocks (UDBs)	Four available on select EZ-BLE Modules
Clocks	3-MHz to 48-MHz IMO 32-kHz ILO
Power Supply Monitoring	Power-on reset (POR) Brown-out detection (BOD) Low-voltage detection (LVD)
Integrated Crystal Oscillators	24-MHz ECO integrated on module 32-kHz WCO integrated on module
Antenna Type	Trace or Chip Antenna (module dependent)

3.2 EZ-BLE Module Low Power Modes

EZ-BLE Modules support the following five power modes as illustrated in Figure 1:

- Active mode: This is the primary mode of operation. In this mode, all peripherals are available.
- Sleep mode: In this mode, the CPU is in sleep mode, SRAM is in retention, and all the peripherals are available. Any interrupt wakes up the CPU and returns the system to Active mode.
- Deep-Sleep mode: In this mode, the high-frequency clock (IMO[1]) and all high-speed peripherals are off. The WDT[2], LCD, I2C/SPI, link layer, and low-frequency clock (32-kHz ILO[3]) are available. Interrupts from GPIO, WDT, or SCBs[4] can cause a wakeup. The current consumption in this mode is 1.3 µA for all PRoC BLE devices in the family.
- Hibernate mode: This power mode provides a best-in-class current consumption of 150 nA while retaining SRAM, programmable logic, and the ability to wake up from an interrupt generated by a GPIO.
- Stop mode: This power mode retains the GPIO states. On some modules, wakeup is only possible by using the external reset (XRES) pin on the module. The current consumption in this mode is only 60 nA.

Figure 1. Power Modes

Power Mode	Current Consumption (Typical)	Code Execution	Digital Peripherals Available	Analog Peripherals Available	Clock Sources Available	Wake-Up Sources	Wake-Up Time
Active	2.2 mA @ 6 MHz	Yes	All	All	All	-	-
Sleep	1.3 mA	No	All	All	All	Any interrupt source	0
Deep-Sleep	1.3 uA	No	WDT, LCD, I2C/SPI, Link-Layer	POR, BOD	WCO, 32-kHz ILO	GPIO, WDT, SCB	25 µs
Hibernate	150 nA	No	No	POR, BOD	No	GPIO	2 ms
Stop	60 nA	No	No	No	No	XRES	2 ms

3.3 EZ-BLE Module Device Security

EZ-BLE Modules provide a number of options for the protection of flash memory from unauthorized access or copying. Each row of flash has a single protection bit; these bits are stored in a supervisory flash row.

[1] Internal Main Oscillator

[2] Watchdog Timer

[3] Internal Low-Speed Oscillator

[4] Serial Communication Blocks can be configured as an I2C, UART, or SPI interface

3.4 EZ-BLE Marketing Part Number Overview

Cypress offers multiple EZ-BLE Module options to suit each solution's needs. Each device within the EZ-BLE Module family has a unique Marketing Part Number (MPN) used for ordering. The MPN format is shown in Figure 2.

Figure 2. EZ-BLE Module Marketing Part Numbering Format

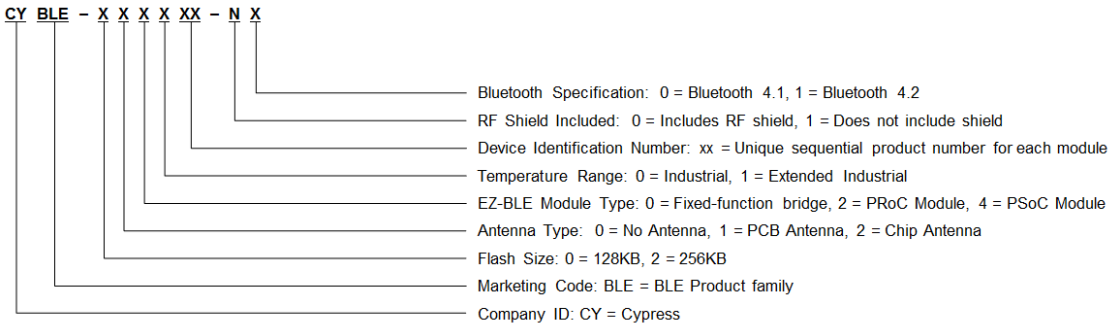


Table 2 summarizes the features and capabilities of each specific EZ-BLE Module Marketing Part Number (MPN) available from Cypress. Click on the specific part number for more detailed information on the device or refer to Appendix B: EZ-BLE Module Product Details.

Table 2. EZ-BLE Module MPN Features and Capabilities

Marketing Part Number	BLE Silicon Device	Module Size (mm)	Range[5]	Regulatory Certification	BLE Standard	Antenna Type	Package	GPIOs	Flash (KB)	SRAM (KB)	SCB	I²S	TCPWM	12-bit SAR ADC	CapSense (# of Sensors)	UDB	Comparator	Opamps
CYBLE-022001-00	PRoC BLE	10 x 10 x 1.8	30	Yes	4.1	Chip	21-SMT[6]	16	128	16	2	Yes	4	Yes	Yes (15)	-	-	-
CYBLE-222005-00	PRoC BLE	10 x 10 x 1.8	30	Yes	4.1	Chip	22-SMT6	16	256	32	2	Yes	4	Yes	Yes (15)	-	-	-
CYBLE-222014-01	PRoC BLE	10 x 10 x 1.8	30	Yes	4.2	Chip	22-SMT6	16	256	32	2	Yes	4	Yes	Yes (15)	-	-	-
CYBLE-012011-00	PRoC BLE	14.5 x 19.2 x 2.0	30	Yes	4.1	Trace	31-SMT	23	128	16	2	Yes	4	Yes	Yes (22)	-	-	-
CYBLE-012012-10	PRoC BLE	14.5 x 19.2 x 1.6	30	No	4.1[7]	Trace	31-SMT	23	128	16	2	Yes	4	Yes	Yes (22)	-	-	-
CYBLE-212019-00	PRoC BLE	14.5 x 19.2 x 2.0	30	Yes	4.1	Trace	31-SMT	23	256	32	2	Yes	4	Yes	Yes (22)	-	-	-
CYBLE-212023-10	PRoC BLE	14.5 x 19.2 x 2.0	30	No	4.1[7]	Trace	31-SMT	23	256	32	2	Yes	4	Yes	Yes (22)	-	-	-
CYBLE-212020-01	PRoC BLE	14.5 x 19.2 x 2.0	30	No	4.2	Trace	31-SMT	23	256	32	2	Yes	4	Yes	Yes (22)	-	-	-
CYBLE-014008-00	PSoC 4 BLE	11 x 11 x 1.8	30	Yes	4.1	Trace	32-SMT	25	128	16	2	Yes	4	Yes	Yes (25)	4	1	4
CYBLE-214009-00	PSoC 4 BLE	11 x 11 x 1.8	30	Yes	4.1	Trace	32-SMT	25	256	32	2	Yes	4	Yes	Yes (25)	4	1	4
CYBLE-214015-01	PSoC 4 BLE	11 x 11 x 1.8	30	Yes	4.2	Trace	32-SMT	25	256	32	2	Yes	4	Yes	Yes (25)	4	1	4
CYBLE-212006-01	PRoC BLE	15.0 x 23.0 x 2.0	400[8]	Yes	4.2	Trace	30-SMT	19	256	32	2	Yes	4	Yes	Yes (18)	-	-	-
CYBLE-202007-01	PRoC BLE	15.0 x 23.0 x 2.05	400[8]	Yes	4.2	-[9]	30-SMT	19	256	32	2	Yes	4	Yes	Yes (18)	-	-	-
CYBLE-202013-11	PRoC BLE	15.0 x 23.0 x 1.55	400[8]	No	4.2	-[9]	30-SMT	19	256	32	2	Yes	4	Yes	Yes (18)	-	-	-
CYBLE-224110-00	PSoC 4 BLE	9.5 x 15.4 x 1.8	400[8]	Yes	4.1	Chip	32-SMT	25	256	32	2	Yes	4	Yes	Yes (25)	4	1	4
CYBLE-224116-01	PSoC 4 BLE	9.5 x 15.4 x 1.8	400[8]	Yes	4.2	Chip	32-SMT	25	256	32	2	Yes	4	Yes	Yes (25)	4	1	4

[5] Measured in meters and is specified as direct Line-of-Sight (LoS) in a noise-free environment with no obstacles.

[6] CYBLE-222005-00 and CYBLE-222014-01 are drop-in compatible with the CYBLE-022001-00. The additional pin included on the CYBLE-222005-00 and CYBLE-222014-01 is the V_{REF} input pin, which does not impact drop-in compatibility.

[7] CYBLE-012012-10 and CYBLE-212023-10 operate to the BT 4.1 standard, but are not qualified with the Bluetooth SIG and do not contain a QDID.

[8] To enable 400-meter range on the Extended Range EZ-BLE modules, please refer to the module datasheet or to the specific Appendix Section of this document for each respective module.

[9] The CYBLE-212007-01 module includes a micro-FL (u.FL) RF connector to connect to an external antenna. The CYBLE-202013-011 includes an RF solder pad for connection to an external antenna.

4 Development Tools

Cypress supports the EZ-BLE Modules with high-quality software tools, with access to a suite of world-class Integrated Design Environments (IDEs).

Cypress provides the following software to get started with a EZ-BLE Module design:

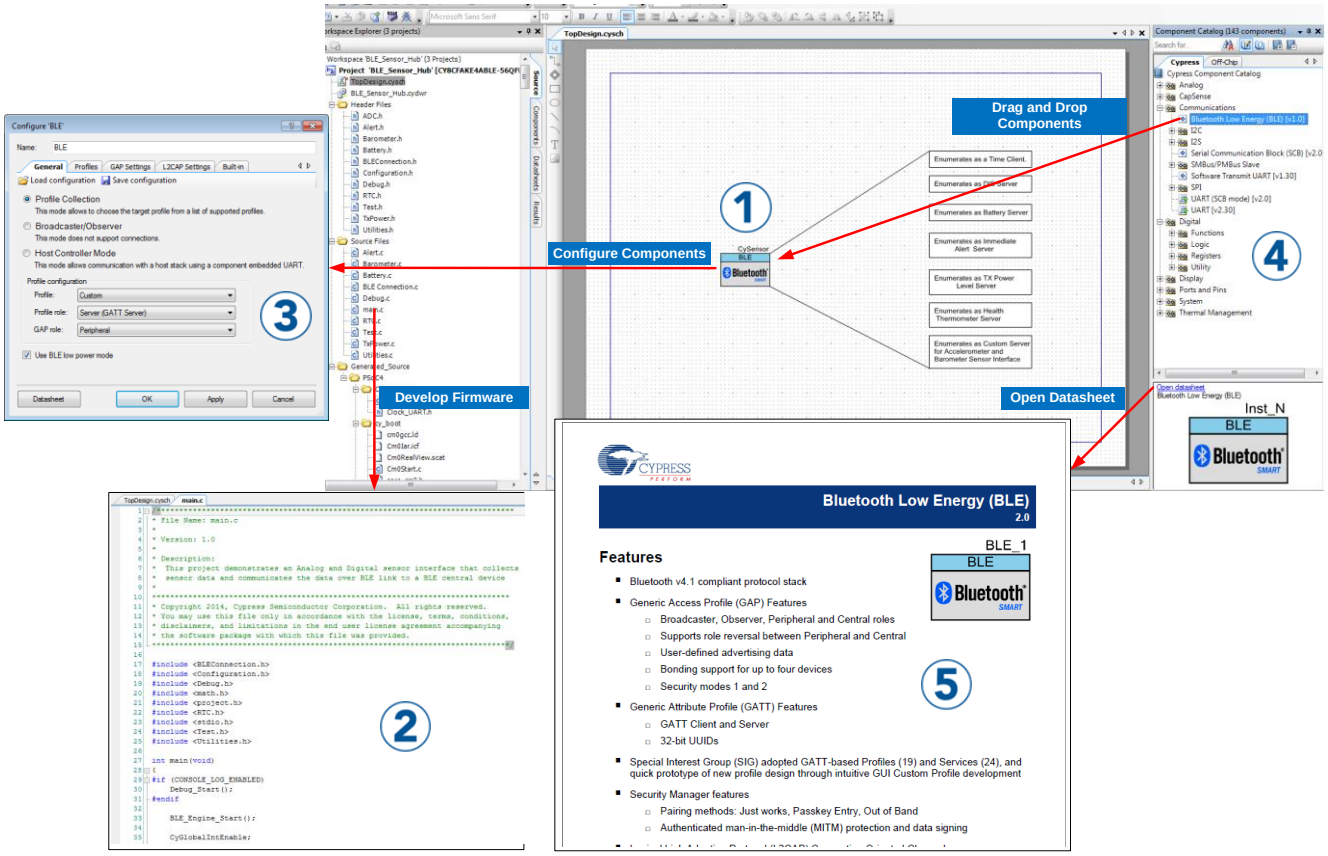
1. PSoC Creator
2. Bluetooth Low Energy Component (part of PSoC Creator)
3. CySmart PC application
4. CySmart Android app
5. CySmart iOS app

4.1 PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables you to design hardware and firmware systems concurrently. As Figure 3 shows, with PSoC Creator, you can:

1. Drag and drop Components to build your hardware system design in the main design workspace.
2. Co-design your application firmware with the PSoC hardware.
3. Configure the Components using configuration tools.
4. Explore the library of more than 100 Components.
5. Review the Component datasheets.

Figure 3. PSoC Creator Schematic Entry and Components



4.2 PSoC Creator Help

Visit the PSoC Creator home page to download and install the latest version of PSoC Creator. Then launch PSoC Creator and navigate to the following items:

- **Quick Start Guide**: Choose **Help** > **Documentation** > **Quick Start Guide**. This guide gives you the basics for developing PSoC Creator projects.
- **Simple Component example projects**: Choose **File** > **Open** > **Example projects**. These example projects demonstrate how to configure and use PSoC Creator Components.
- **Starter designs**: Choose **File** > **New** > **Project** > **PSoC 4 Starter Designs**. These starter designs demonstrate the unique features of PSoC 4 BLE.
- **System Reference Guide**: Choose **Help** > **System Reference** > **System Reference Guide**. This guide lists and describes the system functions provided by PSoC Creator.
- **Component datasheets**: Right-click a Component and select “Open Datasheet.” Visit the PRoC BLE Component Datasheets page for a list of all PSoC 4 BLE Component datasheets.
- **Document Manager**: PSoC Creator provides a document manager to help you to easily find and review document resources. To open the document manager, choose the menu item **Help** > **Document Manager**.

4.3 Bluetooth Low Energy Component

The Bluetooth Low Energy Component inside PSoC Creator provides a comprehensive GUI-based configuration window that lets you quickly design BLE applications. The Component incorporates a Bluetooth Core Specification v4.1- or v4.2-compliant BLE protocol stack and provides API functions to enable user applications to interface with the underlying Bluetooth Low Energy Sub-System (BLESS) hardware via the stack.

The Component supports the SIG-adopted GATT-based profiles and services as well as custom BLE profiles and services, and it allows various GAP and GATT roles to be configured. The Component generates the necessary code for a particular profile and service operation, as configured in the GUI, abstracting the underlying BLE stack and hardware configuration so that you can concentrate on the system design.

The BLE Component also provides profile Application Programming Interfaces (APIs) to design BLE solutions without requiring manual stack-level manipulation. The exception to this is the L2CAP configuration specified in Bluetooth v4.1, which allows advanced users to configure the L2CAP layer of the stack if desired.

See AN91267 - Getting Started with PSoC® 4 BLE for a detailed overview of Bluetooth Low Energy (BLE) and the BLE Component.

4.4 CySmart PC Application

The CySmart Host Emulation Tool is a Windows application that emulates a BLE Central device using the BLE Pioneer Kit’s BLE Dongle; see Figure 12. It is installed as a part of the BLE Pioneer Kit installation and can be launched from right-click options in the BLE Component. It provides a platform for you to test your EZ-BLE Module Peripheral implementation over GATT or L2CAP connection-oriented channels by allowing you to discover and configure the BLE Services, Characteristics, and Attributes on your Peripheral.

Operations that you can perform with CySmart Host Emulation Tool include, but are not limited to:

- Scan BLE Peripherals to discover available devices to which you can connect.
- Discover available BLE Attributes including Services and Characteristics on the connected Peripheral device.
- Perform read and write operations on Characteristic values and descriptors.
- Receive Characteristic notifications and indications from the connected Peripheral device.
- Establish a bond with the connected Peripheral device using BLE Security Manager procedures.
- Establish a BLE L2CAP connection-oriented session with the Peripheral device and exchange data per the Bluetooth 4.1 specification.

Figure 4 and Figure 5 show the user interface of CySmart Host Emulation Tool. For more information on how to set up and use this tool, see the CySmart user guide from the **Help** menu.

Figure 4. CySmart Host Emulation Tool Master Device Tab

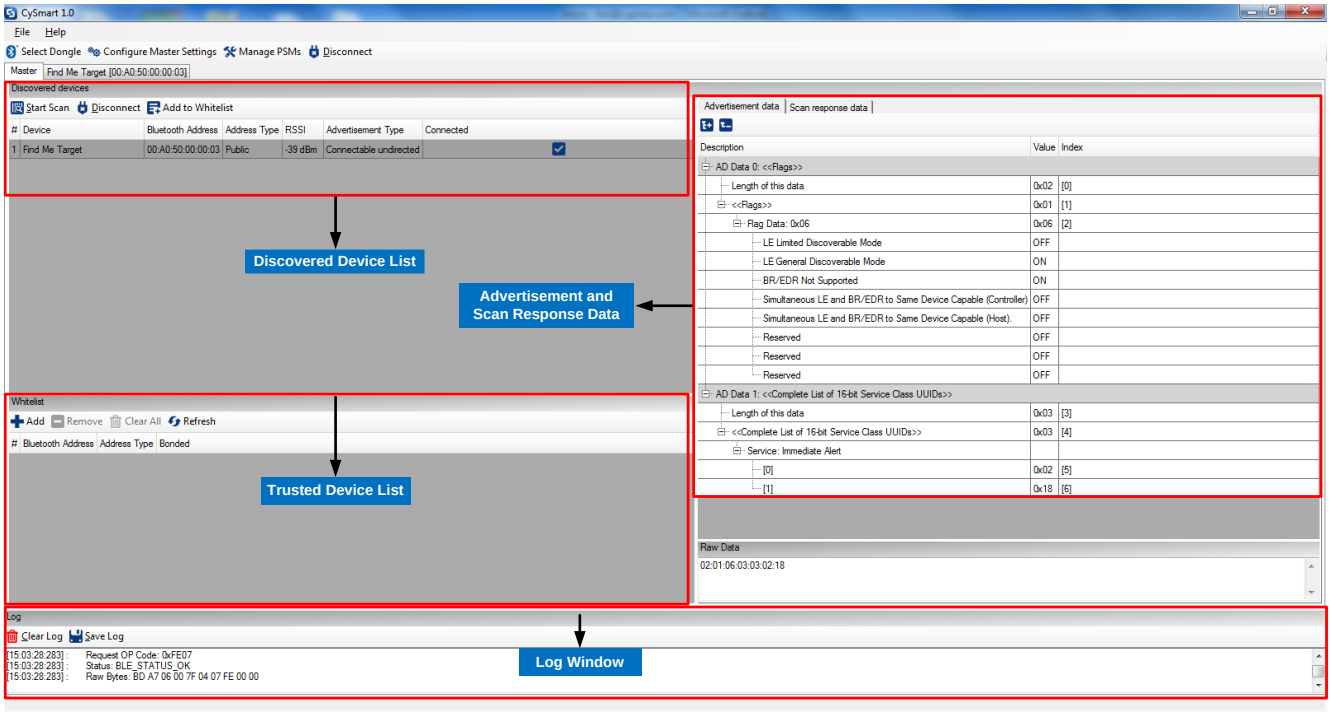
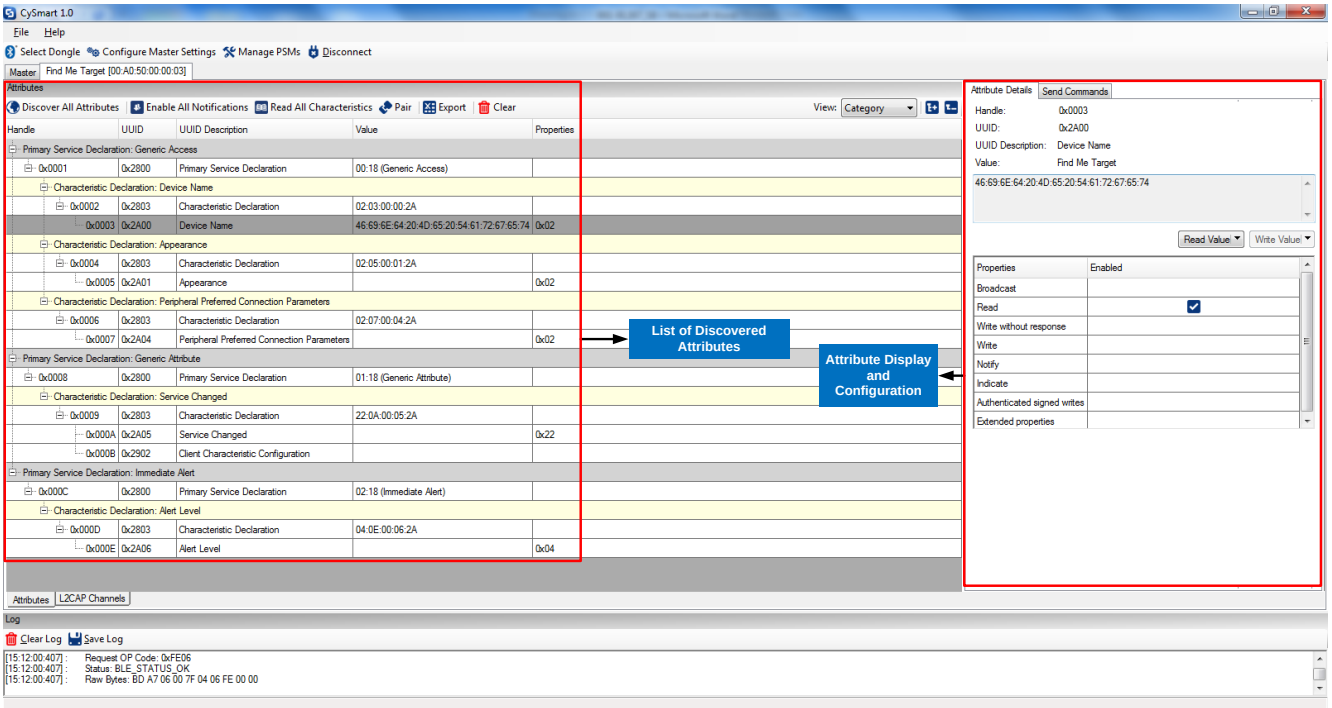


Figure 5. CySmart Host Emulation Tool Peripheral Device Attributes Tab



4.5 CySmart Mobile App

In addition to the PC tool, you can download the CySmart mobile app for iOS or Android from the respective app stores. This app uses the iOS Core Bluetooth framework and the Android built-in platform framework for BLE respectively to configure your BLE-enabled smartphone as a Central device that can scan and connect to Peripheral devices.

The mobile app supports SIG-adopted BLE standard Profiles through an intuitive GUI and abstracts the underlying BLE Service and Characteristic details. In addition to the BLE standard Profiles, the app demonstrates a custom Profile implementation using Cypress's LED and CapSense demo examples. Figure 6 and Figure 7 show a set of CySmart app screenshots for the Heart Rate Profile user interface. For a description of how to use the app with BLE Pioneer Kit example projects, see the *BLE Pioneer Kit Guide*.

Figure 6. CySmart iOS App Heart Rate Profile Example

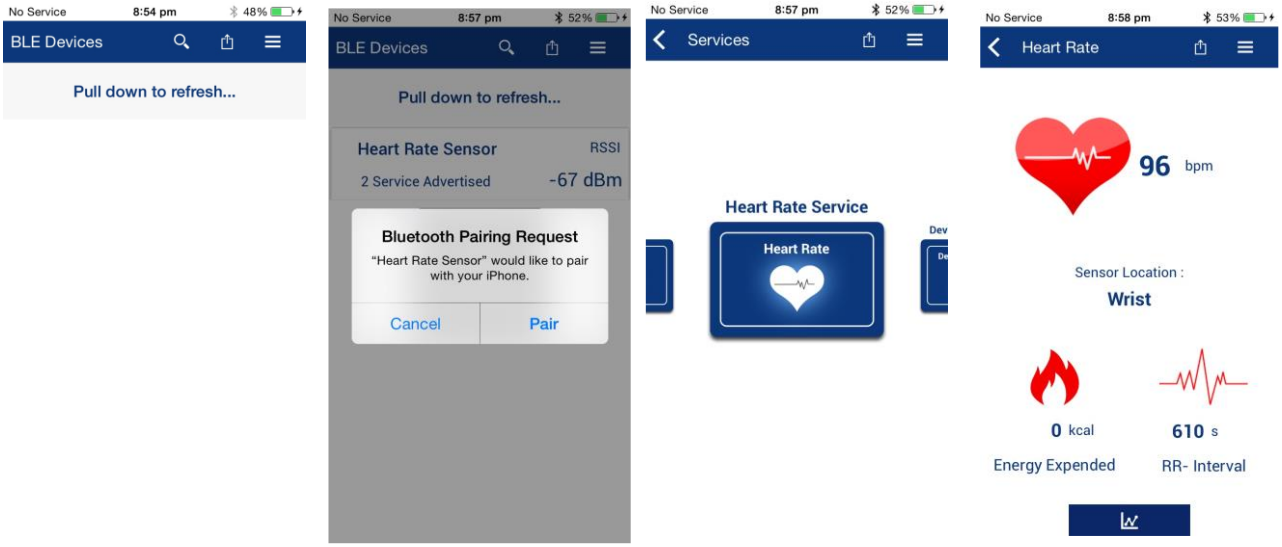
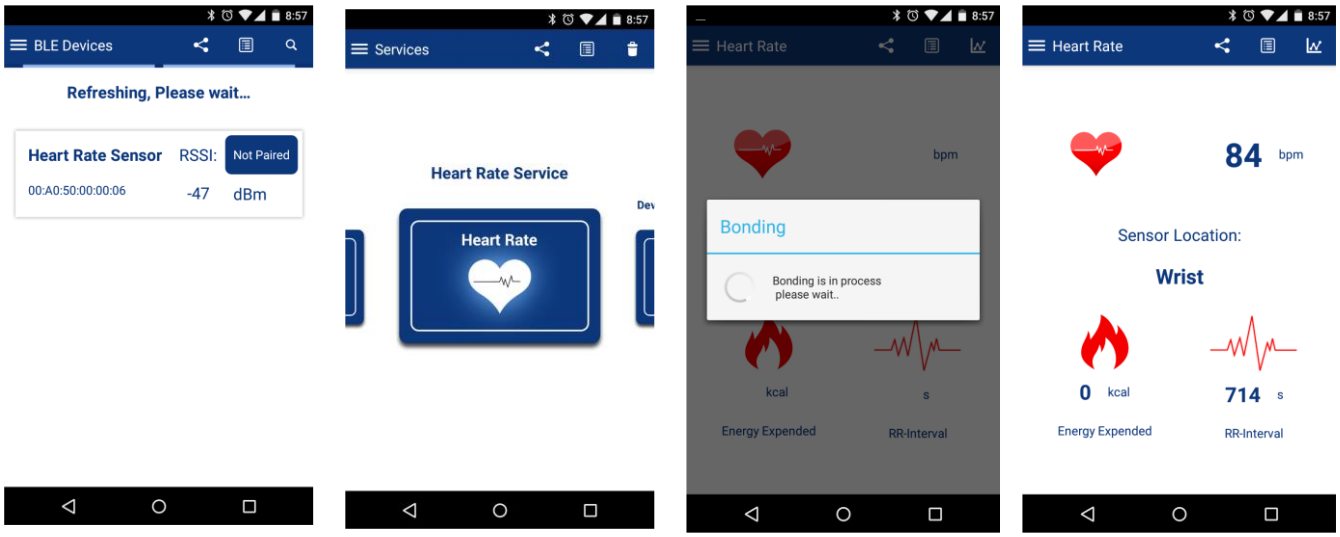


Figure 7. CySmart Android App Heart Rate Profile Example



5 Development Kits and Evaluation Boards

Cypress provides an easy-to-use development kit to help you prototype your EZ-BLE Module design.

5.1 CY8CKIT-042-BLE-A Pioneer Kit

The CY8CKIT-042-BLE-A Pioneer Kit, as shown in Figure 8, is an Arduino Uno-compliant BLE development kit for the PRoC BLE and PSoC 4 BLE family of devices, including EZ-BLE Modules. The CY8CKIT-042-BLE-A kit consists of pluggable BLE modules that connect to a baseboard. The Pioneer Kit can be powered through the USB interface or with a coin cell battery.

The Pioneer baseboard and RF module combination enables you to develop battery-operated low-power BLE designs that work in conjunction with standard Arduino shields and additional PSoC 4 and PRoC BLE device capabilities such as the CapSense user interface on the Pioneer baseboard.

The kit contains a BLE USB dongle that acts as a BLE master and works with the CySmart application to provide a BLE master emulation platform on non-BLE Windows systems.

Cypress offers evaluation boards for each of the EZ-BLE Modules to evaluate and develop with the Cypress module without the need to design custom hardware.

Figure 8. BLE 4.2 Pioneer Kit

The kit includes of a set of BLE example projects and documentation that should help you get started with developing your own BLE applications. Visit www.cypress.com/CY8CKIT-042-BLE-A to get latest updates on the kit and to download kit design, example projects, and documentation files.

5.2 EZ-BLE Evaluation Boards

For details and images of each EZ-BLE Evaluation Board, see Appendix C: EZ-BLE Evaluation Board Details.

The EZ-BLE Evaluation Boards are designed to fan out the connections of each respective EZ-BLE Module to headers compatible with the CY8CKIT-042-BLE and CY8CKIT-042-BLE-A Pioneer Kits. The EZ-BLE Evaluation boards allow you to evaluate the Cypress EZ-BLE Modules without having to design custom hardware to mount the Cypress EZ-BLE Module.

Table 3 lists each of the available EZ-BLE Modules and their corresponding evaluation board part numbers. Click on your evaluation board for additional information.

Table 3. EZ-BLE Modules and Corresponding Evaluation Board Part Numbers

EZ-BLE Module Part Number	EZ-BLE Evaluation Board Part Number
CYBLE-022001-00	CYBLE-022001-EVAL
CYBLE-222005-00	CYBLE-222005-EVAL
CYBLE-222014-01	CYBLE-222014-EVAL
CYBLE-012011-00	CYBLE-012011-EVAL
CYBLE-012012-10	CYBLE-012011-EVAL
CYBLE-212019-00	CYBLE-212019-EVAL
CYBLE-212023-10	CYBLE-212019-EVAL
CYBLE-212020-01	CYBLE-212020-EVAL
CYBLE-014008-00	CYBLE-014008-EVAL
CYBLE-214009-00	CYBLE-214009-EVAL
CYBLE-214015-01	CYBLE-214015-EVAL
CYBLE-212006-01	CYBLE-212006-EVAL
CYBLE-202007-01	CYBLE-202007-EVAL
CYBLE-202013-11	CYBLE-202013-EVAL
CYBLE-224110-00	CYBLE-224110-EVAL
CYBLE-224116-01	CYBLE-224116-EVAL

Each EZ-BLE Evaluation Board contains the following components:

- Cypress EZ-BLE Module – soldered directly to the Evaluation Board
- PCB substrate used for I/O fan out
- Connection headers
- C_{mod} capacitor (for use with Capacitive Sensing elements on the CY8CKIT-042-BLE-A kit).

  Note: Certain EZ-BLE Modules integrate the C_{mod} capacitor on the module (for example, CYBLE-014008-00). In these cases, the associated EZ-BLE evaluation board will not include an addition C_{mod} capacitor.

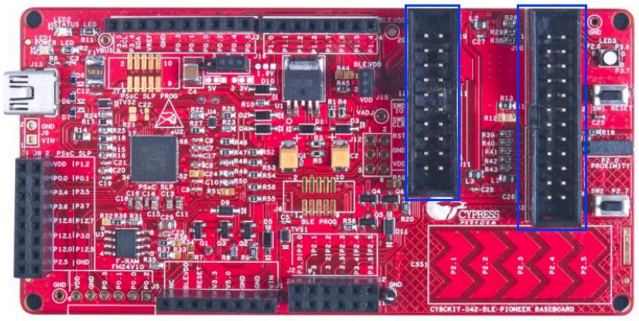
- Inductors (for power supply noise reduction) – refer to your EZ-BLE Module datasheet for recommended external components)

EZ-BLE Evaluation Boards are designed to simulate the placement and connection of the EZ-BLE Modules in a final application. All host-side layout pattern recommendations (as shown in each specific module's datasheet) are followed for each evaluation board.

Note that not all connections available on the CY8CKIT-042-BLE-A are populated on the EZ-BLE Evaluation Boards. This is due to the number of I/Os supported on the EZ-BLE Modules. When designing applications, PSoC Creator will only display connections that are available on the specific EZ-BLE Module that you are designing with. See Appendix C: EZ-BLE Evaluation Board Details for details on the connections available for each of the EZ-BLE Evaluation Boards and the corresponding connections on the CY8CKIT-042-BLE-A development kit.

To place any of the EZ-BLE Module Evaluation Boards on the CY8CKIT-042-BLE-A baseboard, locate the 20-pin (J11) and 24-pin (J10) connection headers, as shown in Figure 9.

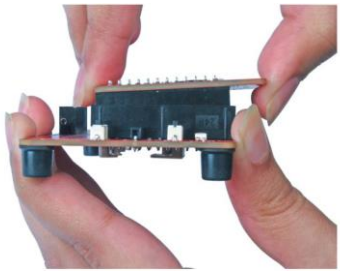
Figure 9. CY8CKIT-042-BLE-A Baseboard with J10 and J11 Headers to Connect the EZ-BLE EVAL Board



Plug the EZ-BLE Evaluation Board into the CY8CKIT-042-BLE-A baseboard on headers J10 and J11, while keeping the antenna directed outside. See Appendix C: EZ-BLE Evaluation Board Details for images showing proper connection to the CY8CKIT-042-BLE-A baseboard for each module. Note that there are notches on both the J10 and J11 headers that will ensure proper insertion orientation.

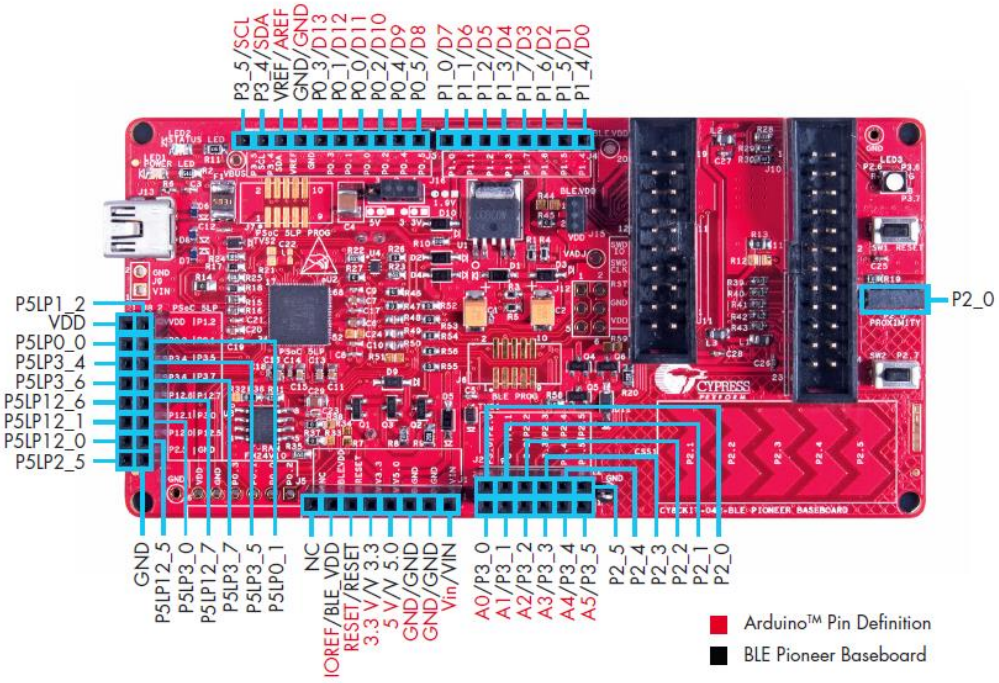
To remove the EZ-BLE Evaluation Board from the CY8CKIT-042-BLE-A baseboard, hold the CY8CKIT-042-BLE-A baseboard in one hand and the EZ-BLE Evaluation Board in the other, as shown in Figure 10, and pull it out using a rocking motion.

Figure 10. Removing the EZ-BLE Evaluation Board from the CY8CKIT-042-BLE-A Baseboard



Each of the connections made from the EZ-BLE Evaluation Board to the CY8CKIT-042-BLE-A baseboard are accessible on the Arduino-compatible headers located on the CY8CKIT-042-BLE-A baseboard. Figure 11 shows the Arduino-compatible headers and port-pin identifiers located on the CY8CKIT-042-BLE-A baseboard.

Figure 11. Arduino Compatible Headers on CY8CKIT-042-BLE-A Baseboard



The connections above are labeled according to the CY8CKIT-042-BLE-A baseboard pinout. For the equivalent and available connections used with your EZ-BLE Evaluation Board, see Appendix C: EZ-BLE Evaluation Board Details. For additional information on the CY8CKIT-042-BLE-A, see the CY8CKIT-042-BLE-A product web page.

6 EZ-BLE Module Development Setup

Figure 12 shows the hardware and software tools required for evaluating BLE Peripheral designs using the EZ-BLE Module Evaluation Boards (for example, CYBLE-022001-EVAL – green board in Figure 12). The BLE Pioneer Kit (red board in Figure 12) acts as a Peripheral that can communicate with either a CySmart iOS/Android app or the CySmart Host Emulation Tool that acts as a Central device. The CySmart Host Emulation Tool also requires a BLE Dongle (black board in Figure 12) for its operation. The dongle is included in the CY8CKIT-042-BLE-A kit. The development system setup required for programming and debugging a BLE design is shown in Figure 13.

Figure 12. BLE Functional Setup

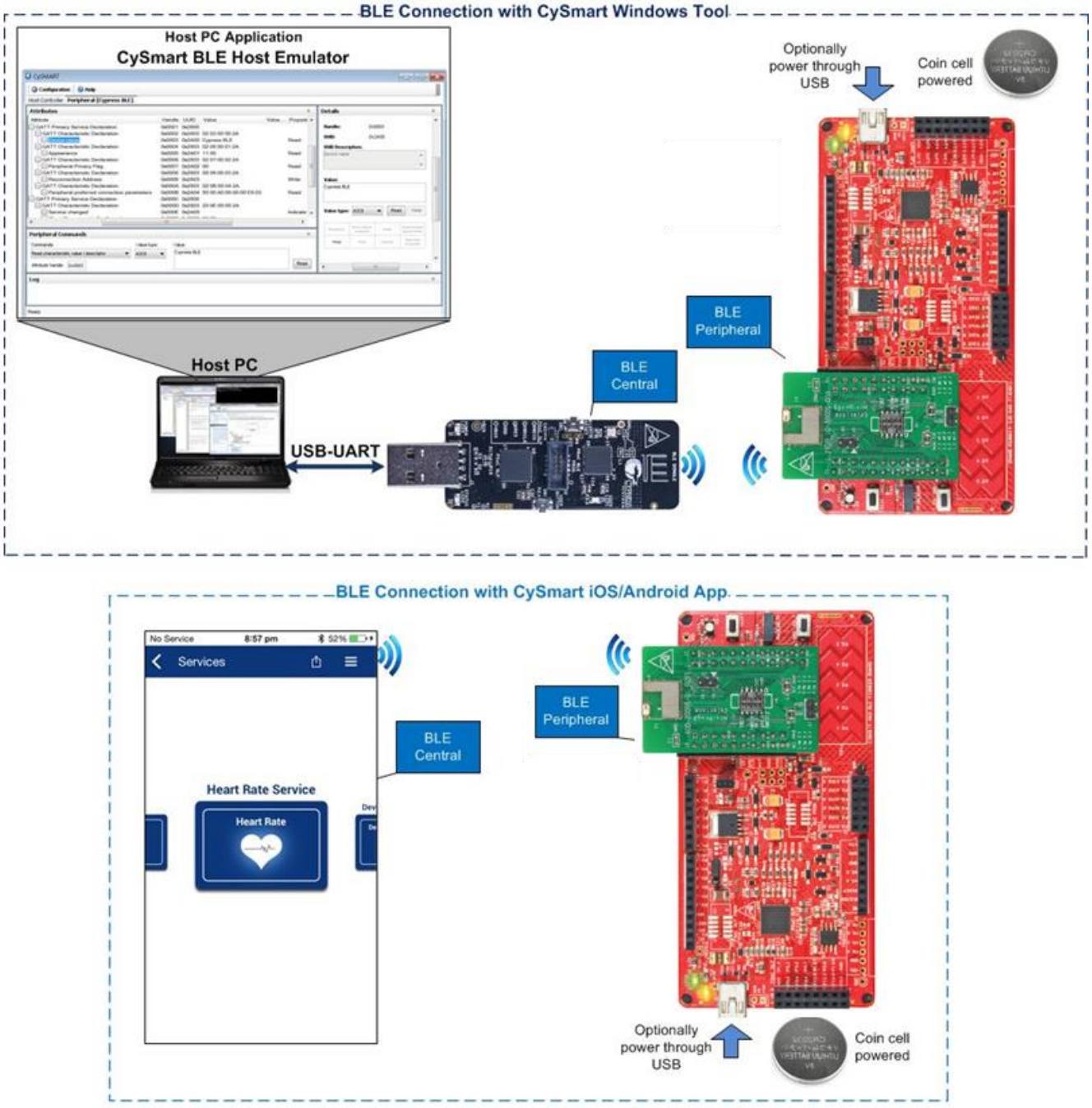
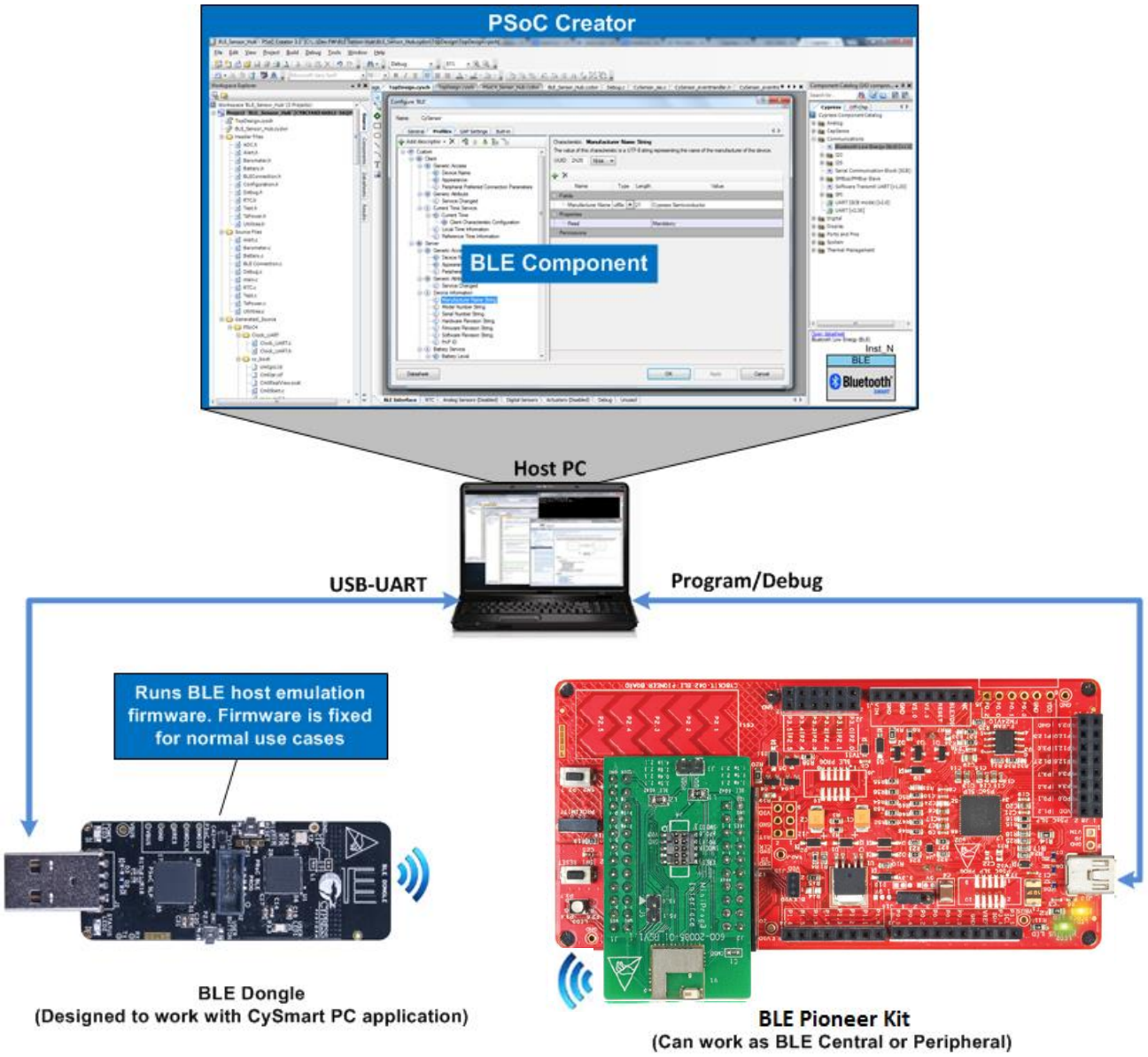


Figure 13. BLE Development Setup



The My First EZ-BLE Module Design section will walk you through a step-by-step configuration of the BLE Component for creating a simple Peripheral application. You may refer to application notes AN91184 and AN91162 for a step-by-step description of how to use the BLE Component to develop applications using BLE standard and custom Profiles.

7 Module Placement and Enclosure Considerations

EZ-BLE Modules are designed to be soldered to a host PCB to provide seamless BLE connectivity. To maximize RF performance of the final product, care needs to be taken on the placement of the module and antenna. This section describes in detail the recommended placement of the module on a host board to ensure optimal RF performance. This section also details the effect of metallic or nonmetallic enclosure and metal obstructions near the EZ-BLE Module.

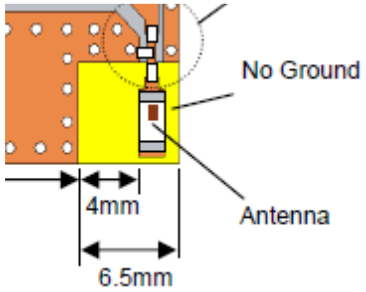
7.1 Antenna Ground Clearance

A monopole antenna requires that no ground plane is below the antenna. The ground plane below it will not allow the field to propagate. This is defined as the Ground Clearance requirement. However, after some distance, a ground must be present for a monopole antenna. Defining this region is a very significant step for any antenna design. The Ground Clearance region defines the bandwidth and the efficiency of the antenna.

Each specific EZ-BLE Module Marketing Part Number specifies the Ground Clearance used for the design of the module, and offers recommended additional ground keep-out area to maximize the RF performance. The examples below reference the CYBLE-022001-00 module specifically. For details on other modules, see the specific module datasheet.

The CYBLE-022001-00 uses the Johansson 2450AT18B100 chip antenna. The datasheet of the antenna requires a Ground Clearance of 6.5 mm × 6.5 mm when placed as shown in Figure 14.

Figure 14. Antenna Clearance



In Figure 14, the chip antenna is placed at the edge of the module. The yellow area in Figure 14 does not have any ground on any layer. The module placement in a host board needs to ensure that no traces or ground layers of the host board comes within this region. Any ground plane below a monopole antenna degrades the radiation and adversely affects the RF efficiency.

7.2 Module Placement in a Host System

The EZ-BLE Module is soldered to a host board and a clearance must be provided for the antenna where no routing or ground is allowed on any layer. Placing the module at the edge of the host board is recommended as it provides the best RF performance and simplifies the requirement of not routing signal or ground traces under the antenna Ground Clearance region. Figure 15 shows four placement options on a host board, with option 1 being the most efficient.

Figure 15. Module Placement in a Host Board

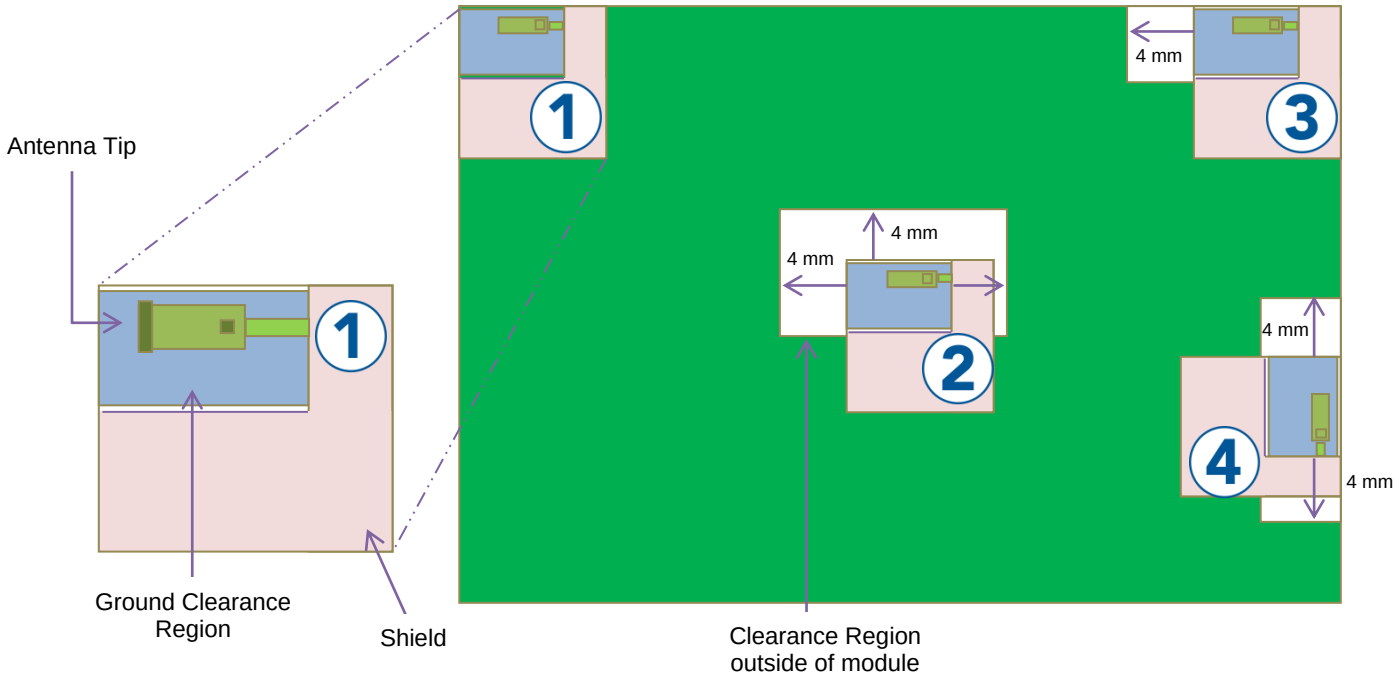


Figure 15 shows an example of four positions of the module in a host board, “1”, “2”, “3”, and “4”. The white area shown around the module is the clearance area. For the antenna in question, it is recommended to provide a clearance area of 4 mm in each direction. For details on the recommended clearance area for your EZ-BLE Module, see the specific module datasheet.

As can be seen in Figure 15, when placing the module at the edge of the host board, the additional clearance area is not required as the antenna is facing outwards (with no possibility of signal or ground traces to be beneath the antenna Ground Clearance region). Conversely, if the module is placed in the middle (placement option “2”) of the host board, the clearance area must be provided in order to achieve an optimal RF performance.

Placement option “1” is the best option shown in Figure 15, because it removes the need to reroute signal or ground traces away from the Ground Clearance region of the module (because no GPIO are located at the top left corner of the module). Furthermore, it does not require any additional clearance area, because the antenna faces outward, with the antenna tip exposed to open space.

In placement options “3” and “4”, although the module is placed at the edge of the host board, the antenna tip is not exposed to free space.

Placement option “2” not only wastes PCB real estate, but also provides diminished RF performance compared to position “1”, as we can have traces facing the antenna tip.

7.3 Enclosure Effects on Antenna Performance

Antennas used in consumer products are sensitive to the PCB RF ground size, the product's plastic casing, and metallic enclosures. This section describes the effect of each of these environmental factors on RF performance.

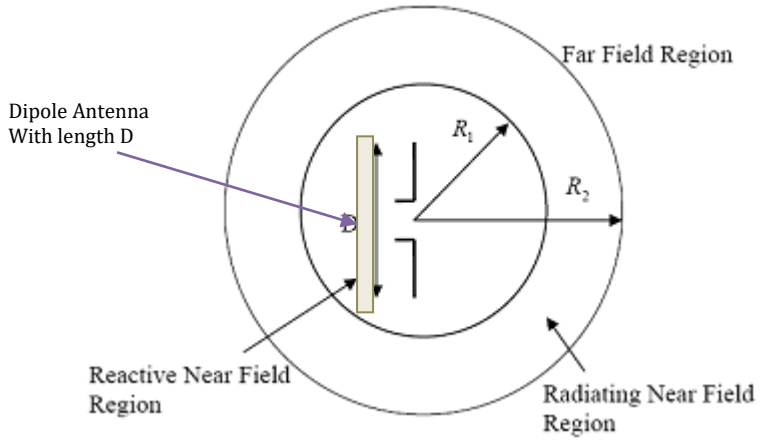
7.3.1 Antenna Near Field and Far Field

Every antenna contains two regions surrounding it: 1) the near field and 2) the far field.

The near field is the region where the radiated field has not yet formed. In this region, the electric and magnetic fields are not orthogonal to each other. This region is very close to the antenna in distance. The near-field region has two regions: the reactive near-field region and the radiating near-field region. The transition to a far-field region happens in the radiating near-field region.

The radiation field is formed after the transition to the far field region. In this region, the relative angular variation of the field does not depend on the distance. This means that if we plot the angular radiation field at a distance from the antenna in the far-field region, their shapes remain the same. Only with distance, the field strength decreases. However, the shape of the radiation pattern remains the same with respect to the angular variation. This region is called the far-field region. An object in the far field does not affect the radiation pattern much. However, any obstruction in the near field can completely change the radiation pattern. If the obstruction is metal, the effect on the radiation pattern is much more pronounced. Figure 16 shows the regions for a dipole antenna.

Figure 16. Near and Far Field



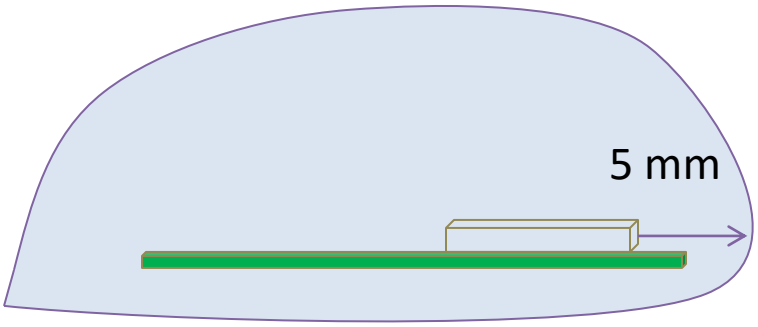
For a module based on a 2.4-GHz chip antenna, the near field extends up to 4 mm.

7.3.2 Effect of Nonmetallic Enclosure

Any plastic enclosure changes the resonating frequency of the antenna. The antenna can be modeled as an LC resonator whose resonant frequency decreases when either L (inductance) or C (capacitance) increases. A larger RF ground plane and plastic casing increase the effective capacitance and thus reduce the resonant frequency. See the application note AN91445 for more details on the effect of an enclosure.

Figure 17 details a module antenna in a plastic enclosure. The clearance from the antenna to the plastic enclosure can be as little as 2 mm. However, clearance of this amount can affect the tuning of the antenna. This can be resolved by retuning the antenna; however for a module solution, it is not recommended to attempt retuning of the antenna. To minimize effects on the module antenna, it is recommended to have a minimum clearance of 5 mm.

Figure 17. Cypress EZ-BLE Module Inside of a Plastic Mouse Enclosure

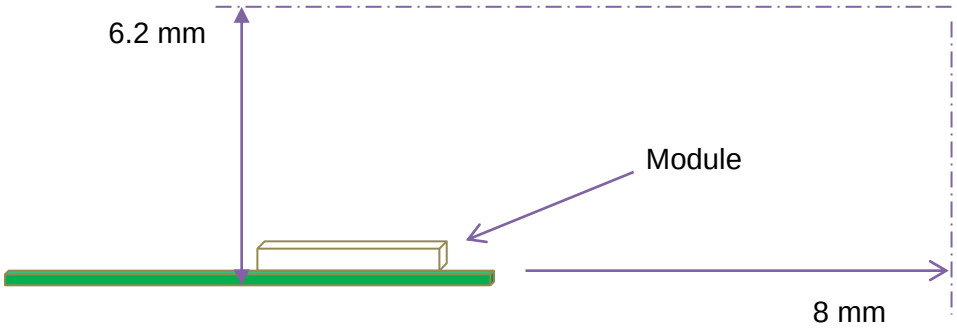


7.3.3 Effect of Metallic Objects

An antenna is sensitive to the presence of metallic objects in its vicinity. A metallic object shorts the electric field and thus changes the radiation field. Depending on the size of the obstruction, electromagnetic waves go through different diffraction patterns or may be completely shielded by the metallic object.

Metallic objects in the near field can have a drastic impact on the radiation pattern. The thickness of the CYBLE-022001-00 module is 1.8 mm (including the antenna) and the near field of this module extends up to 4 mm from the antenna. Therefore, it is recommended that any metallic obstruction be at least 6.2 mm away from the PCB plane to avoid negative effects to the RF performance. Cypress recommends an 8-mm gap from the module PCB plane to any metallic enclosure. Figure 18 details the required clearance from the EZ-BLE Module to small metal obstructions.

Figure 18. Clearance from Small Metal Obstructions



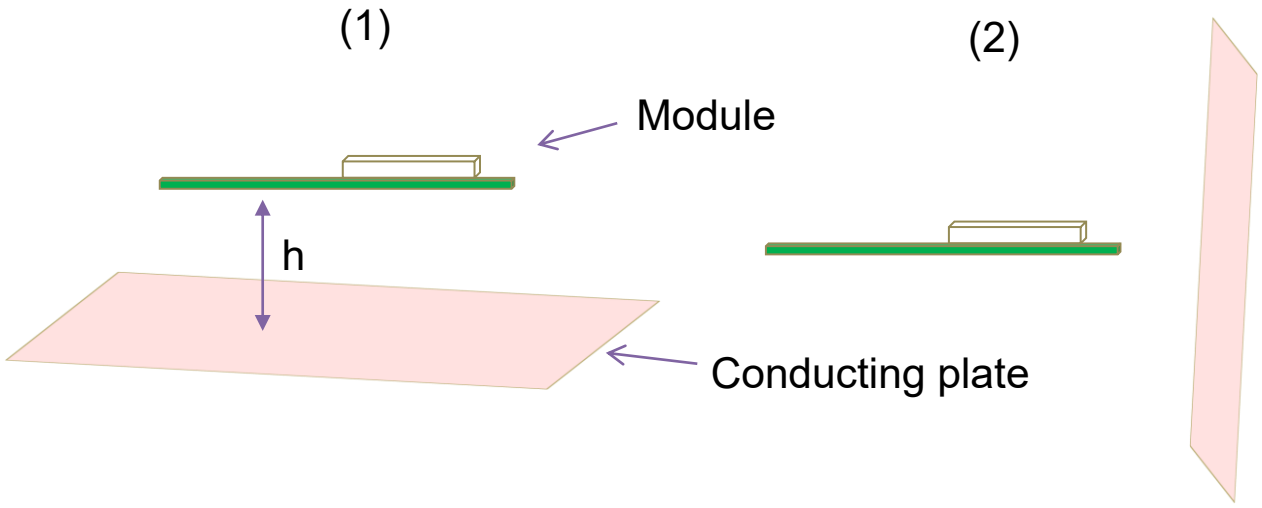
7.3.4 Recommendations for Placement over a Large Metal Plane

The other effect of metal is the formation of an image antenna. The best practice in this case is to orient the metal orthogonal to the antenna to ensure minimum effects. If the length or width of the plane approaches the size of the module, it is considered a large metal objects near the antenna. Figure 19 details two placement options for this scenario. Of these two placement options, option “1” should be avoided.

It is recommended to not have any large metallic objects parallel to the antenna. This has a drastic effect because the image antenna is of opposite polarity. The interference caused by such an antenna is destructive to the RF radiation.

If it is not possible to avoid a large metallic object running parallel to the module plane, then it is recommended to maintain a distance (h) of at least 30 mm. This will ensure that the interference caused by the image antenna will not be completely destructive. The radiation will be strongly directional below the 30-mm distance and the efficiency will dramatically drop at a distance (h) below 8 mm. At a distance (h) of around 2 mm, the radiation efficiency can go below 20%.

Figure 19. Clearance from a Large Metal Plane



7.4 Guidelines for Enclosures and Ground Plane

The best practices with respect to enclosure design and ground planes are summarized:

- Ensure that there is no component, mounting screw, or ground plane near the tip or the length of the antenna located on the EZ-BLE Module.
- Ensure that no battery cable, microphone cable, or trace crosses the antenna trace on the PCB.
- Ensure that the antenna is not completely covered by a metallic enclosure. If the product has a metallic casing or shield, the casing should not cover the antenna. No metal is allowed in the antenna near the field.
- Ensure that paint on plastic enclosures is nonmetallic near the antenna.
- The orientation of the antenna should be in-line with the final product orientation (if possible) so that radiation is maximized in the desired direction. The polarization of the receive antenna and the position of the receive antenna should be taken into account so that the module can be oriented to maximize radiation.
- There should not be any ground directly below the antenna Ground Clearance region of the module.

8 Manufacturing with EZ-BLE Modules

EZ-BLE Modules are intended to be used with traditional Surface Mount Technology (SMT) manufacturing lines and are compatible with industry-standard reflow profiles for Pb-free solders.

8.1 SMT Manufacturing Pick-and-Place

The EZ-BLE Modules should be picked up from the topside of the module using industry-standard pick-and-place machinery and nozzles. The ideal location for picking up the module is on the shield area of the module. For the optimal location for your EZ-BLE Module, see the module's datasheet.

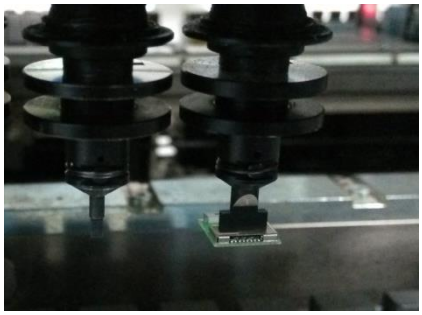
Each EZ-BLE Module marketing part number has a unique center-of-mass detailed in each product's datasheet. This center-of-mass is the area that represents the optimal location to pick up the unit with the nozzle. Using the center-of-mass guidelines for pick-and-place location will minimize SMT line disturbances caused by units releasing prematurely from the nozzle.

Figure 20 shows an image of a nozzle used by Cypress manufacturing the CYBLE-022001-EVAL Evaluation Board product. See the center-of-mass dimensions in each module's datasheet to select an appropriate nozzle for your manufacturing line equipment.

Figure 20. Nozzle Used by Cypress for Evaluation Board Production

Figure 21 shows an image of the CYBLE-022001-00 picked up at the center-of-mass by the nozzle referenced above.

Figure 21. Image of Nozzle Used by Cypress for Evaluation Board Production



8.2 Manufacturing Solder Reflow

EZ-BLE Modules are compatible with industry-standard reflow profiles for Pb-free solder. Table 4 details the solder reflow specifications for all EZ-BLE Modules.

Table 4. EZ-BLE Module Solder Reflow Specification

Module Package	Maximum Peak Temperature	Time at Maximum Temperature
All Packages	260 °C	30 seconds

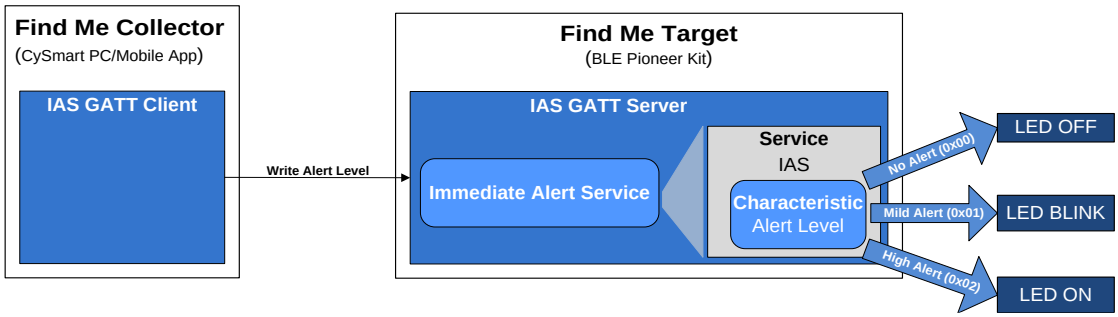
9 My First EZ-BLE Module Design

This section gives you a step-by-step process for building a simple BLE Pioneer Kit-based design with the EZ-BLE Module Evaluation Board using PSoC Creator. This example project is specific to the CYBLE-022001-EVAL Evaluation Board (using the CYBLE-022001-00 EZ-BLE PRoC Module).

9.1 About the Design

This design implements a BLE Find Me Profile in the Target role that consists of an Immediate Alert Service (IAS). Alert levels triggered by the Find Me Locator are indicated by varying the state of a LED on the BLE Pioneer Kit, as Figure 22 shows. Two status LEDs indicate the state of the BLE interface.

Figure 22. My First EZ-BLE Module Design



9.2 Prerequisites

Before you get started with the implementation, make sure that you have a BLE Pioneer Kit, the CYBLE-022001-EVAL board, and have installed the following software:

- PSoC Creator 4.1 or later with PSoC Programmer 3.26 or later
- CySmart Host Emulation Tool or CySmart iOS/Android app

You can create your first EZ-BLE PRoC Module design in four steps:

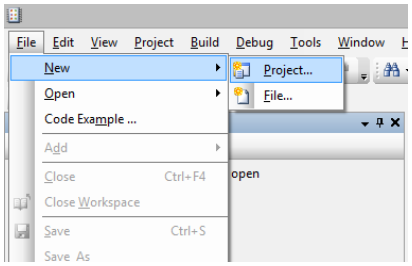
1. Configure the design in the PSoC Creator schematic page.
2. Write the firmware to initialize and handle BLE events.
3. Program the EZ-BLE PRoC Module on the BLE Pioneer Kit.
4. Test your design using the CySmart Host Emulation Tool or mobile application.

9.3 Part 1: Configure the Design

This section takes you on a step-by-step guided tour of the design process. It starts with creating an empty project and guides you through schematic design entry. You can skip this section if you simply wish to try the example project provided with this application note without going through the build process.

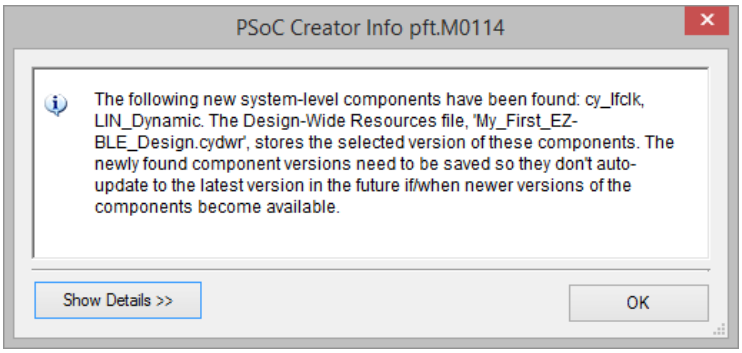
1. Install PSoC Creator 4.1 or newer on your PC. After installation, a registration page for Keil license will be shown.
2. Start PSoC Creator, and from the **File** menu, choose **New** > **Project**, as Figure 23 shows.

Figure 23. Creating a New Project



Note: If you choose to open the completed example project directly instead of creating the project from scratch, you may be informed that your version of PSoC Creator has newer components available than were used in the creation of the example project associated with this application note. The information screen will appear as shown in Figure 24. The details contained in this screen will differ based on the version of PSoC Creator being used.

Figure 24. Component Update Information

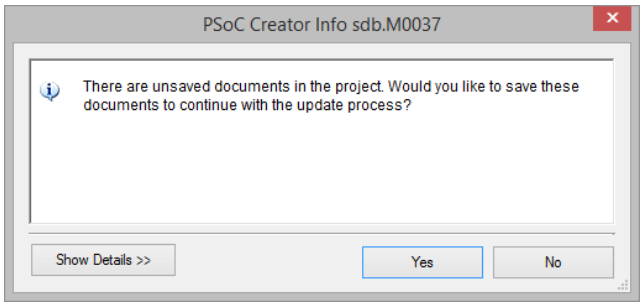


3. Select **OK** and your workspace opens. To build and program an application to your EZ-BLE Module, you must first update the components used in the example project using the Component Update Tool. To access the Component Update Tool, left-click the warning icon that is present in the lower right corner of PSoC Creator, as shown in Figure 25.

Figure 25. Component Update Tool Warning Icon Location

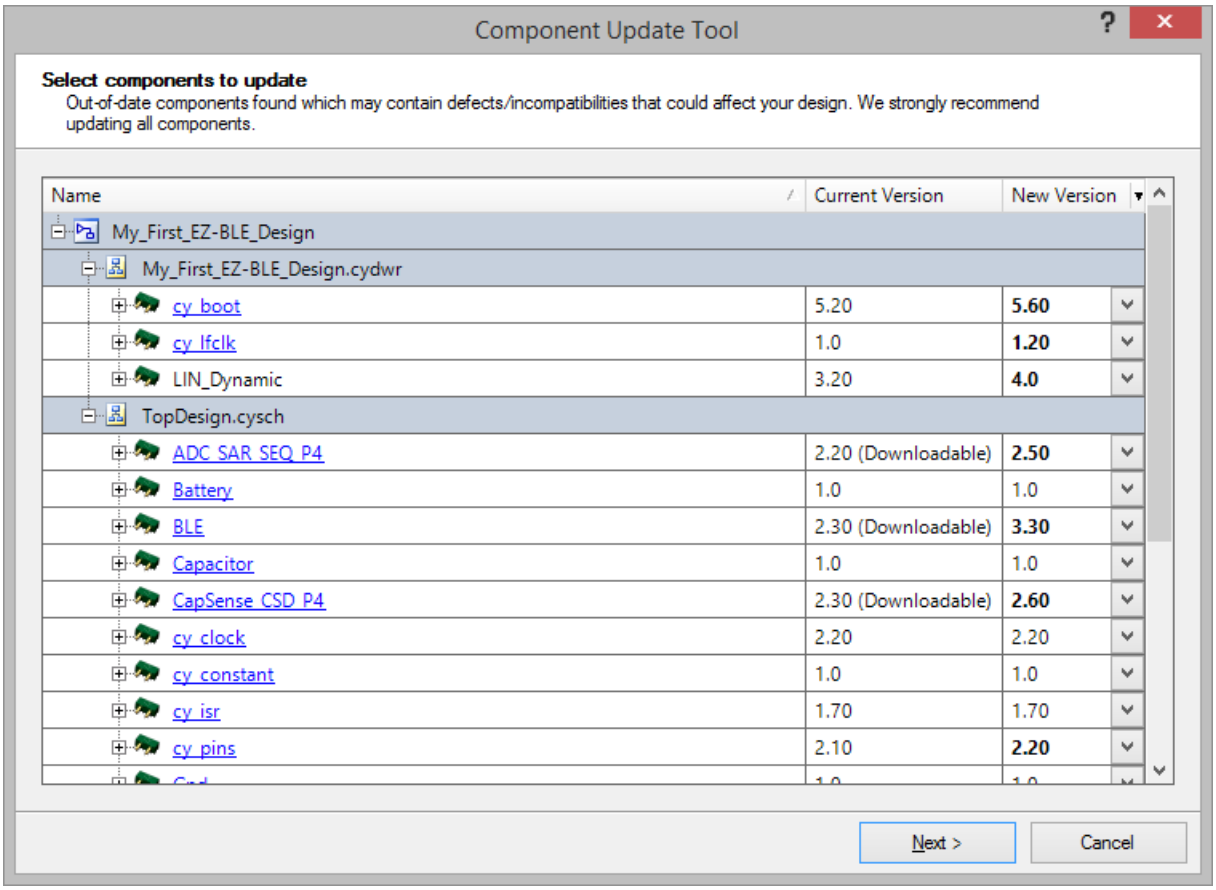
4. Before the Component Update Tool opens, you will be prompted if you wish to save your any unsaved documents before proceeding, as shown in Figure 26. Select **Yes** to proceed with the component update or **No** to exit the update, or click **Show Details** for more information. The Component Update Tool will not perform updates on unsaved documents.

Figure 26. Prompt for Saving Documents Prior to Component Update



5. After selecting **Yes** in Figure 26, the Component Update Tool will prompt you to update any Components that are out of date. Figure 27 shows the Component Update Tool. Select **Next** to proceed to the next page of the component update.

Figure 27. Component Update Tool



6. After clicking **Next**, the Component Update Tool will preview the components that will be updated and provide the option to “Create workspace archive before updating.” Select the desired option and then click **Finish**. Figure 28 shows the Component Update Tool with the option to create a workspace archive before updating. After clicking **Finish**, you may proceed after the status window shown in Figure 29 is no longer present.

Figure 28. Review, Archive and Update Components

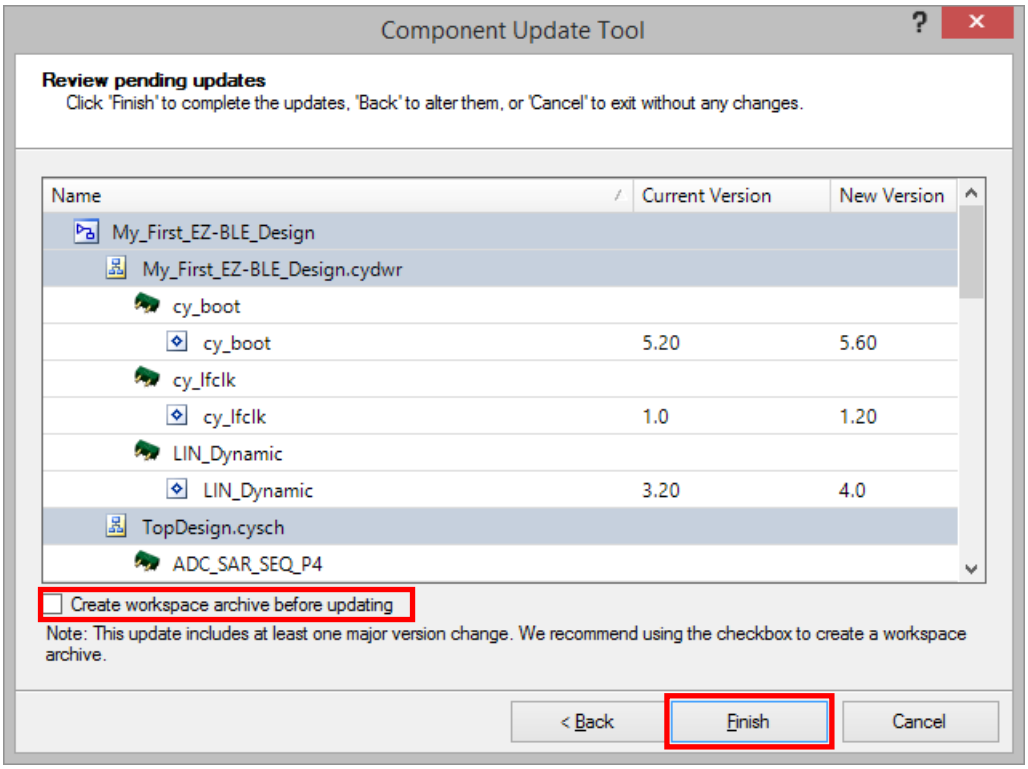
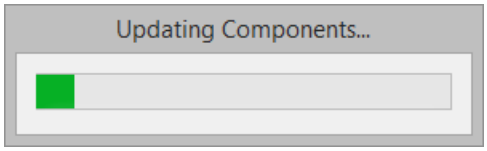
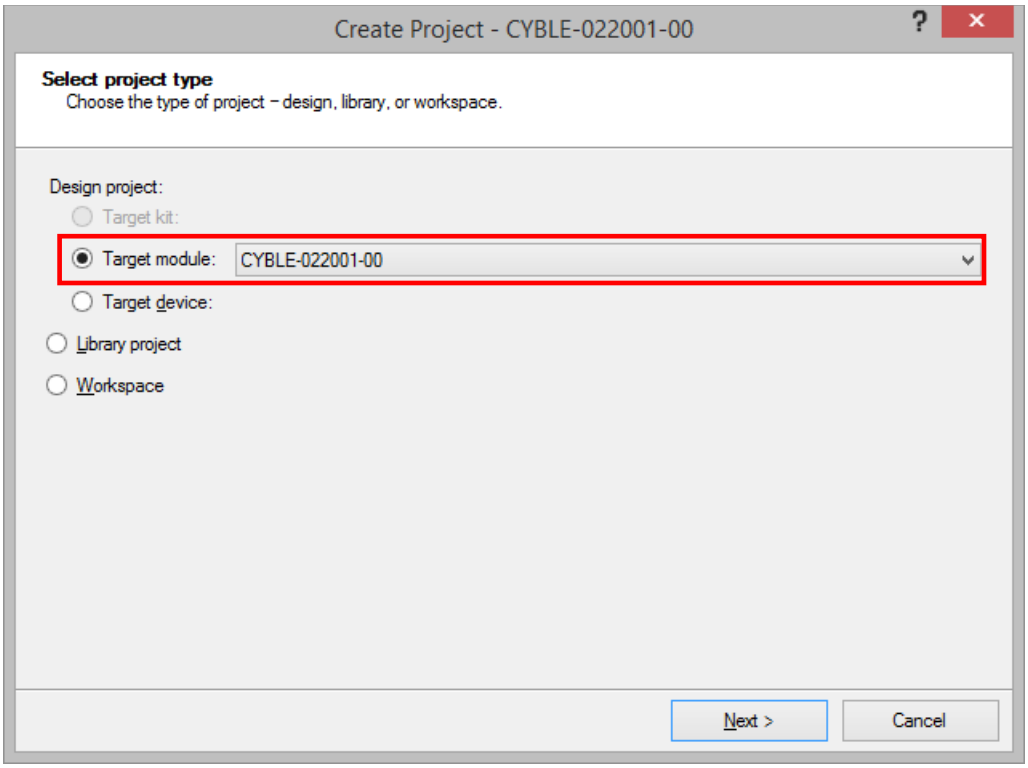


Figure 29. Component Update in Progress



7. Select the target module from the drop-down menu as "CYBLE-022001-00" as shown in Figure 30 and click **Next**. All EZ-BLE Modules are located under the “Target module” drop-down list. If you are using a custom EZ-BLE Module hardware or a different EZ-BLE part number, choose the "Launch Device Selector" option in Target device and select the appropriate part number.

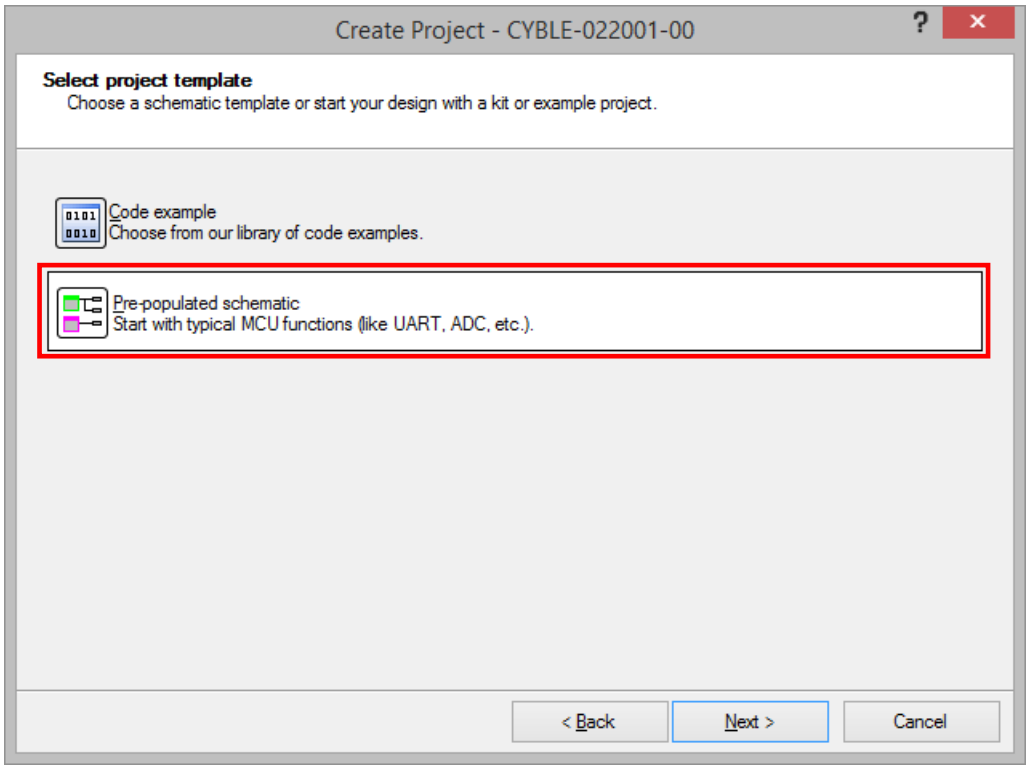
Figure 30. Selecting the Target Module



8. Select the “Pre-populated schematic” project template as shown in Figure 31 and click **Next**. In addition to the Pre-populated schematic project template, you can alternatively begin from a Code example project.

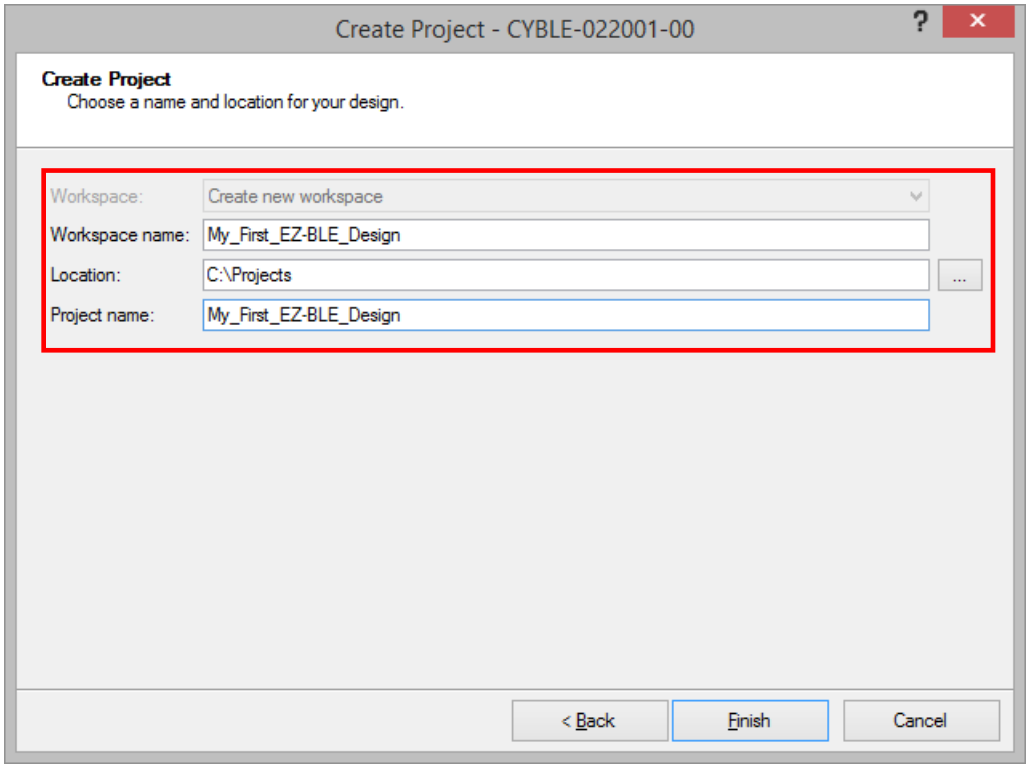
   Note: EZ-BLE PSoC Modules provide the additional option to start with an Empty Schematic project template.

Figure 31. Selecting the Project Template



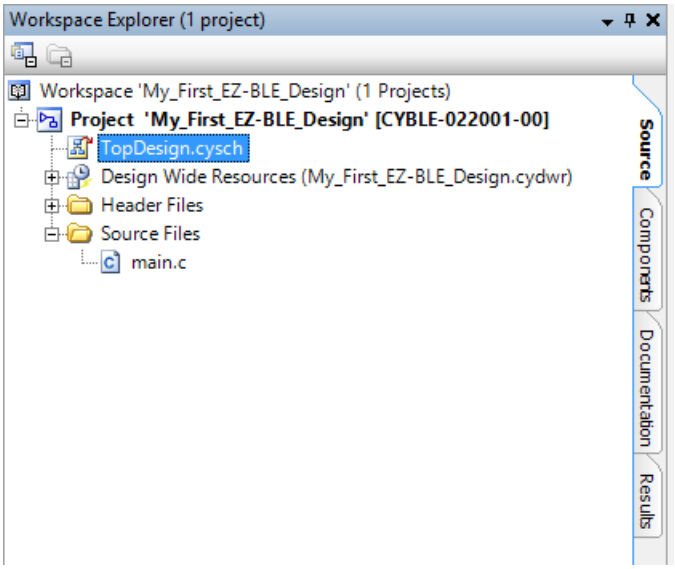
9. Give the workspace and the project a name such as “My_First_EZ-BLE_Design,” as Figure 32 shows. Choose an appropriate location for your new project, and then click **Finish**.

Figure 32. Naming the New Project



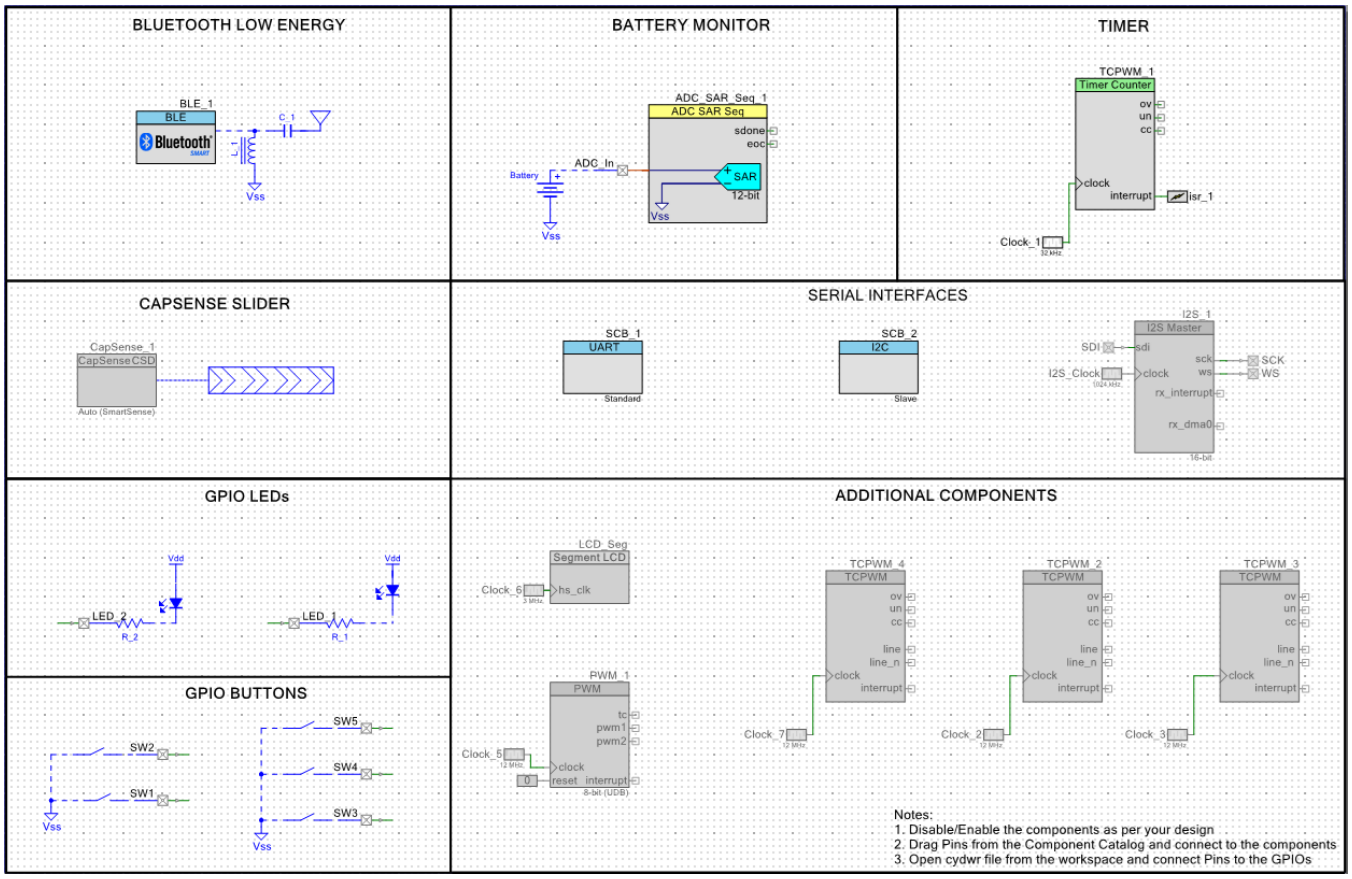
10. Creating a new project generates a project folder with a baseline set of files. You can view these files in the **Workspace Explorer** window, as Figure 33 shows. Open the project schematic file *TopDesign.cysch* by double-clicking it.

Figure 33. Opening TopDesign Schematic



11. You can see pre-populated Components in the schematic as Figure 34 shows.

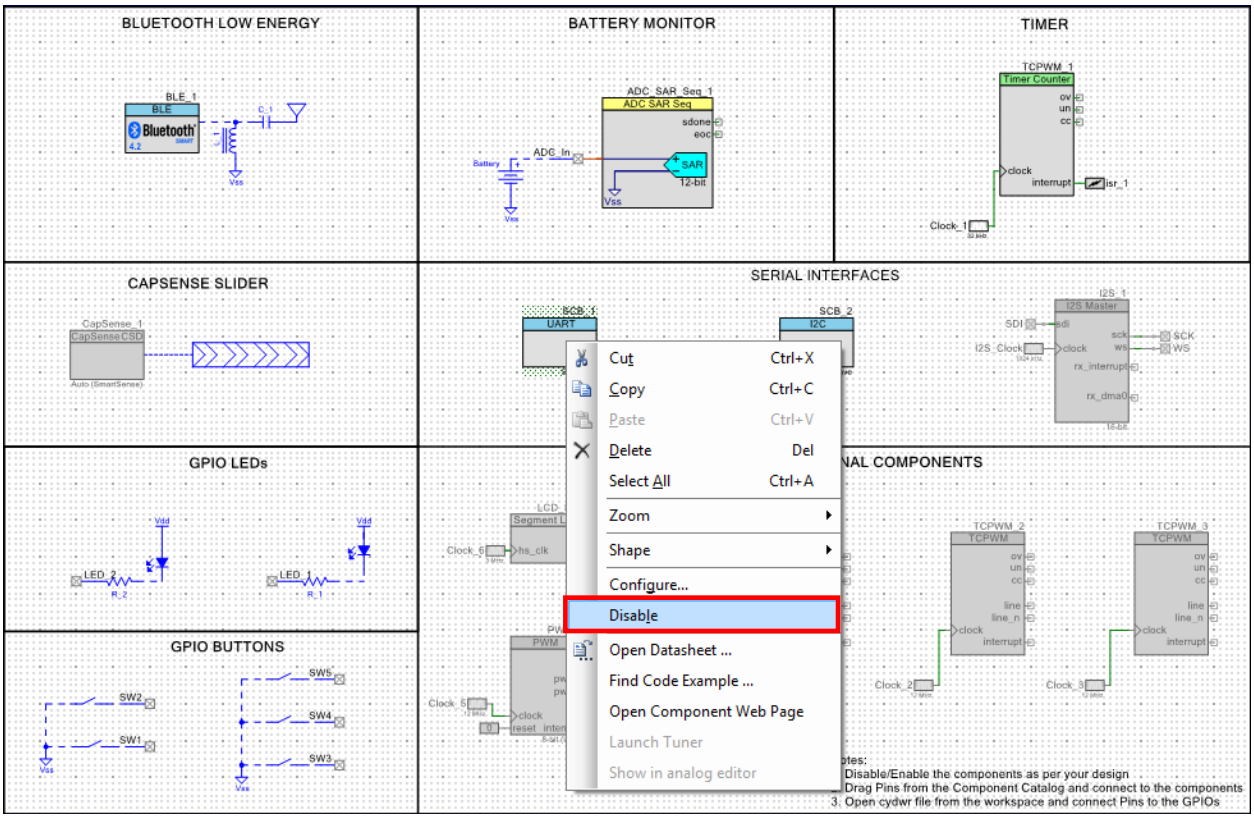
Figure 34. Pre-populated Components



12. Disable/enable the Components per your design. For this design, right-click on each of the Components as follows and enable/disable Components/features as Figure 35 shows:

- In the BATTERY MONITOR section, disable the ADC_SAR_Seq_1 and pin ADC_In
- In the GPIO BUTTONS section, disable all switches (SW1 through SW5)
- In the TIMER section, disable TCPWM_1, Clock_1, and ISR_1
- In the SERIAL INTERFACES section disable SCB_1 and SCB_2 (I2S_1 should already be disabled)

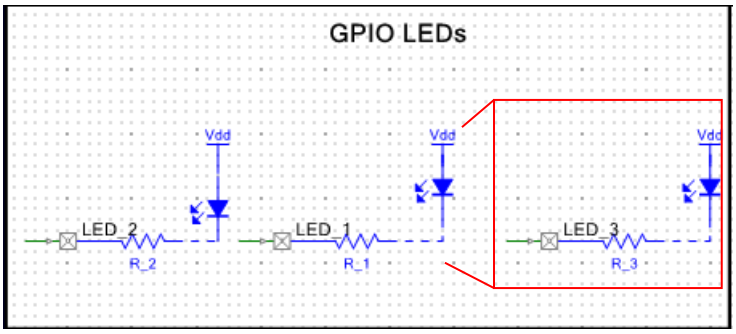
Figure 35. Enable/Disable Components



An alternative to disabling the Components is to delete the unused Components. Deleted Components can be replaced from the Component Catalog if required.

13. Add one more LED by selecting the following schematic and right-clicking **Copy** and **Paste** as shown in Figure 36. The new LED is automatically named “LED_3” in the schematic view. You will need to move the existing Components first in order to have enough space in the schematic. You can move selected Components by holding the left mouse button and dragging or by using the arrow keys.

Figure 36. Adding One More LED



14. Double-click the BLE Component on the schematic to configure it as a “BLE Find Me Target” with the following properties:
    - GAP Peripheral role with Find Me Target (GATT server) configuration
    - GAP Device Name set to “Find Me Target” and Appearance set to “Generic Keyring.” This configures the device name and type that appears when another device attempts to discover your device.

- General mode with an advertising timeout of 30 seconds and a fast advertisement interval of 20 to 30 ms. Fast advertising allows quick discovery and connection but consumes more power due to increased RF advertisement packets.
- Advertisement Packet with Immediate Alert Service enabled and Scan Response Packet with Local Name, Tx Power Level, and Appearance fields enabled.
- GAP security set to the lowest possible configuration that does not require authentication, encryption, or authorization for data exchange (Mode 1, No Security)

Figure 37 to Figure 43 show the BLE Component screenshots for this configuration.

Note: You do not need to change the default configuration of the BLE Component in the **Profiles** tab for this design.

Figure 37. BLE Component General Configuration

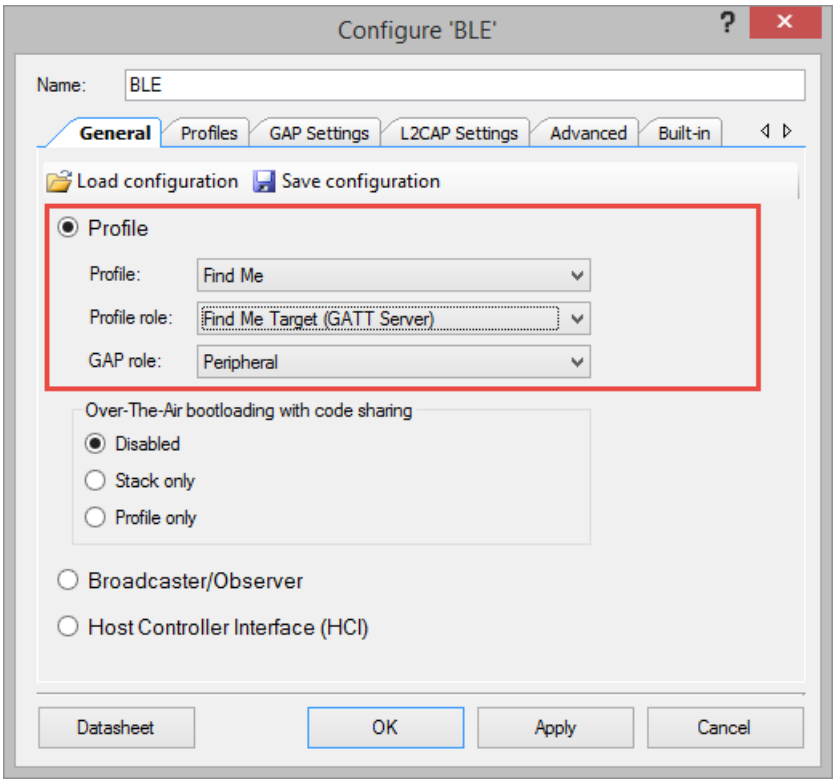


Figure 38. BLE Component GAP General Settings

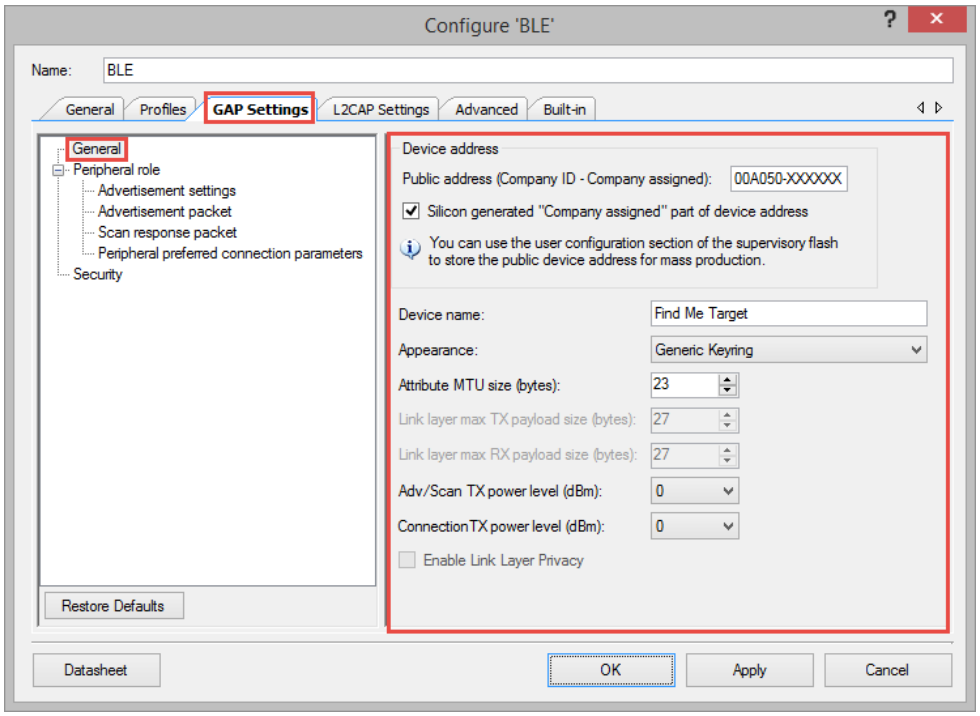


Figure 39. BLE Component GAP Advertisement Settings

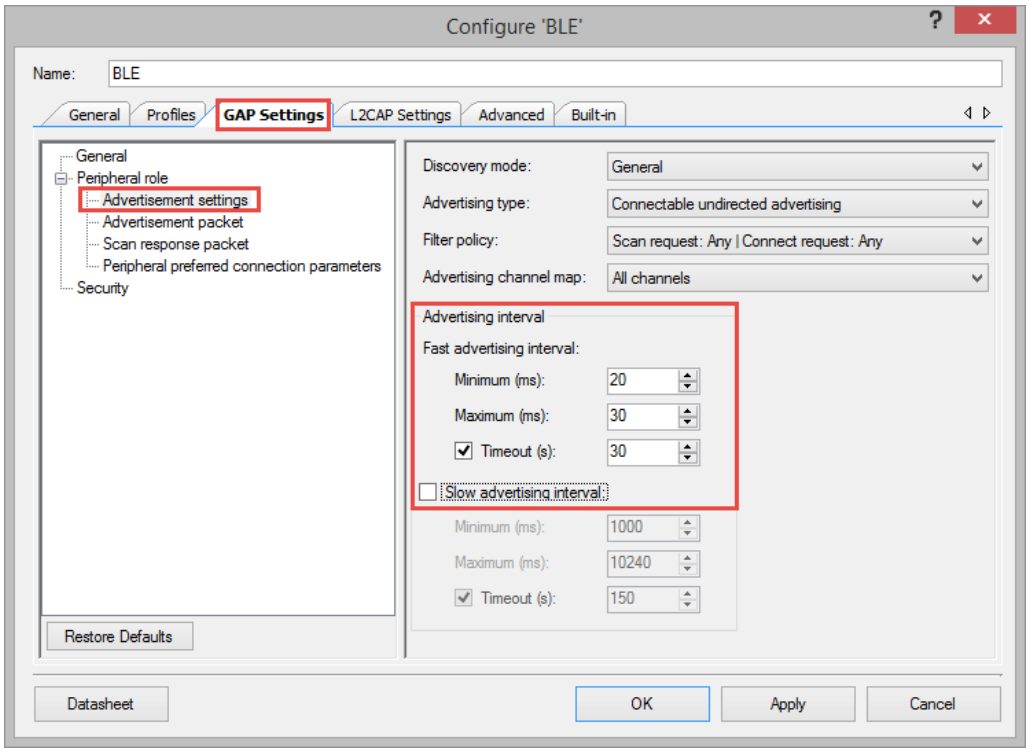


Figure 40. BLE Component GAP Advertisement Packet

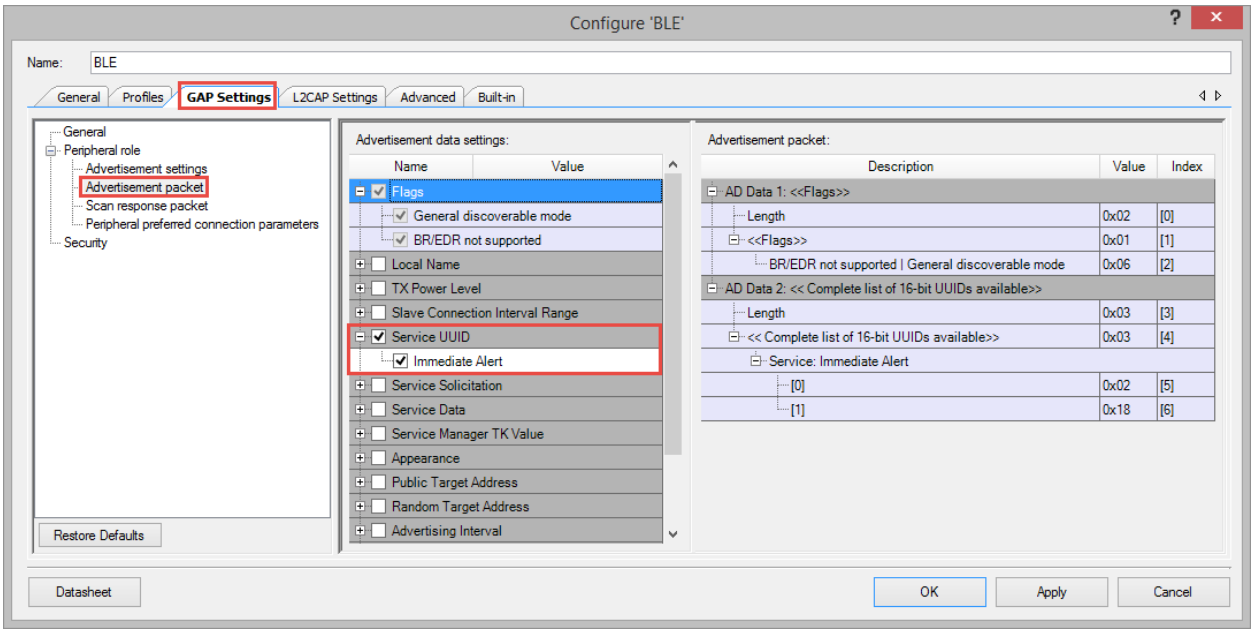


Figure 41. BLE Component GAP Scan Response Packet

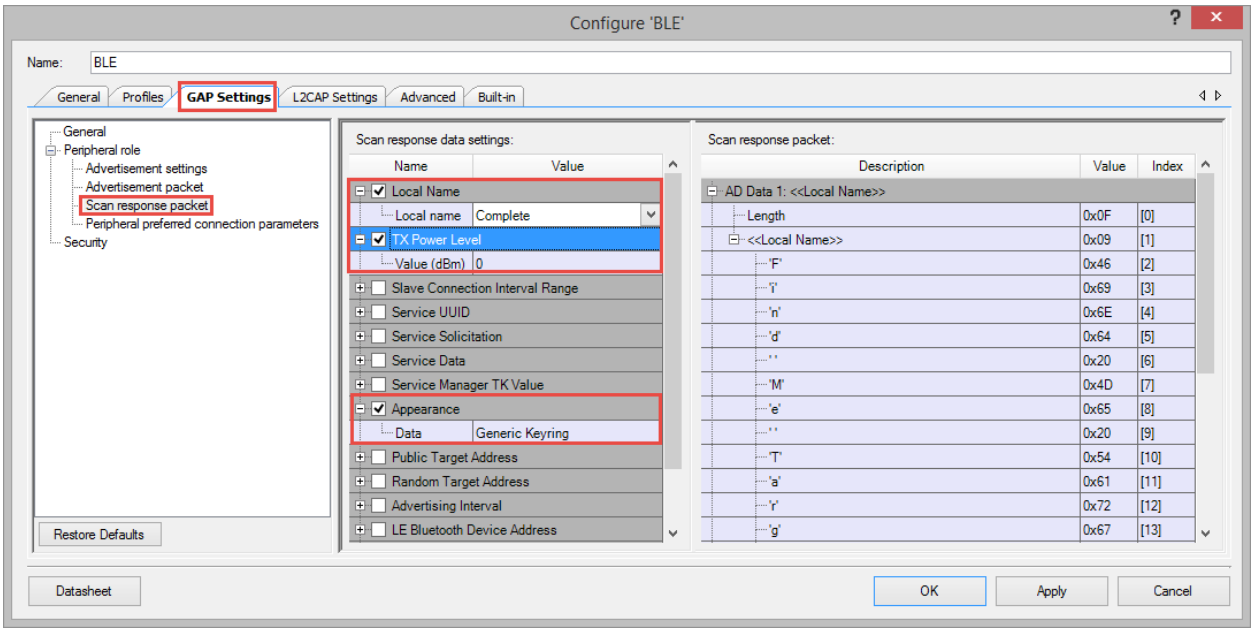


Figure 42. BLE Component GAP Security Settings

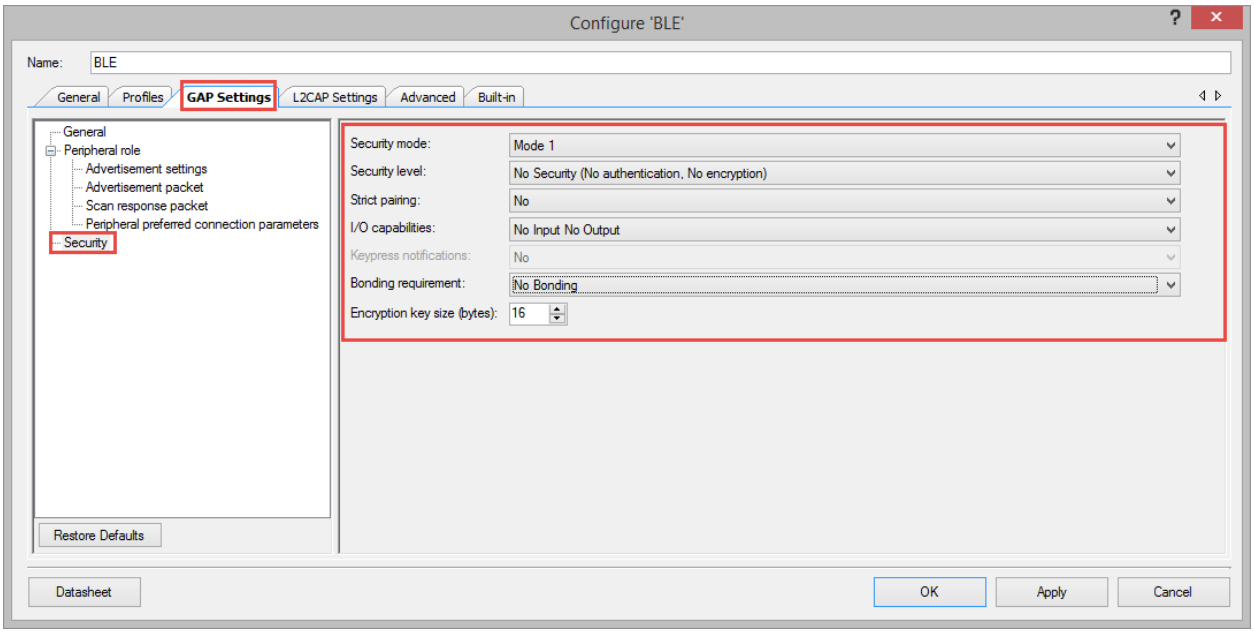
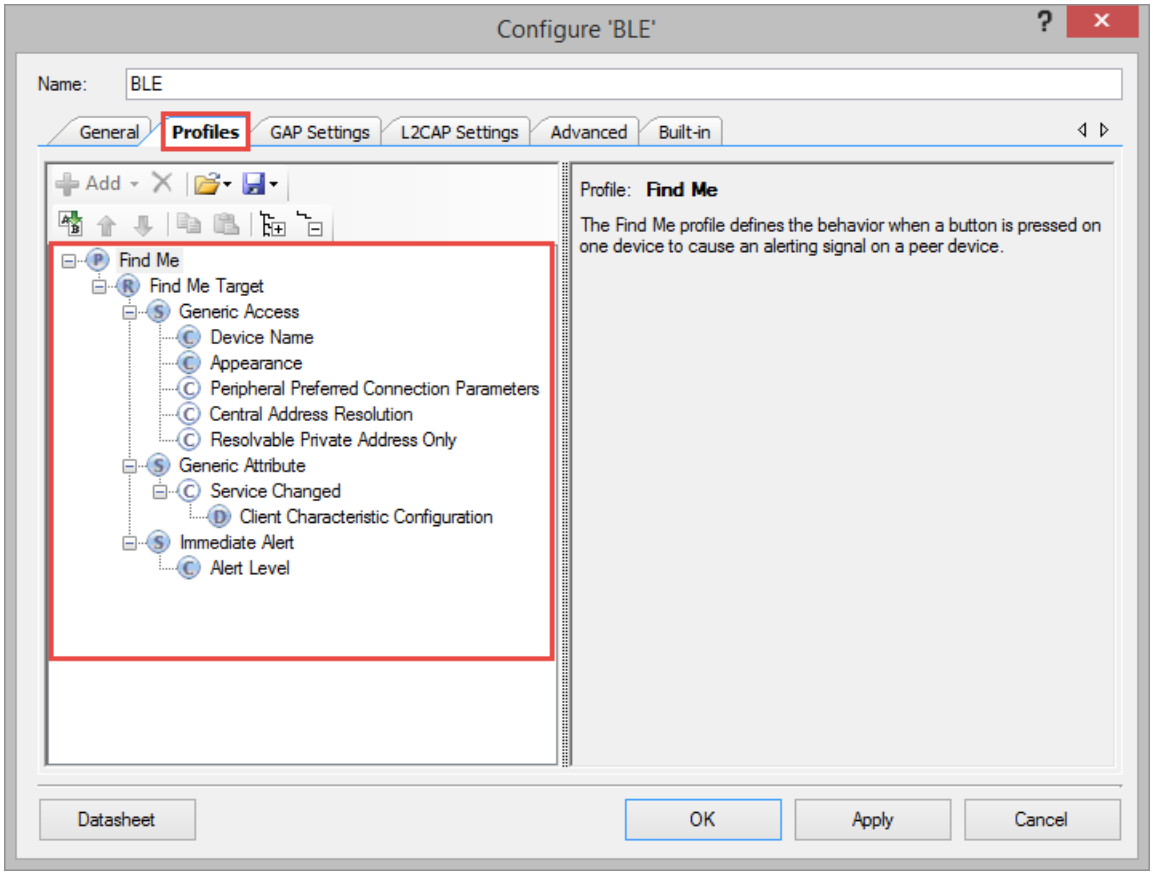
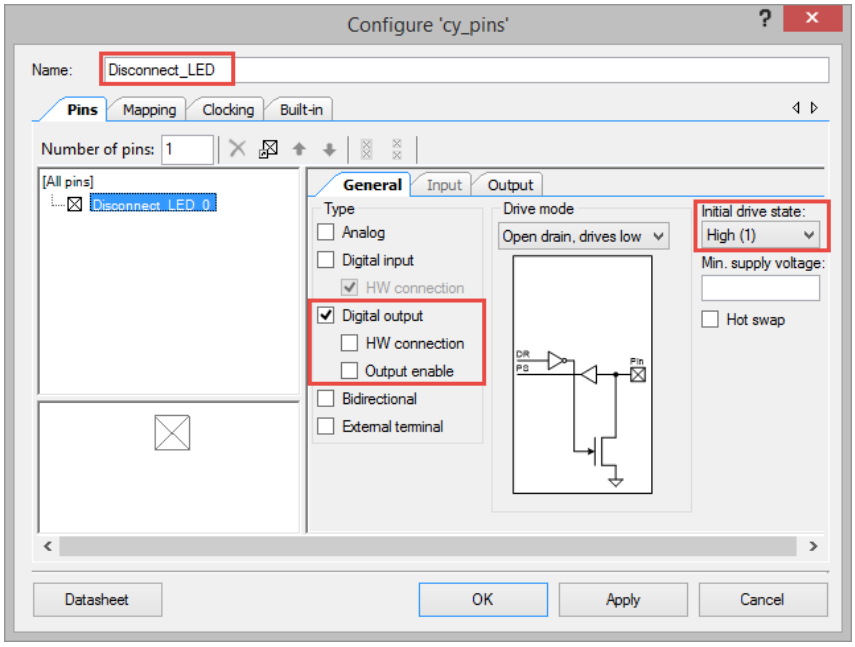


Figure 43. BLE Component Profiles Configuration



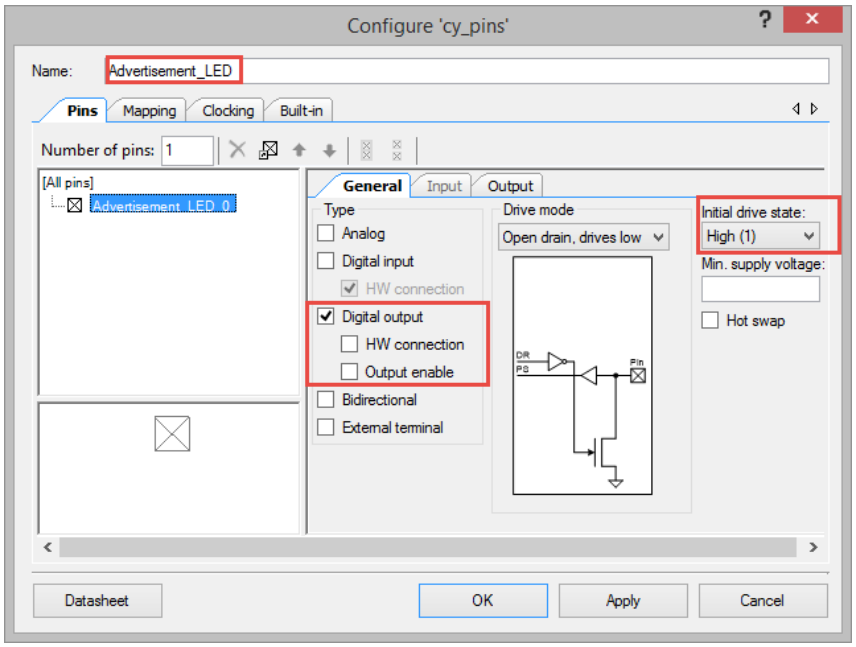
15. Rename the LEDs (LED_1, LED_2, and LED_3) as shown in steps 13 through 15.
16. Double-click LED_1 and rename it as “Disconnect_LED” as shown in Figure 44.

Figure 44. Disconnection LED Configuration



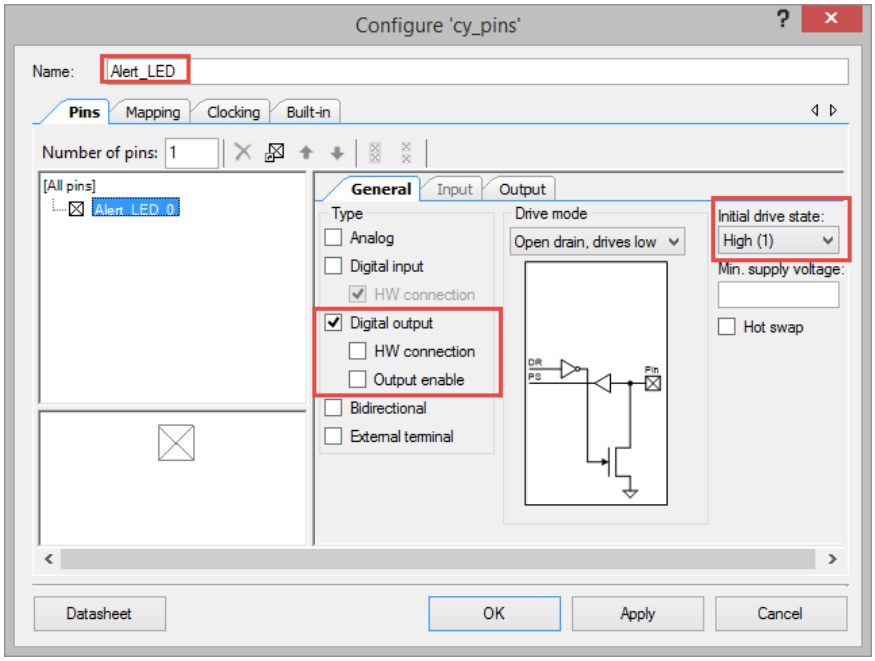
17. Double-click LED_2 and rename is as “Advertising_LED” with **HW Connection** deselected and **Initial drive state** set to “High(1),” as shown in Figure 45. These pins will be used to drive the BLE advertising and disconnection state indicator LEDs. The LEDs on the BLE Pioneer Kit are active LOW; that is, the high pin-drive state turns off the LEDs and the low pin-drive state turns them on.

Figure 45. Advertising LED Configuration



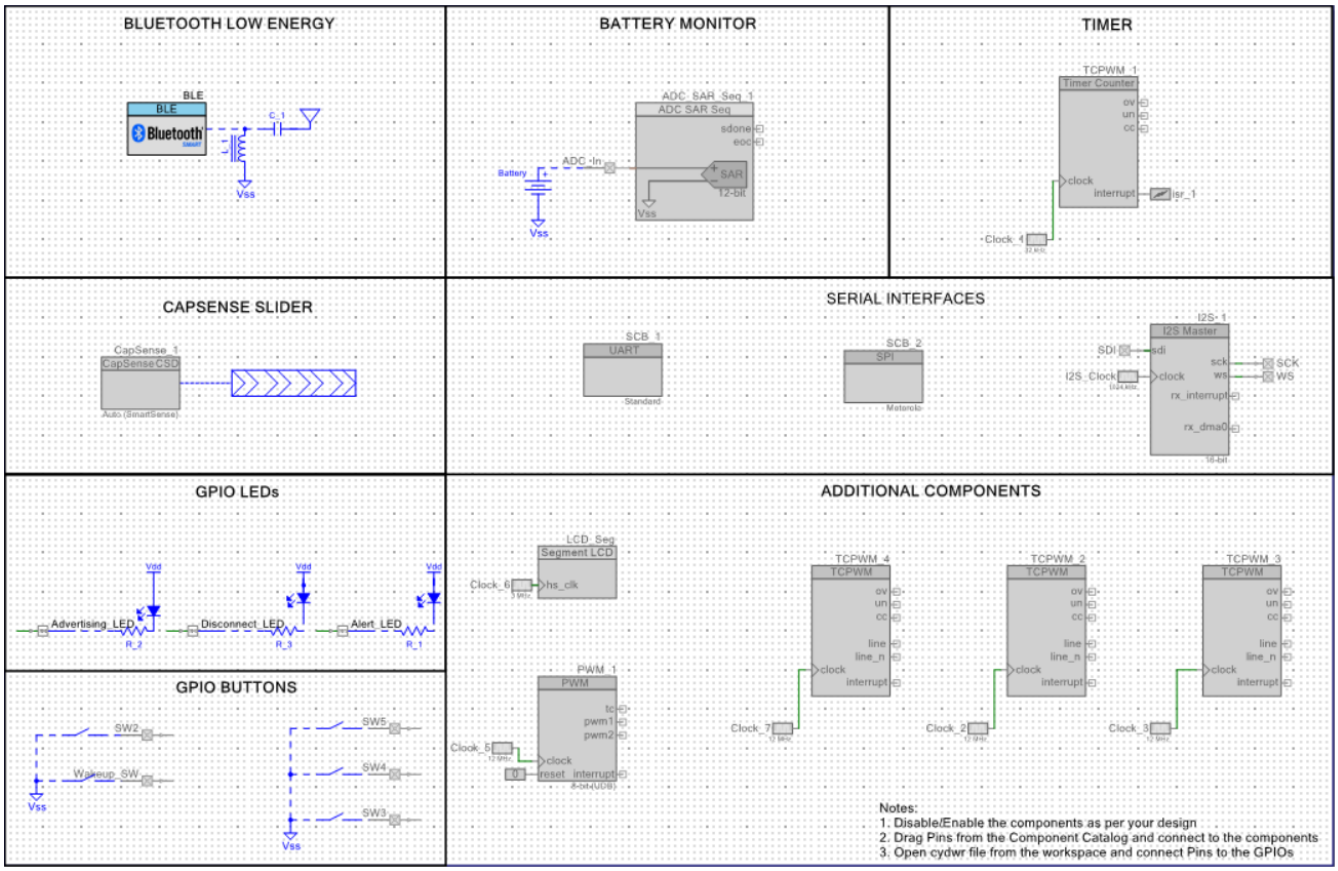
18. Double-click LED_3 and rename it as “Alert_LED” with **HW Connection** deselected and **Initial drive state** set to “High(1),” as shown in Figure 46.

Figure 46. Alert LED Configuration



19. After completing the schematic configuration, your design should look similar to Figure 47.

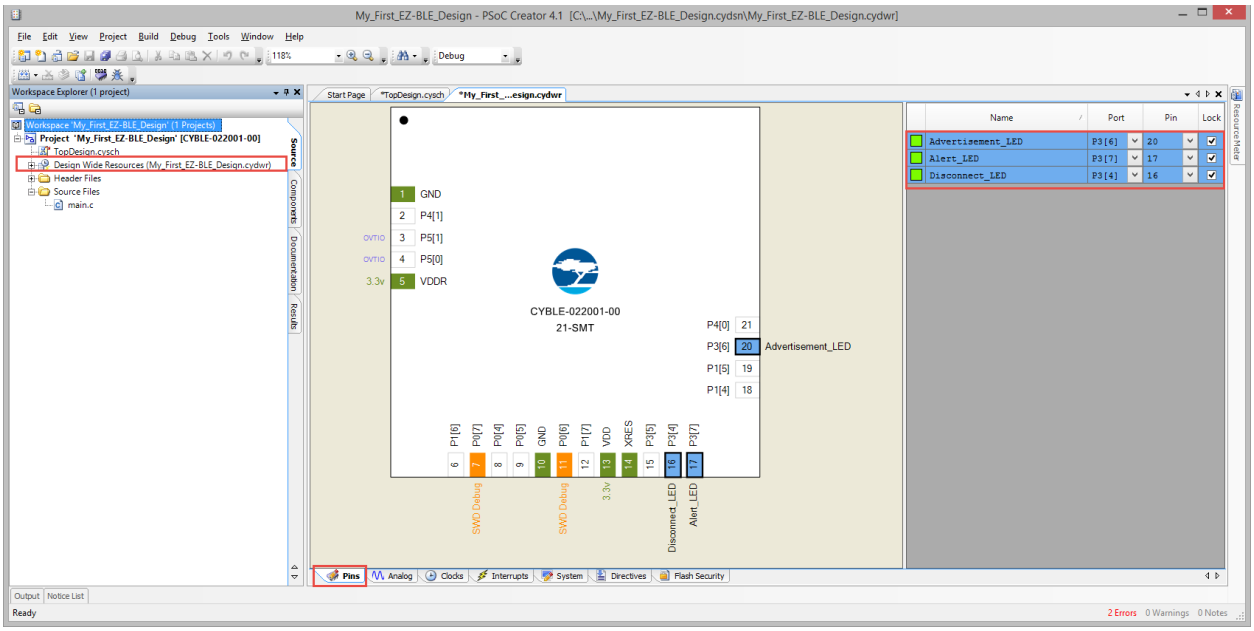
Figure 47. Schematic Configuration



Note: The blue dotted lines, the LED symbols, and resistor symbols shown in Figure 47 are off-chip PSoC Creator Components that are present only for descriptive purposes and are not required for the functioning of your design. You can add off-chip Components to your design by dragging and dropping the required off-chip Components on to your project schematic page from PSoC Creator's off-chip Component Catalog.

20. Open the file *My_First_EZ-BLE_Design.cydwr* (Design-Wide Resources) file from **Workspace Explorer** and click the **Pins** tab. You can use this tab to select the device pins for the outputs (Advertising_LED, Disconnect_LED, and Alert_LED). Figure 48 shows the pin configuration to connect the Advertising_LED, Disconnect LED, and Alert_LED pins to the green LED, red LED, and blue LED on the BLE Pioneer Kit respectively.

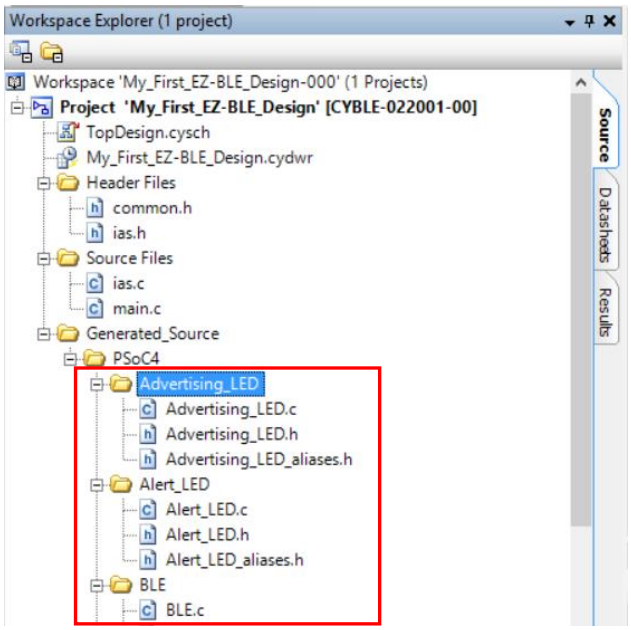
Figure 48. Pin Selection



If you are using your own board or a development kit with no LEDs, select the appropriate pins. You can connect external LEDs to the selected pins, as Figure 22 shows.

21. Select **Generate Application** from the **Build** menu. Notice in the **Workspace Explorer** window that PSoC Creator automatically generates source code files for the BLE and Digital Output Pin Components, as Figure 49 shows.

Figure 49. Generated Source Files



9.4 Part 2: Write the Firmware

Four main firmware blocks are required for designing BLE standard Profile applications using PSoC Creator:

- System initialization
- BLE stack event handler
- BLE service-specific event handler
- Main loop and low-power implementation

The following sections discuss these blocks with respect to the design that you configured in Part 1: Configure the Design.

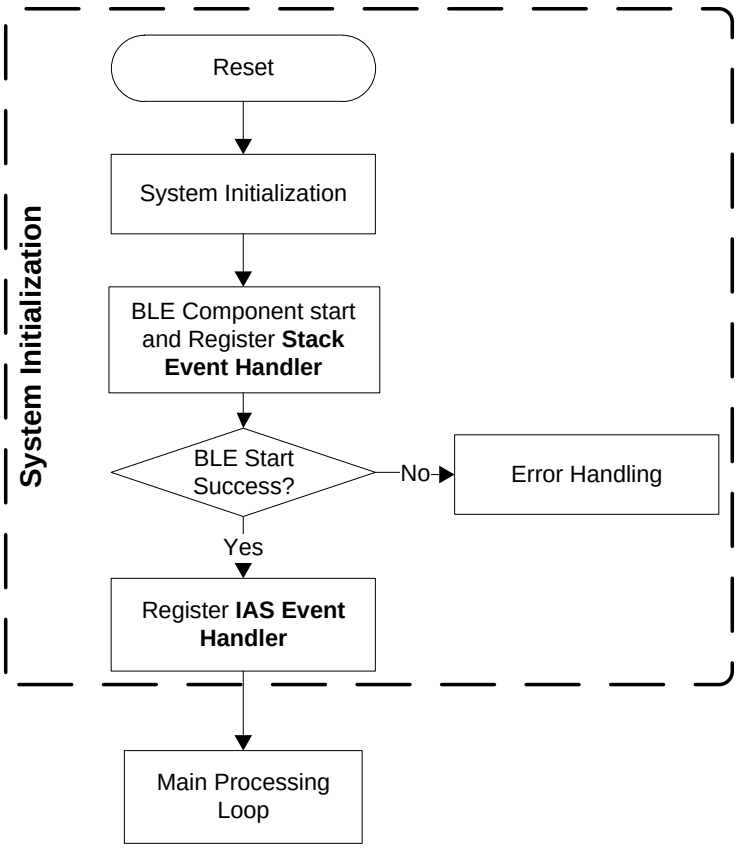
9.4.1 System Initialization

When the EZ-BLE PRoC Module is reset, the firmware first performs the system initialization, which includes enabling global interrupts and enabling other Components used in the design. After the system is initialized, the firmware initializes the BLE Component, which internally initializes the complete BLE subsystem.

As a part of the BLE Component initialization, you must pass the event-handler function, which will be called by the BLE stack to notify pending events. The BLE stack event handler shown in Code 2 is registered as a part of the BLE initialization. If the BLE Component initializes successfully, the firmware registers another event handler for the IAS-specific events and switches control to the main loop.

Figure 50 and Code 1 show the flow chart and the firmware source code for system initialization. Note that in Code 1, the trim value for the 24-MHz crystal oscillator integrated on the EZ-BLE PRoC Module is provided (shown in the red box in Code 1). This value provides optimal crystal performance for the CYBLE-022001-00 EZ-BLE PRoC Module. It is not recommended to change this value. For the optimal trim value for other EZ-BLE Modules, see the module datasheet. Refer to the datasheet to verify the appropriate trim value for your EZ-BLE Module.

Figure 50. System Initialization Flow Chart



Code 1. System Initialization Firmware

```
#include <Project.h>

#define LED_ON                  (0u)
#define LED_OFF                 (1u)

#define NO_ALERT                (0u)
#define MILD_ALERT              (1u)
#define HIGH_ALERT              (2u)

#define LED_TOGGLE_TIMEOUT      (100u)

#define CAPACITOR_TRIM_VALUE    0x00009898

uint8 alertLevel;

int main()
{
  CYBLE_API_RESULT_T apiResult;

  CyGlobalIntEnable;

  apiResult = CyBle_Start(StackEventHandler);

  if(apiResult != CYBLE_ERROR_OK)
  {
    /* BLE stack initialization failed, check your configuration */
    CYASSERT(0);
  }

  CyBle_IasRegisterAttrCallback(IasEventHandler);
}
```

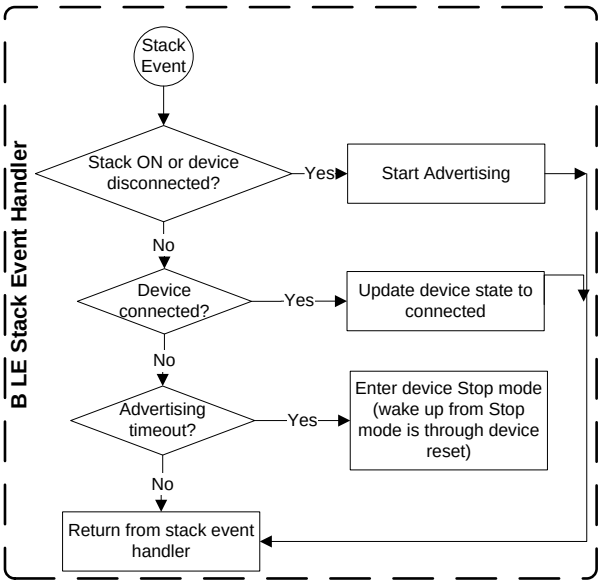
9.4.2 BLE Stack Event Handler

The BLE stack within the BLE Component generates events to provide the BLE interface status and data to the application firmware through the BLE stack event handler registered by you. The event handler must handle a few basic events from the stack, such as device connection and stack on, and configure the stack accordingly to establish and maintain the BLE link. For the Find Me Target application that you are creating, the BLE stack event handler must process all the events described in Table 5. The flow chart and the firmware for handling BLE stack events are shown in Figure 51 and Code 2.

Table 5. BLE Stack Events

BLE Stack Event Name	Event Description	Event Handler Action
CYBLE_EVT_STACK_ON	BLE stack initialization completed successfully.	Start advertisement and reflect the advertisement state on the LED.
CYBLE_EVT_GAP_DEVICE_DISCONNECTED	BLE link with the peer device is disconnected.	Restart advertisement and reflect the advertisement state on the LED.
CYBLE_EVT_GAP_DEVICE_CONNECTED	BLE link with the peer device is established.	Update the BLE link state on the LED.
CYBLE_EVT_GAPP_ADVERTISEMENT_START_STOP	BLE stack advertisement start/stop event.	Configure the device in Stop mode if the advertisement has timed out.

Figure 51. BLE Stack Event Handler Flow Chart



Code 2. BLE Stack Event Handler Firmware

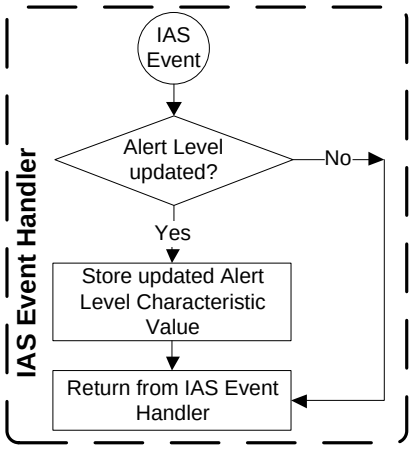
```
void StackEventHandler(uint32 event, void *eventParam)
{

        CYBLE_BLESS_CLK_CFG_PARAMS_T clockConfig;

    switch(event)
    {
        /* Mandatory events to be handled by Find Me Target design */
        case CYBLE_EVT_STACK_ON:
            /* load capacitors on the ECO should be tuned and the tuned value
            * must be set in the CY_SYS_XTAL_BLERD_BB_XO_CAPTRIM_REG  */

            CY_SYS_XTAL_BLERD_BB_XO_CAPTRIM_REG = CAPACITOR_TRIM_VALUE;

            /* Get the configured clock parameters for BLE sub-system */

           CyBle_GetBleClockCfgParam(&clockConfig);

        case CYBLE_EVT_GAP_DEVICE_DISCONNECTED:
            /* Start BLE advertisement for 30 seconds and update link
             * status on LEDs */
            CyBle_GappStartAdvertisement(CYBLE_ADVERTISING_FAST);
            Advertising_LED_Write(LED_ON);
            alertLevel = NO_ALERT;
        break;

        case CYBLE_EVT_GAP_DEVICE_CONNECTED:
            /* BLE link is established */
            Advertising_LED_Write(LED_OFF);
            Disconnect_LED_Write(LED_OFF);
        break;
```

```
        case CYBLE_EVT_GAPP_ADVERTISEMENT_START_STOP:
            if(CyBle_GetState() == CYBLE_STATE_DISCONNECTED)
            {
                /* Advertisement event timed out, go to low power
                 * mode (Stop mode) and wait for device reset
                 * event to wake up the device again */
                Advertising_LED_Write(LED_OFF);
                Disconnect_LED_Write(LED_ON);
                CySysPmSetWakeupPolarity(CY_PM_STOP_WAKEUP_ACTIVE_HIGH);
                CySysPmStop();

                /* Code execution will not reach here */
            }
        break;

        default:
        break;
    }
}
```

9.4.3 BLE Service-Specific Event Handler

The BLE Component also generates events corresponding to each of the Services supported by your design. For the Find Me Target application that you are creating, the BLE Component will generate IAS events that will let the application know if the Alert Level Characteristic is updated with a new value. The flow chart and the firmware for handling BLE IAS events are shown in Figure 52 and Code 3 respectively.

Figure 52. BLE IAS Event Handler Flow Chart



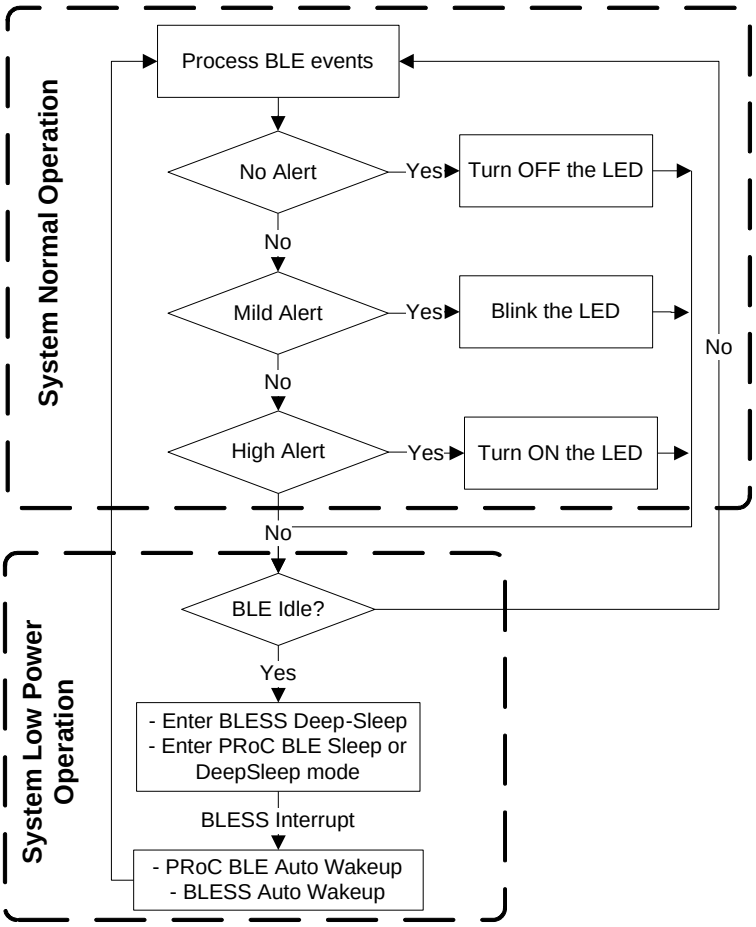
Code 3. BLE IAS Event Handler Firmware

```
void IasEventHandler(uint32 event, void *eventParam)
{
    /* Alert Level Characteristic write event */
    if(event == CYBLE_EVT_IASS_WRITE_CHAR_CMD)
    {
        /* Read the updated Alert Level value from the GATT database */
        CyBle_IassGetCharacteristicValue(CYBLE_IAS_ALERT_LEVEL,
            sizeof(alertLevel), &alertLevel);
    }
}
```

9.4.4 Main Loop and Low-Power Implementation

The main loop firmware in your design must periodically service the BLE stack-processing event, update the blue alert LED state per the IAS Alert Level Characteristic value, and configure the BLESS block and the EZ-BLE PRoC Module system into low-power mode between consecutive BLE advertisement and connection intervals. For more information on power management, see the application note AN92584. The main loop flow chart and the firmware are shown in Figure 53 and Code 4.

Figure 53. Firmware Main Loop Flow Chart



Code 4. Main Loop Firmware

```
for(;;)
{
    static uint8 toggleTimeout = 0;
    CYBLE_BLESS_STATE_T blessState;
    uint8 intrStatus;

    /* Single API call to service all the BLE stack events. Must be
     * called at least once in a BLE connection interval */
                                    CyBle_ProcessEvents();

    /* Update Alert Level value on the blue LED */
    switch(alertLevel)
    {
        case NO_ALERT:
```

```
            Alert_LED_Write(LED_OFF);
            break;

            case MILD_ALERT:
            toggleTimeout++;
            if(toggleTimeout == LED_TOGGLE_TIMEOUT)
            {
                /* Toggle alert LED after timeout */
                Alert_LED_Write(Alert_LED_Read() ^ 0x01);
                toggleTimeout = 0;
            }
            break;

            case HIGH_ALERT:
            Alert_LED_Write(LED_ON);
            break;
        }

        /* Configure BLESS in Deep-Sleep mode */
        CyBle_EnterLPM(CYBLE_BLESS_DEEPSLEEP);

        /* Prevent interrupts while entering system low power modes */
        intrStatus = CyEnterCriticalSection();

        /* Get the current state of BLESS block */
        blessState = CyBle_GetBleSsState();

        /* If BLESS is in Deep-Sleep mode or the XTAL oscillator is turning on,
         * then PRoC BLE can enter Deep-Sleep mode (1.3uA current consumption) */
        if(blessState == CYBLE_BLESS_STATE_ECO_ON ||
            blessState == CYBLE_BLESS_STATE_DEEPSLEEP)
        {
            CySysPmDeepSleep();
        }
        else if(blessState != CYBLE_BLESS_STATE_EVENT_CLOSE)
        {
            /* If BLESS is active, then configure PRoC BLE system in
             * Sleep mode (~1.6mA current consumption) */
            CySysPmSleep();
        }
        else
        {
            /* Keep trying to enter either Sleep or Deep-Sleep mode */
        }
        CyExitCriticalSection(intrStatus);

        /* BLE link layer timing interrupt will wake up the system from Sleep
         * and Deep-Sleep modes */
    }
```

After including the above code snippets in the correct order, go to **Build** > **Clean and Build** your project to compile the firmware. Appendix E details the complete *main.c* firmware.

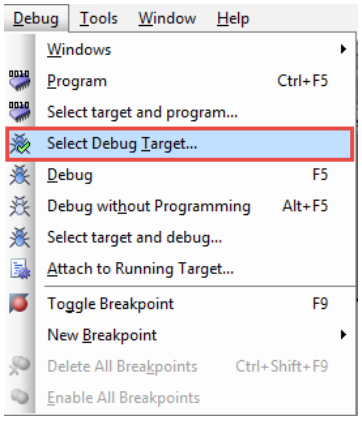
9.5 Part 3: Program the Device

This section shows how to program the EZ-BLE PRoC Module Evaluation Board. If you are using a development kit with a built-in programmer (the BLE Pioneer Kit, for example), connect the kit board to your computer using the USB cable. For other kits, see the kit guide.

Note: The source project for this design is located on the AN96841 web page.

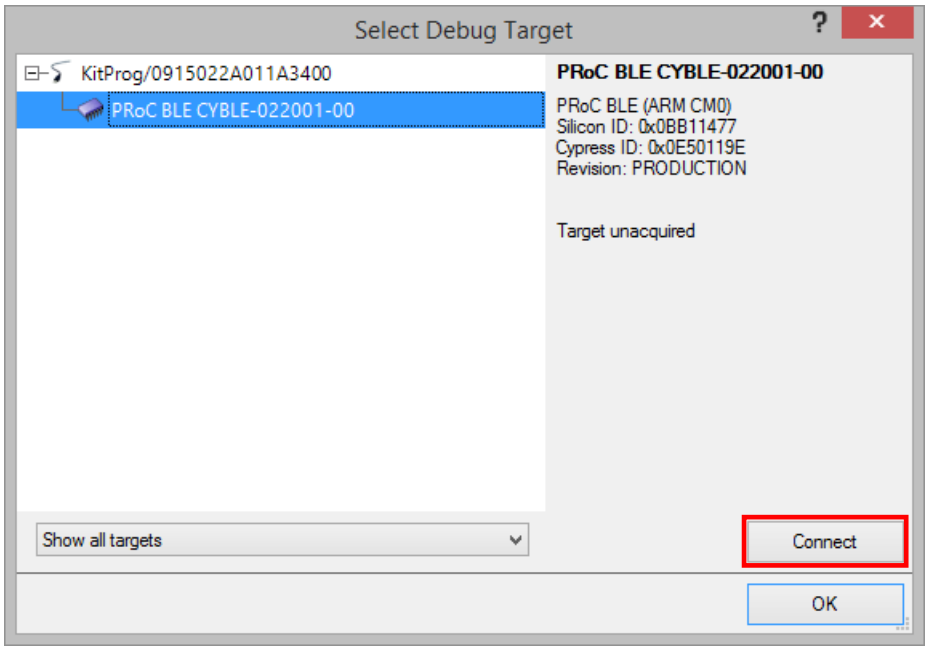
If you are developing on your own hardware, you need a hardware debugger; for example, a Cypress CY8CKIT–002 MiniProg3. In PSoC Creator, choose **Debug** > **Select Debug Target**, as Figure 54 shows.

Figure 54. Selecting Debug Target



1. In the **Select Debug Target** dialog box, click **Port Acquire**, and then click **Connect**, as Figure 55 shows. Click **OK** to close the dialog box.

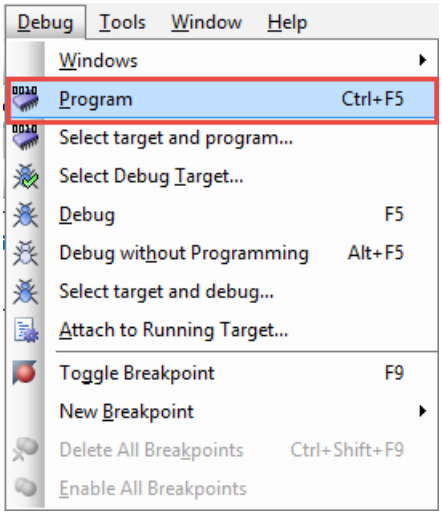
Figure 55. Connecting to a Device



If you are using your own hardware, make sure the **Port Setting** configuration in the **Select Debug Target** window for your programming hardware is configured per your setup.

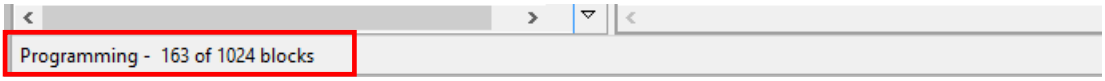
2. In PSoC Creator, choose **Debug** > **Program** to program the device with the project, as Figure 56 shows.

Figure 56. Programming the Device



3. You can view the programming status on the PSoC Creator status bar (lower left corner of the window), as Figure 57 shows.

Figure 57. Programming Status



9.6 Part 4: Test Your Design

This section describes how to test your BLE design using the CySmart mobile apps and PC tool. The setup for testing your design using the BLE Pioneer Kit is shown in Figure 12.

1. Turn on Bluetooth on your iOS or Android device.
2. Launch the CySmart app. Press the reset switch on the BLE Pioneer Kit to start BLE advertisements from your design.
3. Pull down the CySmart app home screen to start scanning for BLE Peripherals. Your device will now appear in the CySmart app home screen. Select your device to establish a BLE connection.
4. Select the “Find Me” Profile from the carousel view.
5. Select one of the Alert Level values on the Find Me **Profile** screen and observe the state of the LED on your device change per your selection.
6. A step-by-step configuration screenshot of the CySmart mobile app is shown in Figure 58 and Figure 59.

Figure 58. Testing with CySmart iOS App

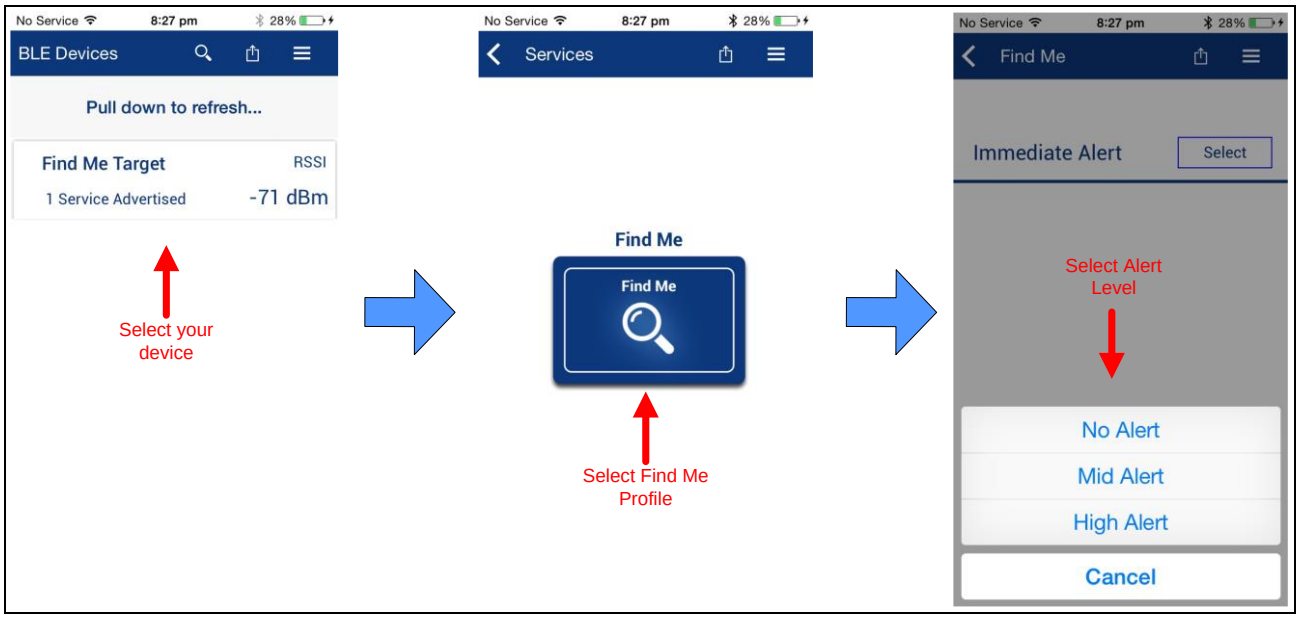
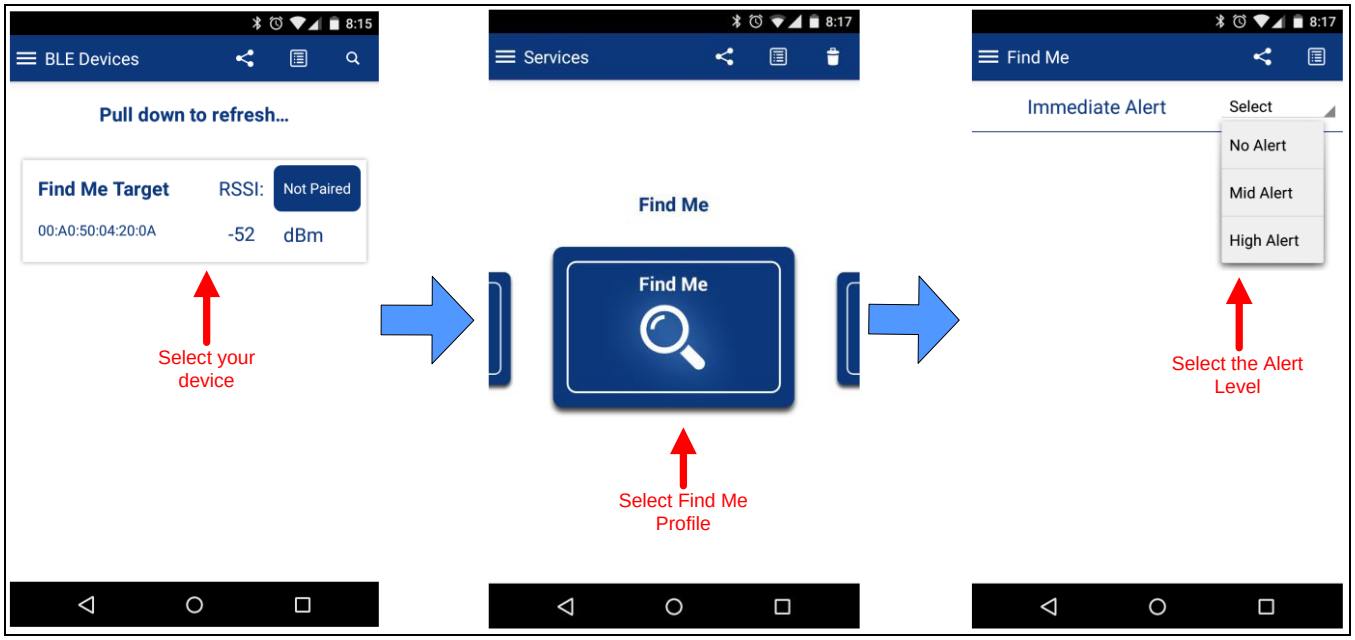


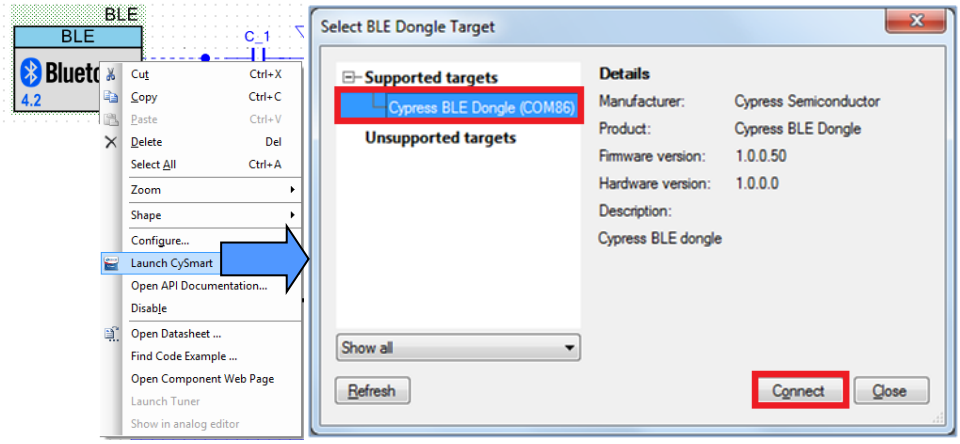
Figure 59. Testing with CySmart Android App



Similar to the CySmart mobile app, you can also use the CySmart Host Emulation Tool on a PC to establish a BLE connection with your design and perform read or write operations on BLE Characteristics.

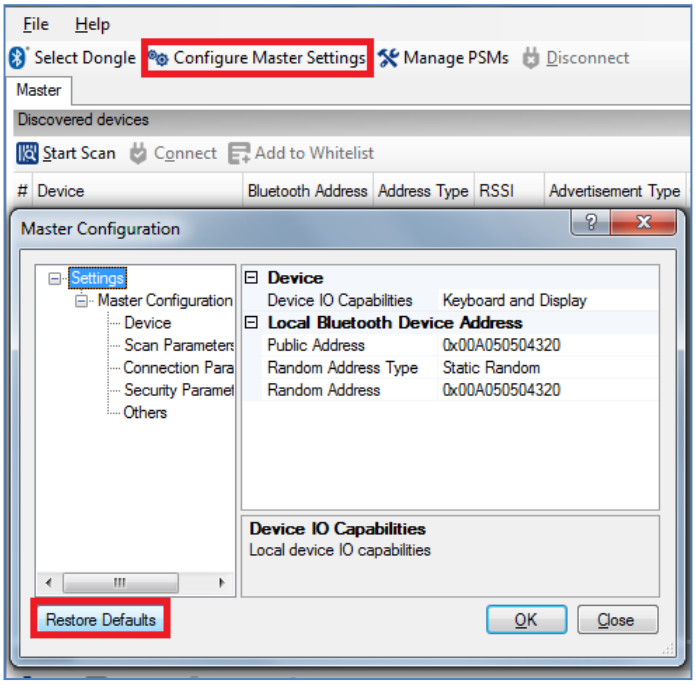
1. Connect the BLE Dongle to your Windows machine. Wait for the driver installation to complete.
2. Launch the CySmart Host Emulation Tool; it automatically detects the BLE Dongle. Click **Refresh** if the BLE Dongle does not appear in the **Select BLE Dongle Target** pop-up window. Click **Connect,** as shown in Figure 60.

Figure 60. CySmart BLE Dongle Selection



3. Select **Configure Master Settings** and restore the values to the default settings, as shown in Figure 61.

Figure 61. CySmart Master Settings Configuration

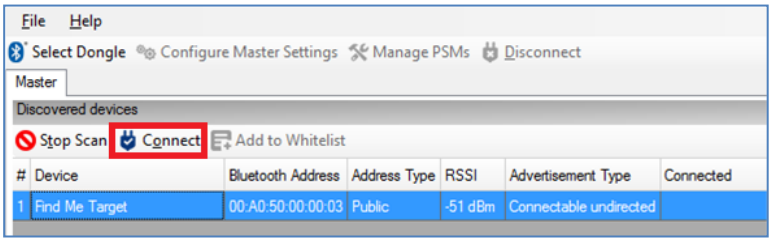


4. Press the reset switch on the BLE Pioneer Kit to start BLE advertisements from your design.
5. On the CySmart Host Emulation Tool, click **Start Scan**. Your device name should appear in the **Discovered devices** list, as shown in Figure 62.

Figure 62. CySmart Device Discovery

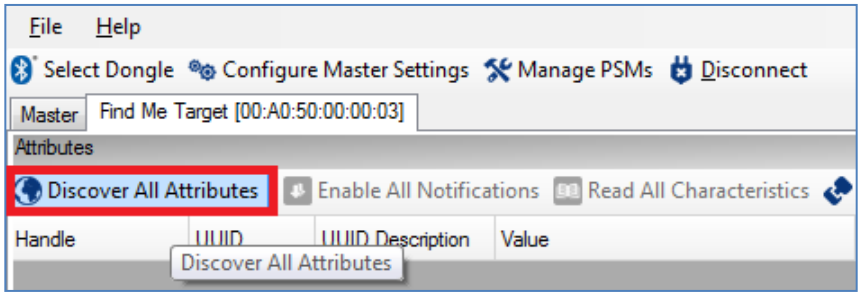
6. Select your device and click **Connect** to establish a BLE connection between the CySmart Host Emulation Tool and your device, as shown in Figure 63.

Figure 63. CySmart Device Connection



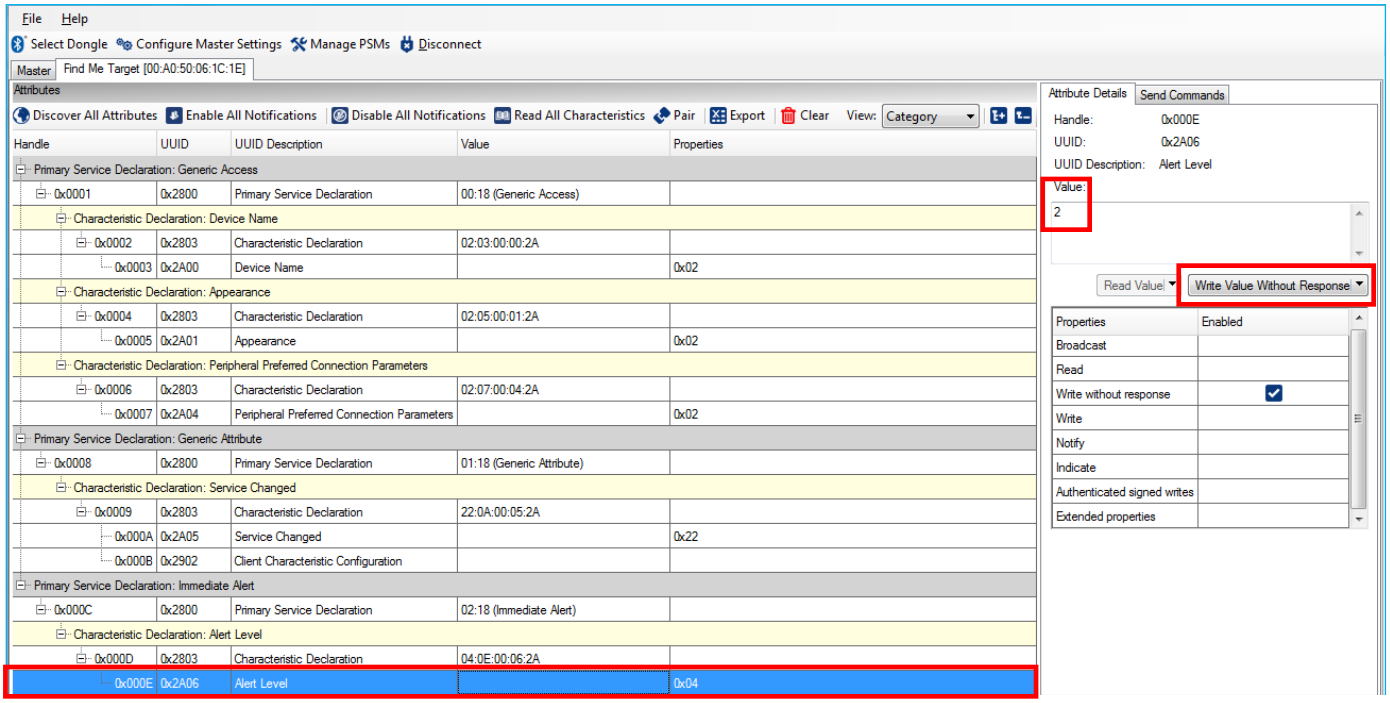
7. Once connected, discover all the Attributes on your design from the CySmart Host Emulation Tool, as shown in Figure 64.

Figure 64. CySmart Attribute Discovery



8. Write a value of 0, 1, or 2 to the Alert Level Characteristic under the Immediate Alert Service, as Figure 65 shows. Observe the state of the LED on your device change per your Alert Level Characteristic configuration.

Figure 65. Testing with CySmart Host Emulation Tool



9.7 Design Source

The functional PSoC Creator project for the BLE example design described in this application note is distributed on the application note web page. See the AN96841 web page to download this complete design.

This design uses GPIOs for three LEDs to indicate different states, a push button switch (SW1 Reset on CY8CKIT-042-BLE) for wake-up from Stop mode, and a BLE subsystem to enable the 'Find Me' profile through the BLE protocol. The schematic for the design from PSoC Creator is shown in Figure 47.

10 Learning Resources

This section provides a list of EZ-BLE Module learning resources that can help you to get started and develop complete applications with your EZ-BLE Module. You can also use the Document Manager in PSoC Creator to view these resources. To open the Document Manager, choose the **Help** > **Document Manager**.

10.1 EZ-BLE Module Datasheet

The EZ-BLE Module datasheets list the features, pinouts, device-level specifications, and fixed-function peripheral electrical specifications of the EZ-BLE Modules.

10.2 PRoC BLE Device Datasheet

PRoC BLE datasheets lists the features, pinouts, device-level specifications, and fixed-function peripheral electrical specifications of all PRoC BLE devices. The PRoC BLE device is available in 128-KB and 256-KB flash options. Datasheets for each of the PRoC BLE devices can be found at the below links:

- PRoC BLE 128-KB Flash device datasheet
- PRoC BLE 256-KB Flash BT 4.1/4.2 device datasheet

10.3 PSoC 4 BLE Device Datasheet

PSoC 4 BLE datasheets lists the features, pinouts, device-level specifications, and fixed-function peripheral electrical specifications of all PSoC 4 BLE devices. The PSoC 4 BLE device is available in 128-KB and 256-KB flash options. Datasheets for each of the PSoC 4 BLE devices can be found at the below links:

- PSoC 4 BLE 128-KB Flash device datasheet
- PSoC 4 BLE 256-KB Flash devices: BT 4.1 datasheet; BT 4.2 datasheet

10.4 PRoC BLE Technical Reference Manual

The PRoC BLE Technical Reference Manual (TRM) describes the PRoC BLE device functionality in detail, with register-level descriptions. The document is divided into two parts: the Architecture TRM and the Register TRM.

10.5 PSoC 4 BLE Technical Reference Manual

The PSoC 4 BLE Technical Reference Manual (TRM) describes the PSoC 4 BLE device functionality in detail, with register-level descriptions. The document is divided into two parts: the Architecture TRM and the Register TRM.

10.6 Learning PSoC Creator

Visit the PSoC Creator home page to download the latest version of PSoC Creator. Launch PSoC Creator and navigate to the following items:

- **Simple Component example projects**: Choose **File** > **Open** > **Example projects**. These example projects demonstrate how to configure and use PSoC Creator Components.
- **System Reference Guide**: Choose **Help** > **System Reference** > **System Reference Guide**. This guide lists and describes the system functions provided by PSoC Creator.
- **Component datasheets**: Right-click a Component and select “Open Datasheet.”

10.7 Application Notes

Application notes assist you with understanding specific features of the device for designing your PSoC application. For a complete list, visit Cypress BLE application notes.

10.8 Technical Support

If you have any questions, our technical support team is happy to assist you. You can create a support request by visiting Cypress Technical Support.

If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. You can also use the following support resources if you need quick assistance.

- Self-help
- Local sales office locations

11 Summary

This application note explored the EZ-BLE Module solution, architecture, development tools, host board placement and orientation, and production manufacturing. EZ-BLE Modules are fully integrated BLE solutions that allow rapid development and production release for customer applications. The core of the EZ-BLE Modules is the PRoC BLE and PSoC 4 BLE ICs, providing a programmable embedded system-on-chip, integrating the BLE radio, configurable analog and digital peripheral functions, memory, and an ARM Cortex-M0 microcontroller. EZ-BLE Modules are available in multiple options to service the needs of any customer application.

12 Related Application Notes

- AN91445 – Antenna Design Guide
- AN94020 – Getting Started with PRoC® BLE
- AN91267 – Getting Started with PSoC® 4 BLE
- AN95089 – PSoC® 4/PRoC™ BLE Crystal Oscillator Selection and Tuning Techniques
- AN91162 – Creating a BLE Custom Profile
- AN91184 – PSoC 4 BLE - Designing BLE Applications
- AN92584 – Designing for Low Power and Estimating Battery Life for BLE Applications
- AN85951 – PSoC® 4 CapSense® Design Guide

About the Author

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Title: Senior Business Unit Director

Background: David Solda has a BS in Computer/Electrical Engineering, a BS in Mathematics, and an MBA from Santa Clara University, California.

Appendix A. Cypress Terms of Art

This section lists the most commonly used terms that you might hear while working with Cypress's PSoC family of devices.

PSoC – PSoC is a programmable, embedded design platform that includes a CPU, such as the 32-bit ARM Cortex-M0, with both analog and digital programmable blocks. It accelerates embedded system design with reliable, easy-to-use solutions, such as touch sensing and enables low-power designs.

PRoC BLE – PRoC BLE is a 32-bit, 48-MHz ARM Cortex-M0 BLE solution with CapSense, 12-bit ADC, four timers, counters, pulse-width modulators (TCPWM), thirty-six GPIOs, two serial communication blocks (SCBs), LCD, and I2S. PRoC BLE includes a royalty-free BLE stack compatible with Bluetooth 4.2 and provides a complete, programmable, and flexible solution for HID, remote controls, toys, beacons, and wireless chargers. In addition to these applications, PRoC BLE provides a simple, low-cost way to add BLE connectivity to any system.

PSoC 4 BLE – A PSoC 4 IC with an integrated BLE radio that includes a royalty-free BLE protocol stack compatible with the Bluetooth 4.2 specification.

EZ-BLE™ PRoC Module (EZ-BLE PRoC) – EZ-BLE PRoC Module is a fully integrated, fully certified, 10 mm × 10 mm × 1.8 mm, programmable, Bluetooth Smart or Bluetooth Low Energy (BLE) module designed for ease-of-use and reducing time-to-market. It contains Cypress's PRoC BLE chip, two crystals, chip antenna, shield and passive components. EZ-BLE PRoC Module provides a simple and low cost way to add a microcontroller, CapSense touch controller and Bluetooth Smart connectivity to any system.

EZ-BLE™ PSoC Module (EZ-BLE PSoC) – An integrated, easy-to-use, fully certified Bluetooth Smart module designed to reduce time-to-market and development cost. Contains PSoC 4 BLE, two crystals, an antenna and passive components

PSoC Creator™ – PSoC 3, PSoC 4, and PSoC 5LP Integrated Design Environment (IDE) software that installs on your PC and allows concurrent hardware and firmware design of PSoC systems, or hardware design followed by export to other popular IDEs.

Components – Free embedded ICs represented by an icon in PSoC Creator software. These are used to integrate multiple ICs and system interfaces into one PSoC Component that are inherently connected to the MCU via the main system bus. For example, the BLE Component creates Bluetooth Smart products in minutes. Similarly, you can use the Programmable Analog Components for sensors.

BLE Component – A Component that creates Bluetooth Smart products in minutes. Includes a Component Configuration Tool that makes the complex BLE Protocol Stack and Profiles simple to implement with a GUI

Component Configuration Tool – Simple graphical user interface in PSoC Creator that is included in each Component. It is used to customize the Component parameters and is accessed by right-clicking a Component.

PSoC Programmer – PSoC Programmer is a flexible, integrated programming application for programming PSoC devices. PSoC Programmer is integrated with PSoC Creator to program PSoC 3, PSoC 4, PRoC, and PSoC 5LP designs.

MiniProg3 – Programming hardware for development purposes that can be used to program PSoC devices on your custom board or PSoC development kits that do not support a built-in programmer.

Timer/Counter/PWM (TCPWM) Block – A PSoC Programmable Digital Block that is configurable as a 16-bit Timer, Counter, PWM or quadrature decoder.

Programmable Analog Block – A hardware block that is configured using PSoC Components to create Analog Front Ends (AFEs), signal conditioning circuits with opamps and filters. Includes Continuous Time Blocks, analog-to-digital converters (ADCs) and digital-to-analog converters (DACs).

Continuous Time Block (CTB) – A Programmable Analog Block that is used to implement continuous time analog circuits such as opamps and programmable gain amplifiers (PGAs)

Programmable Digital Block – A hardware block that is configured using PSoC Components to implement custom digital peripherals and glue logic Includes Universal Digital Blocks, Serial Communication Blocks (SCBs) and TCPWMs.

Universal Digital Block (UDB) – A PSoC Programmable Digital Block that contains two programmable logic devices (PLDs), one programmable datapath with an arithmetic logic unit (ALU), one status register and one control register. Configured in PSoC Creator using PSoC Components, or with the graphical UDB editor or using Verilog code

Serial Communication Block (SCB) – A PSoC Programmable Digital Block that is configurable as a UART, SPI or I2C interface.

CapSense® – Cypress's third-generation touch-sensing user interface solution that "just works" in noisy environments and in the presence of water. The industry's No. 1 solution in sales by 4x over No. 2.

Component Configuration Tools – Simple graphical user interfaces in PSoC Creator embedded in each Component. Used to customize Component parameters as shown to the right.

Appendix B. EZ-BLE Module Product Details

Appendix B provides detailed information on each of the respective EZ-BLE Modules. The information contained for each module part number includes the following:

- Physical image for each EZ-BLE Module marketing part number
- Pinout and functionality for each EZ-BLE Module marketing part number
- Recommended host PCB layout footprint for each EZ-BLE Module marketing part number
- Recommended additional clearance area for each EZ-BLE Module marketing part number

To jump to your specific EZ-BLE Module, click the marketing part number in the below list:

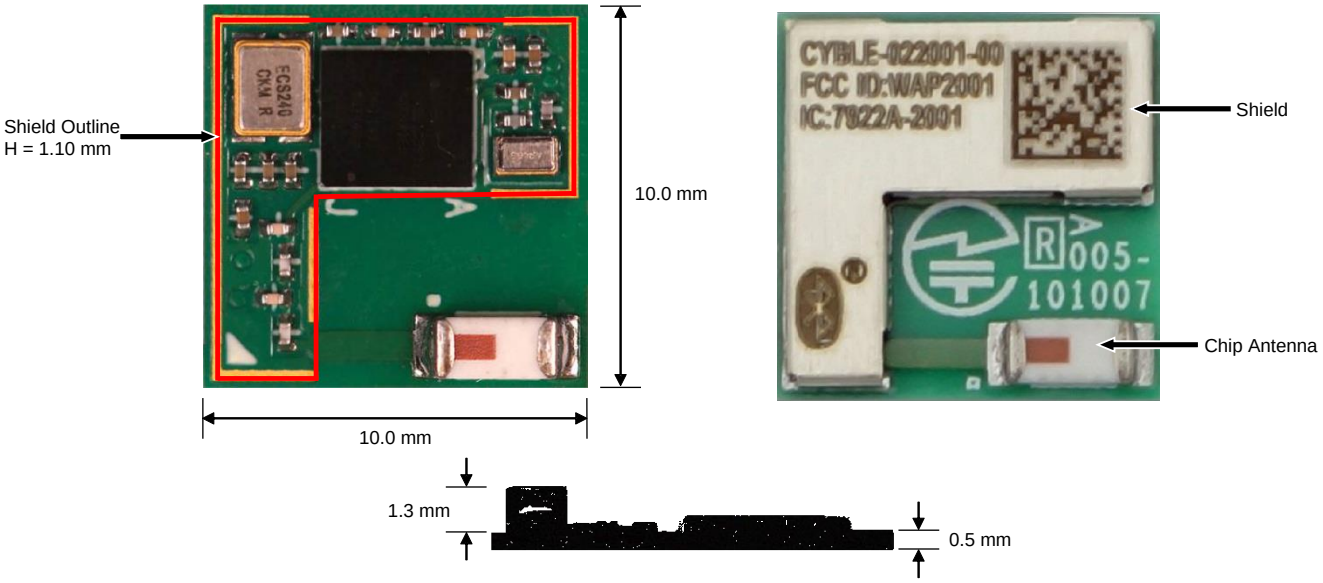
- CYBLE-022001-00
- CYBLE-2220XX-0X
- CYBLE-01201X-X0 (CYBLE-012011-00 and CYBLE-012012-10)
- CYBLE-2120XX-XX (CYBLE-212019-00, CYBLE-212023-10, and CYBLE-212020-01)
- CYBLE-014008-00
- CYBLE-2140XX-0X (CYBLE-214009-00 and CYBLE-214015-01)
- CYBLE-2X20XX-X1 XR (CYBLE-212006-01, CYBLE-202007-01, and CYBLE-202013-11)
- CYBLE-22411X-0X (CYBLE-224110-00 and CYBLE-224116-01)

B.1 EZ-BLE Module Part Number Details

B.1.1 CYBLE-022001-00

Figure 66 shows a physical picture of the CYBLE-022001-00 EZ-BLE PRoC module.

Figure 66. CYBLE-022001-00 Module Top View (with and without Shield) and Side View

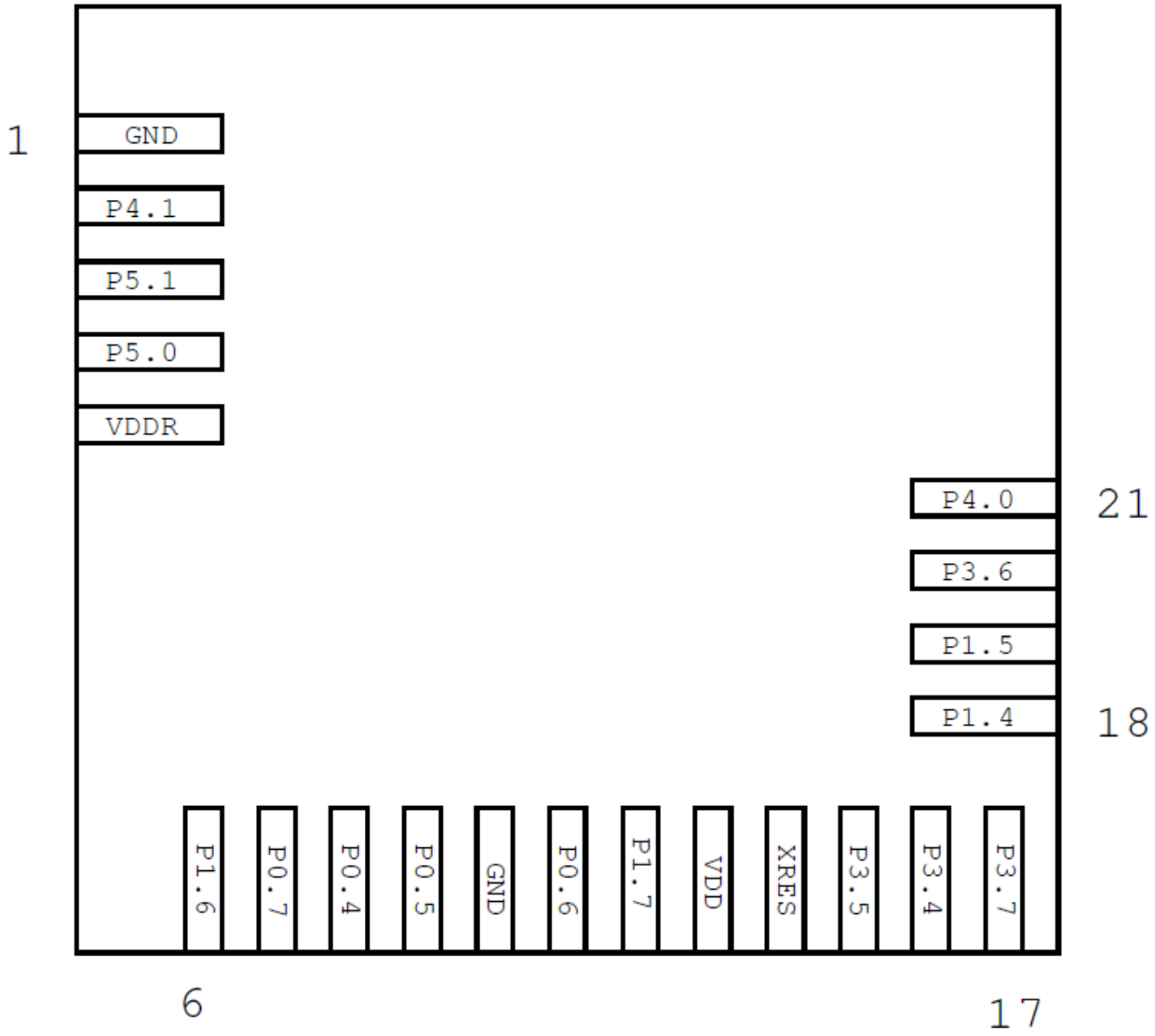


For more details on this module's dimensions, external component connections, and module placement recommendations, see the CYBLE-022001-00 datasheet specification.

B.1.1.1 Pinout and Functionality

The CYBLE-022001-00 module is designed to mount as a component on an end-product PCB. Only a portion of the available I/O of the PRoC BLE silicon device is exposed on the CYBLE-022001-00 module in order to minimize the module footprint size. The CYBLE-022001-00 module contains 21 connections on the bottom side of the module. Figure 67 details the bottom side connections available on the CYBLE-022001-00 module.

Figure 67. CYBLE-022001-00 Module Bottom View (Seen from Bottom)



A list of the available I/Os and supported functionality for each I/O of the CYBLE-022001-00 is shown in Table 6.

Table 6. CYBLE-022001-00 Module Available Connections and Functionality

Module Solder Pad Number	Silicon Port Pin	Functionality									
		UART	SPI	I2C	TCPWM[10, 11]	CapSense	LCD Drive	WCO Out	ECO_OUT[12]	SWD	GPIO[13]
1	GND		Ground Connection								
2	P4[1]	SCB1_CTS	SCB1_MISO		TCPWM0_N	Sensor/C_{TANK}	Yes				Yes
3	P5[1]	SCB1_TX	SCB1_SCLK	SCB1_SCL	TCPWM3_N	Sensor	Yes		Yes		Yes
4	P5[0]	SCB1_RX	SCB1_SS	SCB1_SDA	TCPWM3_P	Sensor	Yes				Yes
5	VDDR	Radio Power Supply 1.9 V to 5.5 V									
6	P1[6]	SCB0_RTS	SCB0_SS		TCPWM	Sensor	Yes				Yes
7	P0[7]	SCB0_CTS	SCB0_SCLK		TCPWM	Sensor	Yes			SWDCLK[14]	Yes
8	P0[4]	SCB0_RX	SCB0_MOSI	SCB0_SDA	TCPWM	Sensor	Yes		Yes		Yes
9	P0[5]	SCB0_TX	SCB0_MISO	SCB0_SCL	TCPWM	Sensor	Yes				Yes
10	GND	Ground Connection									
11	P0[6]	SCB0_RTS	SCB0_SS		TCPWM	Sensor	Yes			SWDIO[14]	Yes
12	P1[7]	SCB0_CTS	SCB0_SCLK		TCPWM	Sensor	Yes				Yes
13	VDD	Digital Power Supply Input 1.71 to 5.5V									
14	XRES	External Reset Hardware Connection Input									
15	P3[5]	SCB1_TX		SCB1_SCL	TCPWM	Sensor	Yes				Yes
16	P3[4]	SCB1_RX		SCB1_SDA	TCPWM	Sensor	Yes				Yes
17	P3[7]	SCB1_CTS	SCB1_MISO		TCPWM	Sensor	Yes	Yes			Yes
18	P1[4]	SCB0_RX	SCB0_MOSI	SCB0_SDA	TCPWM	Sensor	Yes				Yes
19	P1[5]	SCB0_TX	SCB0_MISO	SCB0_SCL	TCPWM	Sensor	Yes				Yes
20	P3[6]	SCB1_RTS			TCPWM	Sensor	Yes				Yes
21	P4[0]	SCB1_RTS	SCB1_MOSI		TCPWM0_P	C_{MOD}	Yes				Yes

[10] Timer, counter, pulse-width modulator (PWM); configurable as 16-bit timer, counter, PWM blocks

[11] TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity. TCPWM connections on ports 4 and 5 are direct and can only be used with the specified TCPWM block and polarity specified above.

[12] External Crystal Oscillator Output from the device/module

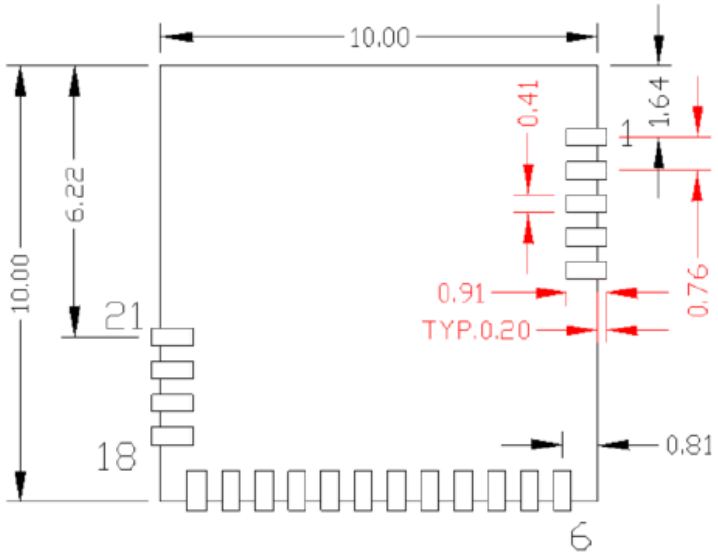
[13] General Purpose Input/Output

[14] SDWCLK and SWDIO connections can be multiplexed as the functional options listed in each of the respective rows and can be used for programming without the need to reconfigure the device I/O.

B.1.1.2 Host Recommended PCB Layout

To assist in the host PCB layout design for the CYBLE-022001-00, Cypress provides three host PCB landing pattern reference drawings in Figure 68, Figure 69, and in Figure 70, and Table 7. Figure 68 provides a dimensioned view of the host PCB layout. Figure 69 provides the location to the center edge of each solder pad relative to the origin of the module (upper right PCB outline). Figure 70 and Table 7 provides the location to each solder pad center location for the host PCB layout. Dimensions shown are in mm unless otherwise stated.

Figure 68. Host Board Required PCB Layout Pattern (Dimensioned View)



Note: Pad length shown includes overhang of the host pad beyond the module pad outline. The minimum recommended pad length on the host PCB is 0.91 mm.

Figure 69. Host Board Required PCB Layout Pattern: To Pad Center Edge Relative to Origin

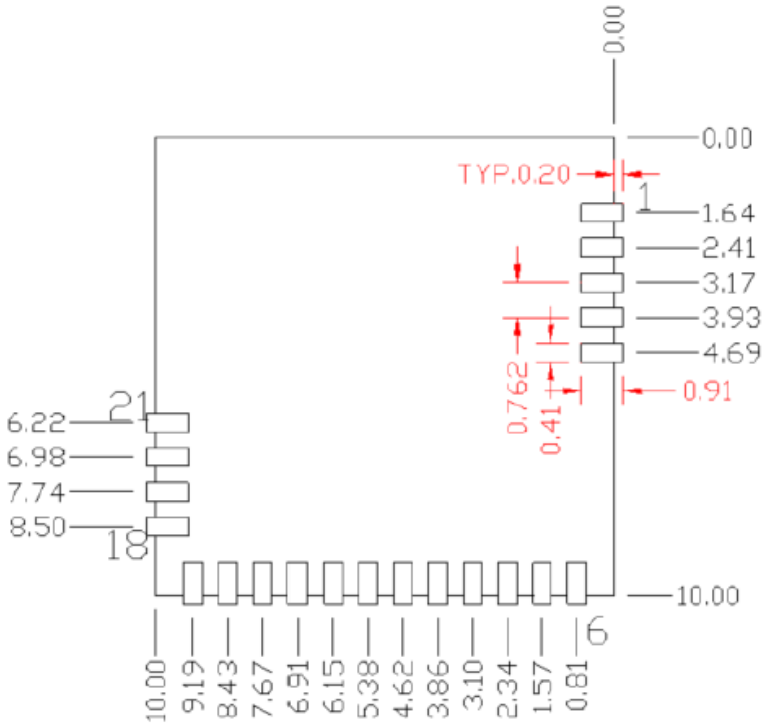


Figure 70. Host Board Required PCB Layout Pattern To Pad Center Relative to Origin

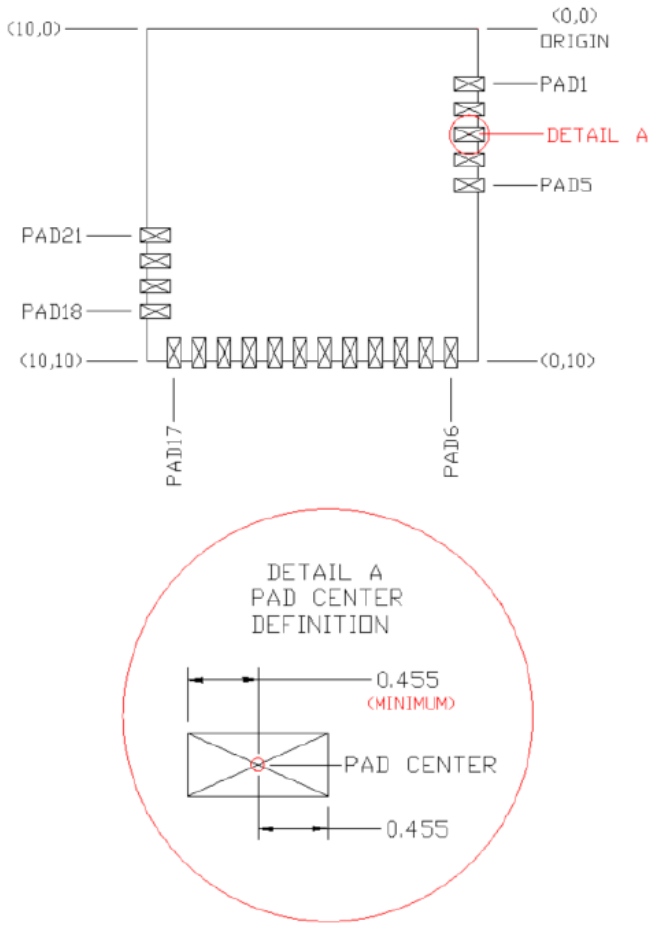
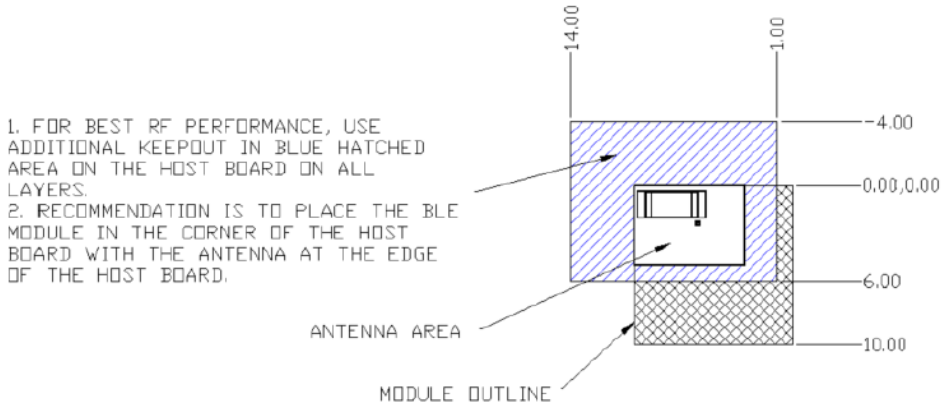


Table 7. Location to Pad Center from Origin (dimensions in mm and mils)

Solder Pad (Center of Pad)	Location (X,Y) from Origin (mm)	Location (X,Y) from Origin (mils)
1	(0.26, 1.64)	(10.24, 64.57)
2	(0.26, 2.41)	(10.24, 94.88)
3	(0.26, 3.17)	(10.24, 124.80)
4	(0.26, 3.93)	(10.24, 154.72)
5	(0.26, 4.69)	(10.24, 184.65)
6	(0.81, 9.74)	(31.89, 383.46)
7	(1.57, 9.74)	(61.81, 383.46)
8	(2.34, 9.74)	(92.13, 383.46)
9	(3.10, 9.74)	(122.05, 383.46)
10	(3.86, 9.74)	(151.97, 383.46)
11	(4.62, 9.74)	(181.89, 383.46)
12	(5.38, 9.74)	(211.81, 383.46)
13	(6.15, 9.74)	(242.13, 383.46)
14	(6.91, 9.74)	(272.05, 383.46)
15	(7.67, 9.74)	(301.97, 383.46)
16	(8.43, 9.74)	(331.89, 383.46)
17	(9.19, 9.74)	(361.81, 383.46)
18	(9.75, 8.50)	(383.86, 334.65)
19	(9.75, 7.74)	(383.86, 304.72)
20	(9.75, 6.98)	(383.86, 274.80)
21	(9.75, 6.22)	(383.86, 244.88)

Figure 71 details additional host board keep out area to achieve optimal RF performance with the CYBLE-022001-00 module (denoted in blue hatched area).

Figure 71. Host Board Additional Keep Out Area for Optimal RF Performance

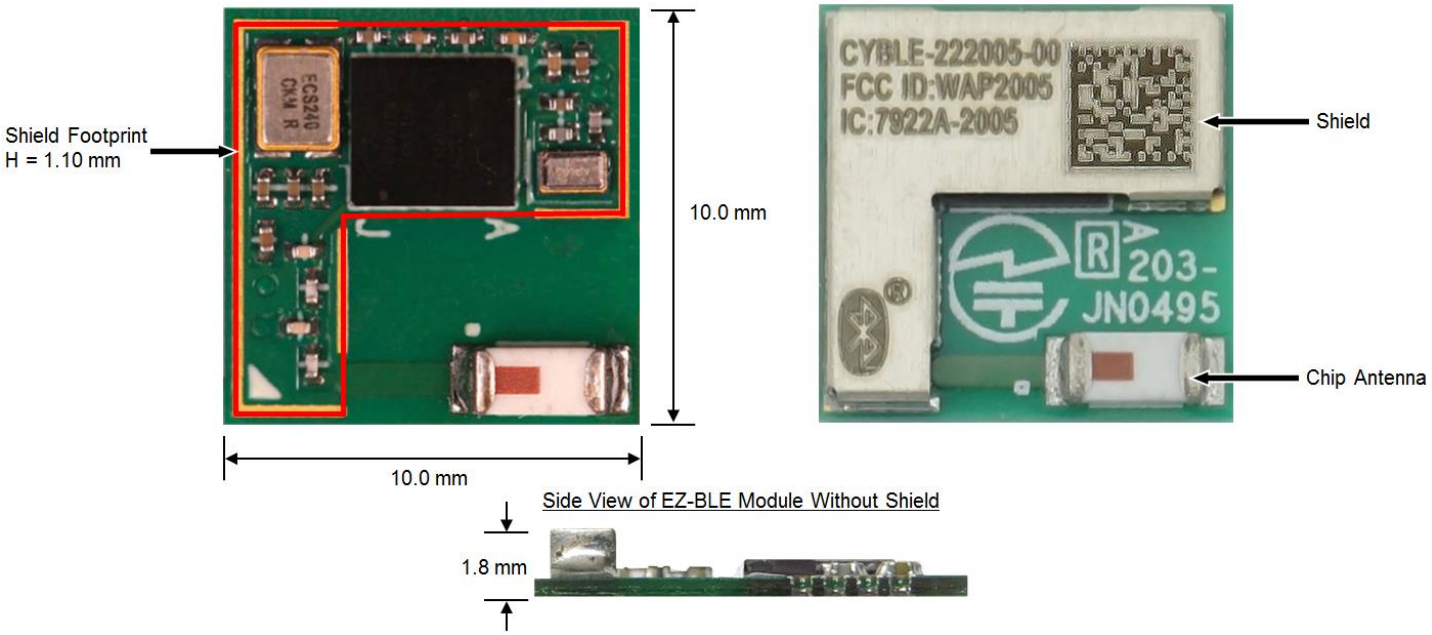


B.1.2 CYBLE-2220XX-0X

This section contains information on the CYBLE-222005-00 and CYBLE-222014-01 modules. The only difference between these module is the BLE standard support (v4.1 for the CYBLE-222005-00 vs. v4.2 for the CYBLE-222014-01). The CYBLE-2220XX-0X is drop-in compatible with the CYBLE-022001-00 module. Although the CYBLE-2220XX-0X includes an additional VREF connection on the module, this connection is optional and is not required to maintain the same functionality as done with the CYBLE-022001-00. The CYBLE-2220XX-0X is a flash and SRAM upgrade to the CYBLE-022001-00, moving from 128-KB flash and 16-KB SRAM to 256-KB flash and 32-KB SRAM, with an optional upgrade to Bluetooth specification v4.2 with the CYBLE-222014-01.

Figure 72 shows a physical picture of the CYBLE-222005-00 EZ-BLE PRoC module. The form factor and image of the CYBLE-222014-01 is identical to the CYBLE-222005-00 with the exception of the laser marking on the top of the shield.

Figure 72. CYBLE-222005-00 Module Top View (with and without Shield) and Side View

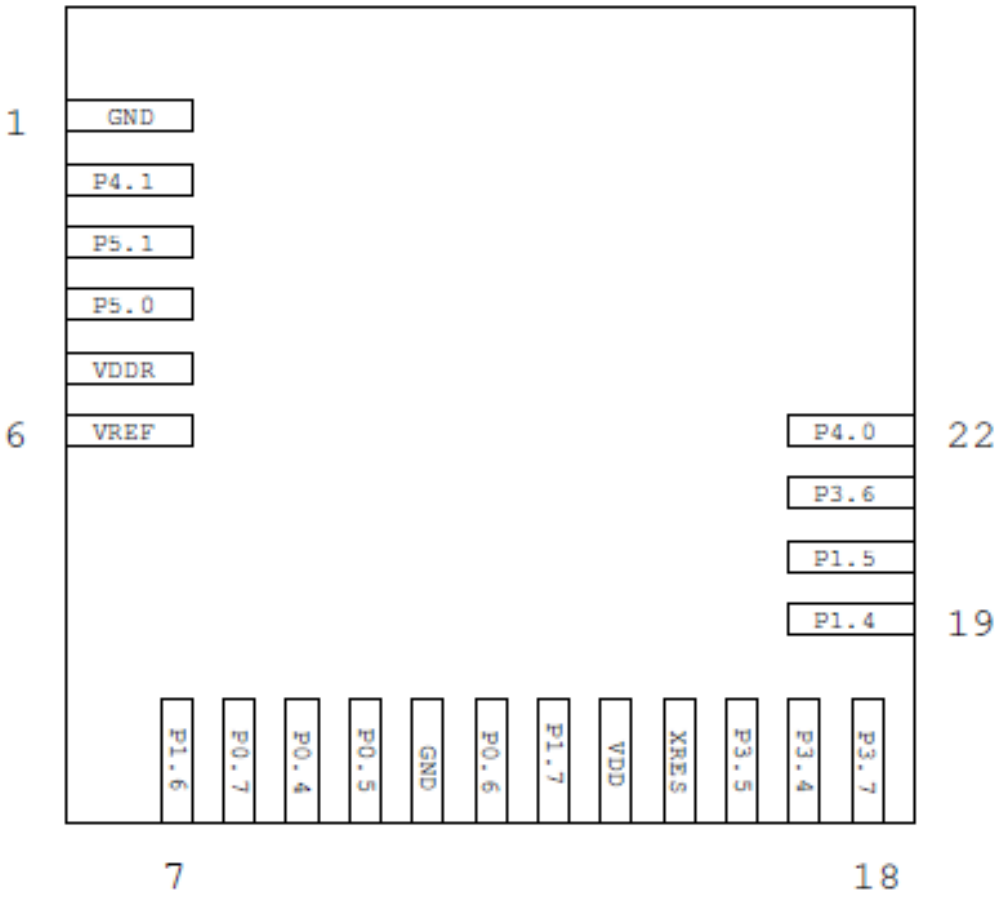


For more details on this module's dimensions, external component connections, and module placement recommendations, see the CYBLE-222005-00 datasheet specification or the CYBLE-222014-01 datasheet specification.

B.1.2.1 Pinout and Functionality

The CYBLE-2220XX-0X module is designed to mount as a component on an end-product PCB. Only a portion of the available I/O of the PRoC BLE silicon device is exposed on the CYBLE-2220XX-0X module in order to minimize the module footprint size. The CYBLE-2220XX-0X module contains 22 connections on the bottom side of the module. Figure 73 details the bottom side connections available on the CYBLE-2220XX-0X module.

Figure 73. CYBLE-2220XX-0X Module Bottom View (Seen from Bottom)



A list of the available I/Os and supported functionality for each I/O of the CYBLE-2220XX-0X is shown in Table 8.

Table 8. CYBLE-2220XX-0X Module Available Connections and Functionality

Module Solder Pad Number	Silicon Port Pin	Functionality									
		UART	SPI	I2C	TCPWM[15, 16]	CapSense	LCD Drive	WCO Out	ECO_OUT[17]	SWD	GPIO[18]
1	GND		Ground Connection								
2	P4[1]	SCB1_CTS	SCB1_MISO		TCPWM0_N	Sensor/C_{TANK}	Yes				Yes
3	P5[1]	SCB1_TX	SCB1_SCLK	SCB1_SCL	TCPWM3_N	Sensor	Yes		Yes		Yes
4	P5[0]	SCB1_RX	SCB1_SS	SCB1_SDA	TCPWM3_P	Sensor	Yes				Yes

[15] Timer, counter, pulse-width modulator (PWM); configurable as 16-bit timer, counter, PWM blocks

[16] TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity. TCPWM connections on ports 4 and 5 are direct and can only be used with the specified TCPWM block and polarity specified above.

[17] External Crystal Oscillator Output from the device/module

[18] General Purpose Input/Output

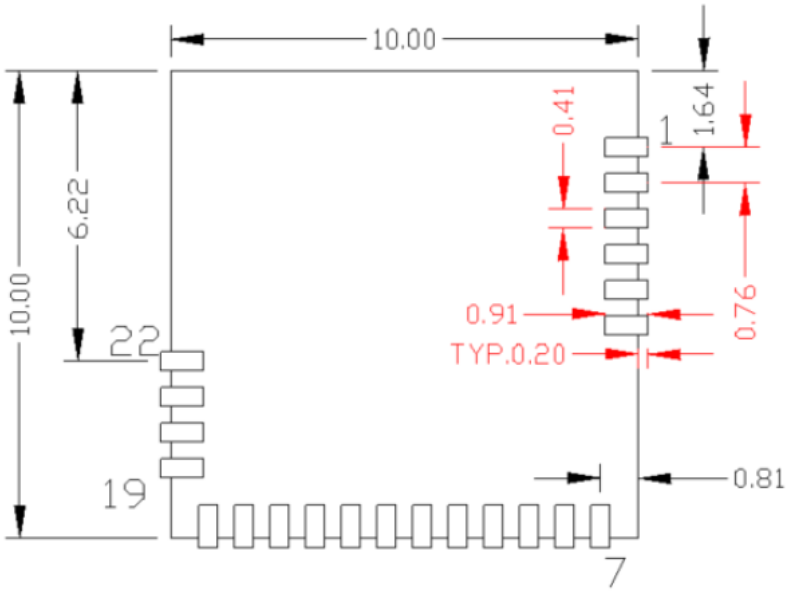
Module Solder Pad Number	Silicon Port Pin	Functionality									
		UART	SPI	I2C	TCPWM[15, 16]	CapSense	LCD Drive	WCO Out	ECO_OUT[17]	SWD	GPIO[18]
5	VDDR	Radio Power Supply 1.9 V to 5.5 V									
6	VREF	Reference Voltage Inputs (Optional)									
7	P1[6]	SCB0_RTS	SCB0_SS		TCPWM	Sensor	Yes				Yes
8	P0[7]	SCB0_CTS	SCB0_SCLK		TCPWM	Sensor	Yes			SWDCLK[19]	Yes
9	P0[4]	SCB0_RX	SCB0_MOSI	SCB0_SDA	TCPWM	Sensor	Yes		Yes		Yes
10	P0[5]	SCB0_TX	SCB0_MISO	SCB0_SCL	TCPWM	Sensor	Yes				Yes
11	GND	Ground Connection									
12	P0[6]	SCB0_RTS	SCB0_SS		TCPWM	Sensor	Yes			SWDIO[19]	Yes
13	P1[7]	SCB0_CTS	SCB0_SCLK		TCPWM	Sensor	Yes				Yes
14	VDD	Digital Power Supply Input 1.71 to 5.5V									
15	XRES	External Reset Hardware Connection Input									
16	P3[5]	SCB1_TX		SCB1_SCL	TCPWM	Sensor	Yes				Yes
17	P3[4]	SCB1_RX		SCB1_SDA	TCPWM	Sensor	Yes				Yes
18	P3[7]	SCB1_CTS	SCB1_MISO		TCPWM	Sensor	Yes	Yes			Yes
19	P1[4]	SCB0_RX	SCB0_MOSI	SCB0_SDA	TCPWM	Sensor	Yes				Yes
20	P1[5]	SCB0_TX	SCB0_MISO	SCB0_SCL	TCPWM	Sensor	Yes				Yes
21	P3[6]	SCB1_RTS			TCPWM	Sensor	Yes				Yes
22	P4[0]	SCB1_RTS	SCB1_MOSI		TCPWM0_P	C_{MOD}	Yes				Yes

[19] SDWCLK and SWDIO connections can be multiplexed as the functional options listed in each of the respective rows and can be used for programming without the need to reconfigure the device I/O.

B.1.2.2 Host Recommended PCB Layout

To assist in the host PCB layout design for the CYBLE-2220XX-0X, Cypress provides three host PCB landing pattern reference drawings in Figure 74, Figure 75, and in Figure 76 and Table 9. Figure 74 provides a dimensions view of the host PCB layout. Figure 75 provides the location to the center edge of each solder pad relative to the origin of the module (upper right PCB outline). Figure 76 and Table 9 provides the location to each solder pad center location for the host PCB layout. Dimensions shown are in mm unless otherwise stated.

Figure 74. Host Board Required PCB Layout Pattern (Dimensioned View)



Note: Pad length shown includes overhang of the host pad beyond the module pad outline. The minimum recommended pad length on the host PCB is 0.91 mm.

Figure 75. Host Board Required PCB Layout Pattern: To Pad Center Edge Relative to Origin

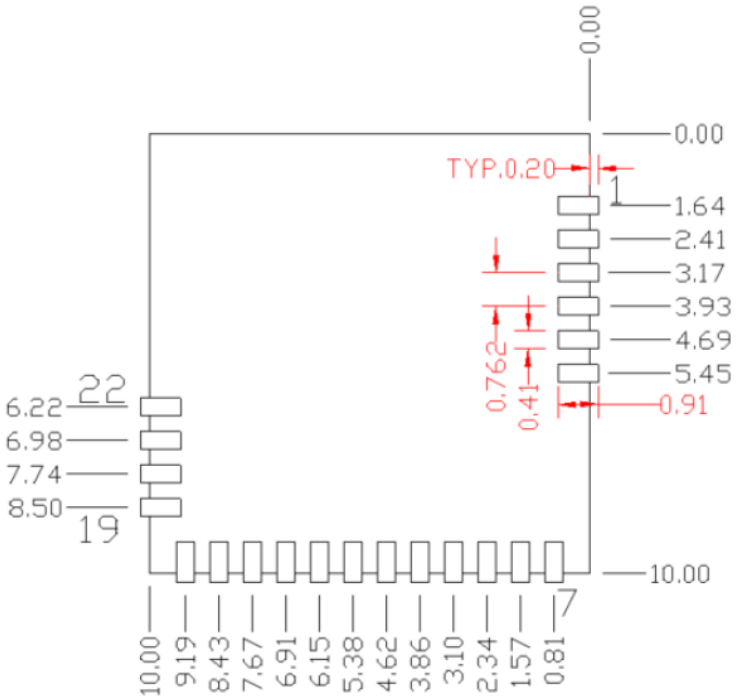


Figure 76. Host Board Required PCB Layout Pattern To Pad Center Relative to Origin

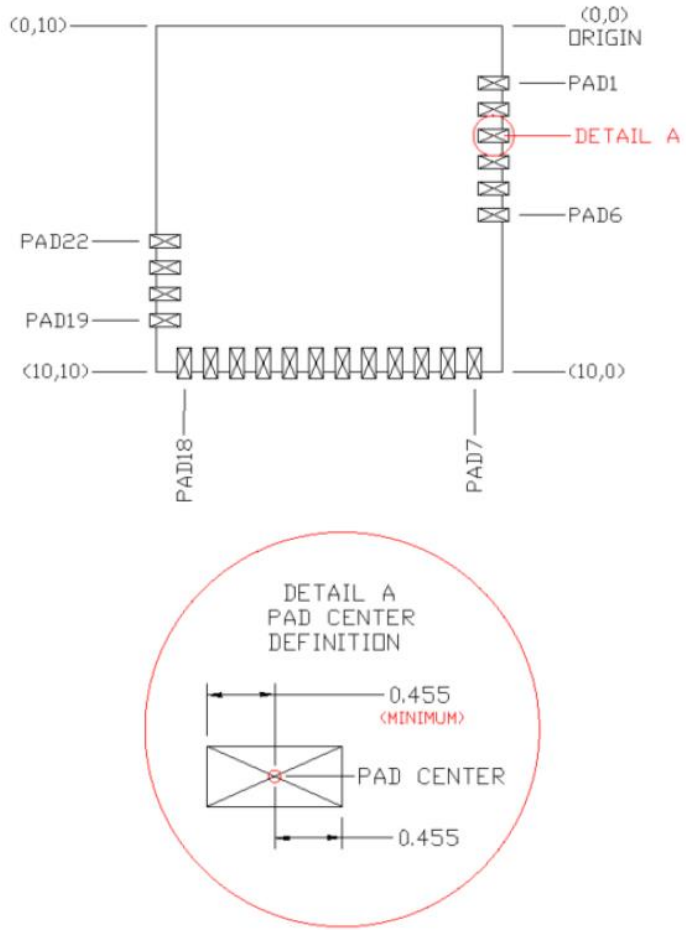
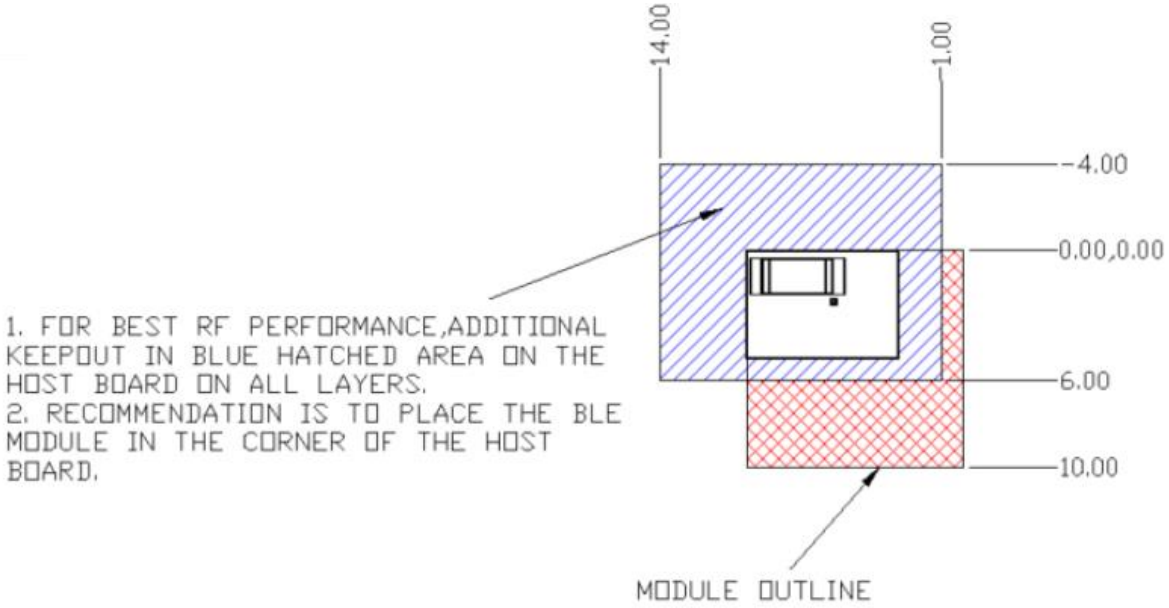


Table 9. Location to Pad Center from Origin (dimensions in mm and mils)

Solder Pad (Center of Pad)	Location (X,Y) from Origin (mm)	Location (X,Y) from Origin (mils)
1	(0.26, 1.64)	(10.24, 64.57)
2	(0.26, 2.41)	(10.24, 94.88)
3	(0.26, 3.17)	(10.24, 124.80)
4	(0.26, 3.93)	(10.24, 154.72)
5	(0.26, 4.69)	(10.24, 184.65)
6	(0.26, 5.45)	(10.24, 214.57)
7	(0.81, 9.74)	(31.89, 383.46)
8	(1.57, 9.74)	(61.81, 383.46)
9	(2.34, 9.74)	(92.13, 383.46)
10	(3.10, 9.74)	(122.05, 383.46)
11	(3.86, 9.74)	(151.97, 383.46)
12	(4.62, 9.74)	(181.89, 383.46)
13	(5.38, 9.74)	(211.81, 383.46)
14	(6.15, 9.74)	(242.13, 383.46)
15	(6.91, 9.74)	(272.05, 383.46)
16	(7.67, 9.74)	(301.97, 383.46)
17	(8.43, 9.74)	(331.89, 383.46)
18	(9.19, 9.74)	(361.81, 383.46)
19	(9.75, 8.50)	(383.86, 334.65)
20	(9.75, 7.74)	(383.86, 304.72)
21	(9.75, 6.98)	(383.86, 274.80)
22	(9.75, 6.22)	(383.86, 244.88)

Figure 77 details additional host board keep-out area to achieve an optimal RF performance with the CYBLE-2220XX-0X module.

Figure 77. Host Board Additional Keep Out Area for Optimal RF Performance



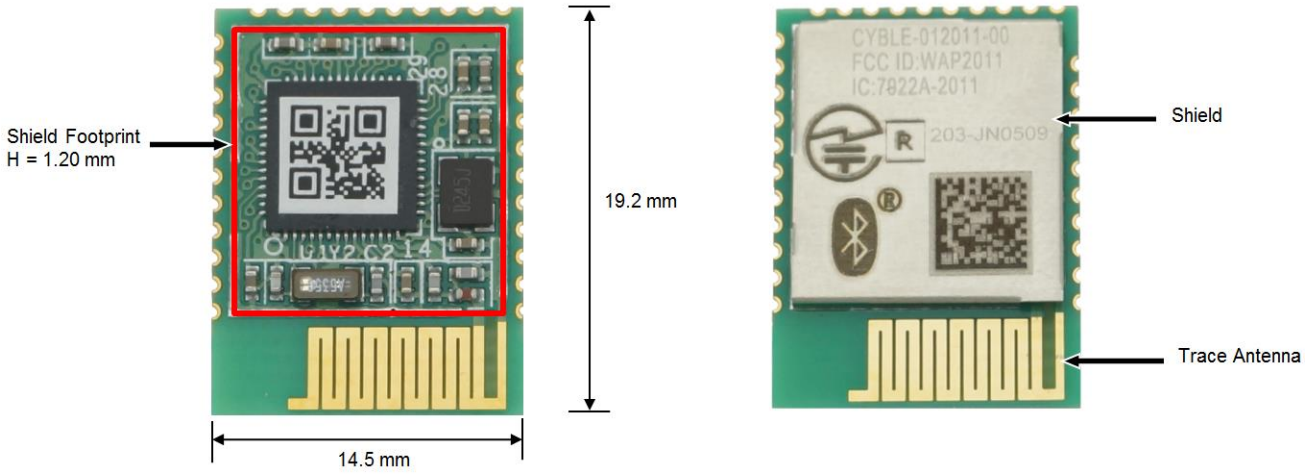
B.1.3 CYBLE-01201X-X0

The CYBLE-01201X-X0 is a cost-optimized platform designed to minimize system cost for applications that can utilize a larger module form factor. This platform is available in a fully certified and qualified option (CYBLE-012011-00), as well as a subset device that is not certified nor qualified with Bluetooth SIG (CYBLE-012012-10). The CYBLE-012011-00 and CYBLE-012012-10 are pin-for-pin compatible with each other. The CYBLE-012012-10 does not come with the RF metal shield on the top side of the module.

The mechanical drawing and reference layout information contained in this section is identical for both CYBLE-012011-00 and CYBLE-012012-10 modules.

Figure 78 shows a physical picture of the CYBLE-012011-00 EZ-BLE PRoC module.

Figure 78. CYBLE-012011-00 Module Top View (with and without Shield)

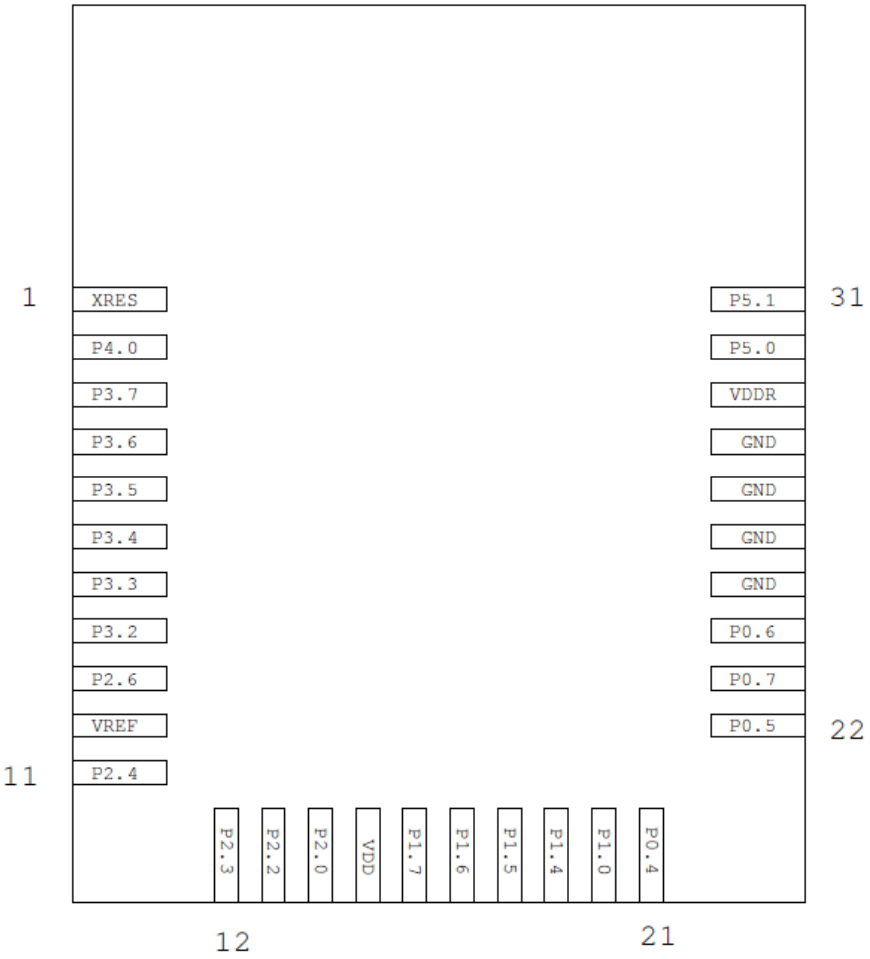


For more details on this module's dimensions, external component connections, and module placement recommendations, see the CYBLE-01201X-X0 datasheet specification.

B.1.3.1 Pinout and Functionality

The CYBLE-01201X-X0 module is designed to mount as a component on an end-product PCB. Only a portion of the available I/O of the PRoC BLE silicon device is exposed on the CYBLE-01201X-X0 module in order to minimize the module footprint size. The CYBLE-01201X-X0 module contains 31 connections on the bottom side of the module. Figure 79 details the bottom side connections available on the CYBLE-01201X-X0 module.

Figure 79. CYBLE-01201X-X0 Module Bottom View (Seen from Bottom)



A list of the available I/Os and supported functionality for each I/O of the CYBLE-01201X-X0 is shown in Table 10.

Table 10. CYBLE-01201X-X0 Module Available Connections and Functionality

Module Solder Pad Number	Silicon Port Pin	Functionality												
		UART	SPI	I2C	TCPWM[20, 21]	CapSense	LCD Drive	WCO Out	ECO_OUT[22]	SWD	SARMUX	OPAMP	LPCOMP	GPIO[23]
1	GND	Ground Connection												
1	XRES	External Reset Hardware Connection Input												
2	P4[0]	SCB1_RTS	SCB1_MOSI		TCPWM0_P	C_{MOD}	Yes							Yes
3	P3[7]	SCB1_CTS			TCPWM	Sensor	Yes	Yes			Yes			Yes

[20] Timer, counter, pulse-width modulator (PWM); configurable as 16-bit timer, counter, PWM blocks

[21] TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity. TCPWM connections on ports 4 and 5 are direct and can only be used with the specified TCPWM block and polarity specified above.

[22] External Crystal Oscillator Output from the device/module

[23] General Purpose Input/Output

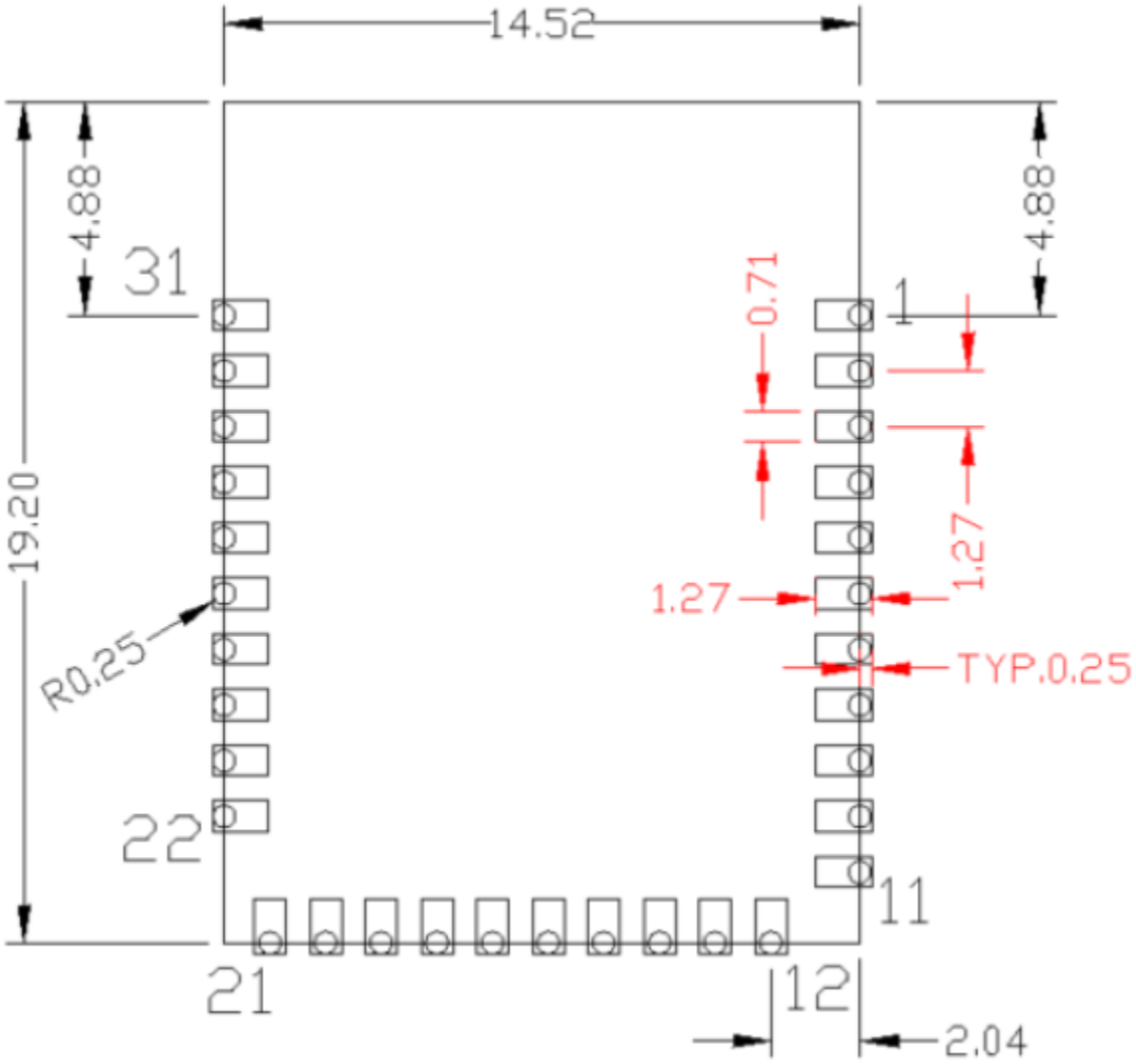
Module Solder Pad Number	Silicon Port Pin	Functionality												
		UART	SPI	I2C	TCPWM[20, 21]	CapSense	LCD Drive	WCO Out	ECO_OUT[22]	SWD	SARMUX	OPAMP	LPCOMP	GPIO[23]
4	P3[6]	SCB1_RTS			TCPWM	Sensor	Yes				Yes			Yes
5	P3[5]	SCB1_TX		SCB1_SCL	TCPWM	Sensor	Yes				Yes			Yes
6	P3[4]	SCB1_RX		SCB1_SDA	TCPWM	Sensor	Yes				Yes			Yes
7	P3[3]	SCB0_CTS			TCPWM	Sensor	Yes				Yes			Yes
8	P3[2]	SCB0_RTS			TCPWM	Sensor	Yes				Yes			Yes
9	P2[6]				TCPWM	Sensor	Yes							Yes
10	VREF	Reference Voltage Inputs (Optional)												
11	P2[4]				TCPWM	Sensor	Yes							Yes
12	P2[3]				TCPWM	Sensor	Yes	Yes						Yes
13	P2[2]		SCB0_SS3		TCPWM	Sensor	Yes							Yes
14	P2[0]		SCB0_SS1		TCPWM	Sensor	Yes							Yes
15	VDD	Digital and Analog Power Supply Input 1.71 to 5.5V												
16	P1[7]	SCB0_CTS	SCB0_SCLK		TCPWM	Sensor	Yes							Yes
17	P1[6]	SCB0_RTS	SCB0_SS0		TCPWM	Sensor	Yes							Yes
18	P1[5]	SCB0_TX	SCB0_MISO	SCB0_SCL	TCPWM	Sensor	Yes							Yes
19	P1[4]	SCB0_RX	SCB0_MOSI	SCB0_SDA	TCPWM	Sensor	Yes							Yes
20	P1[0]				TCPWM	Sensor	Yes		Yes					Yes
21	P0[4]	SCB0_RX	SCB0_MOSI	SCB0_SDA	TCPWM	Sensor	Yes		Yes					Yes
22	P0[5]	SCB0_TX	SCB0_MISO	SCB0_SCL	TCPWM	Sensor	Yes							Yes
23	P0[7]	SCB0_CTS	SCB0_SCLK		TCPWM	Sensor	Yes			SWDCLK[24]				Yes
24	P0[6]	SCB0_RTS	SCB0_SS0		TCPWM	Sensor	Yes			SWDIO[24]				Yes
25	GND	Ground Connection												
26	GND	Ground Connection												
27	GND	Ground Connection												
28	GND	Ground Connection												
29	VDDR	Radio Power Supply 1.9 V to 5.5 V												
30	P5[0]	SCB1_RX	SCB1_SS0	SCB1_SDA	TCPWM3_P	Sensor	Yes							Yes
31	P5[1]	SCB1_TX	SCB1_SCLK	SCB1_SCL	TCPWM3_N	Sensor	Yes		Yes					Yes

[24] SDWCLK and SWDIO connections can be multiplexed as the functional options listed in each of the respective rows and can be used for programming without the need to reconfigure the device I/O.

B.1.3.2 Host Recommended PCB Layout

To assist in the host PCB layout design for the CYBLE-01201X-X0, Cypress provides three host PCB landing pattern reference drawings in Figure 80, Figure 81, and in Figure 82 and Table 11. Figure 80 provides a dimensions view of the host PCB layout. Figure 81 provides the location to the center edge of each solder pad relative to the origin of the module (upper right PCB outline). Figure 82 and Table 11 provides the location to each solder pad center location for the host PCB layout. Dimensions shown are in mm unless otherwise stated.

Figure 80. Host Board Required PCB Layout Pattern (Dimensioned View)



Note: Pad length shown includes overhang of the host pad beyond the module pad outline. The minimum recommended pad length on the host PCB is 1.27 mm.

Figure 81. Host Board Required PCB Layout Pattern: To Pad Center Edge Relative to Origin

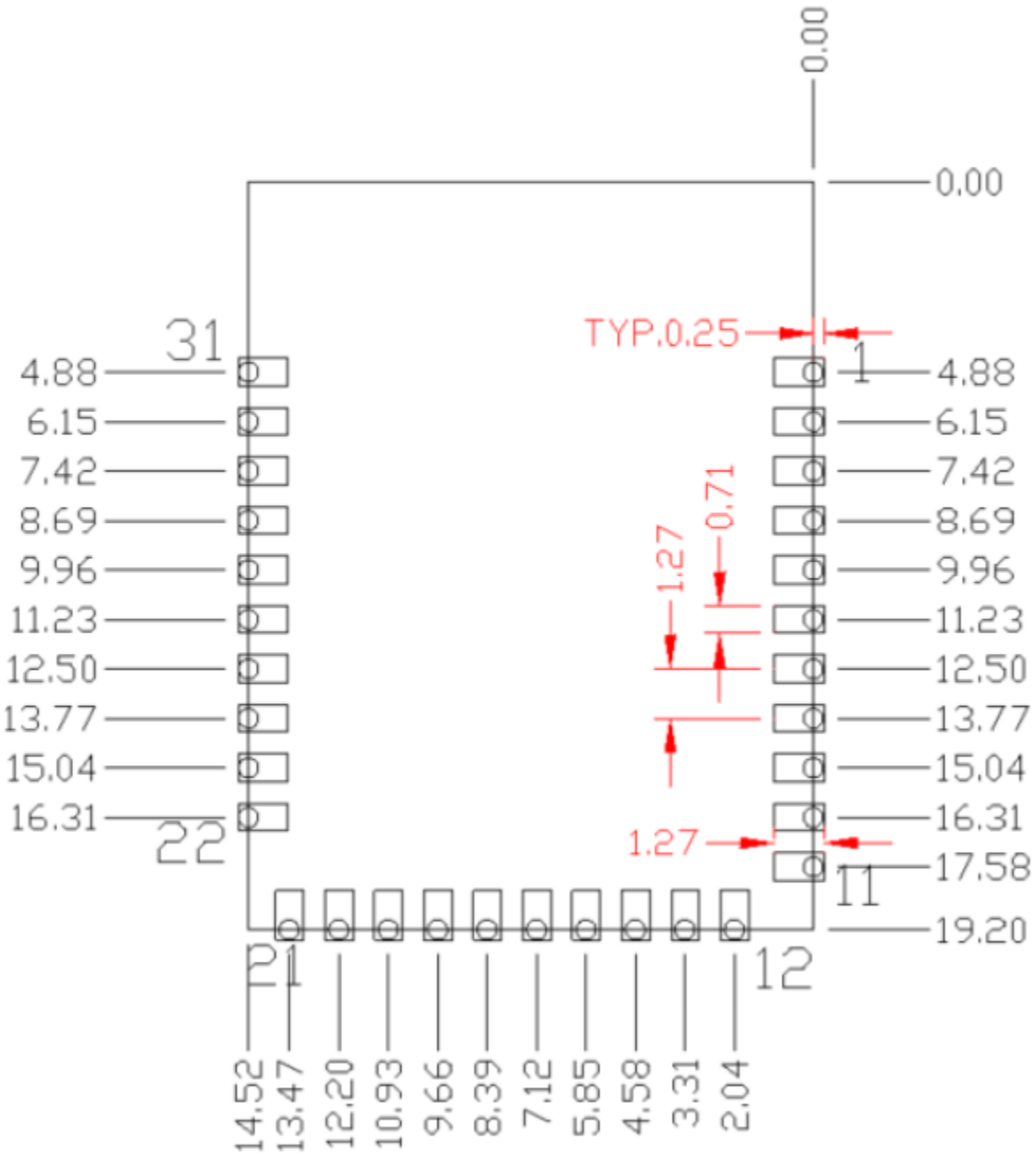


Figure 82. Host Board Required PCB Layout Pattern To Pad Center Relative to Origin

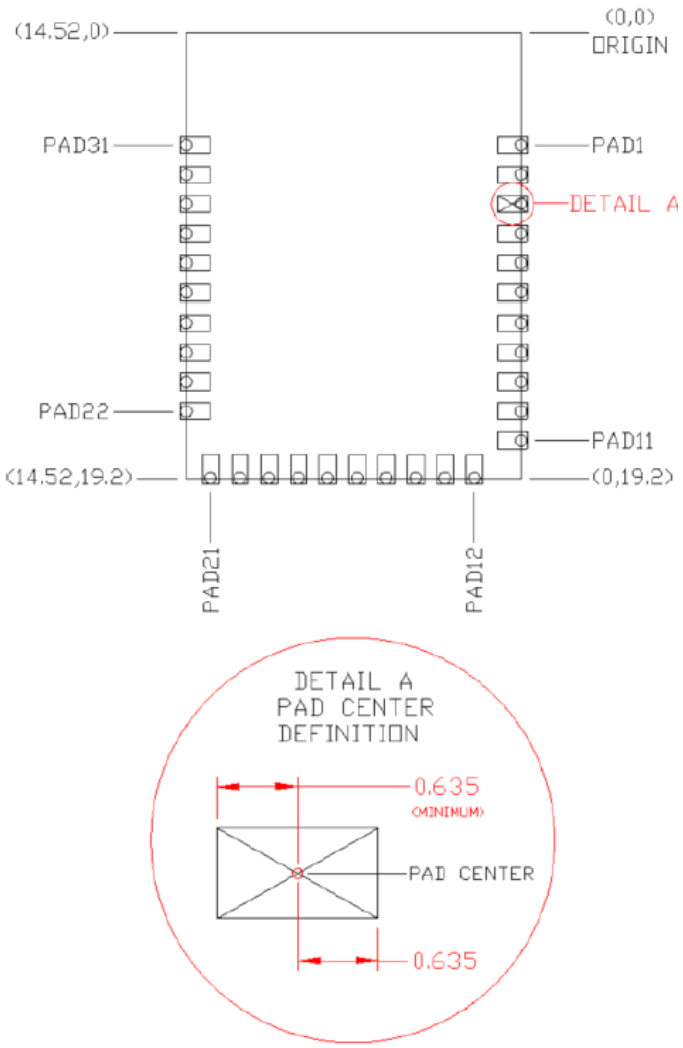
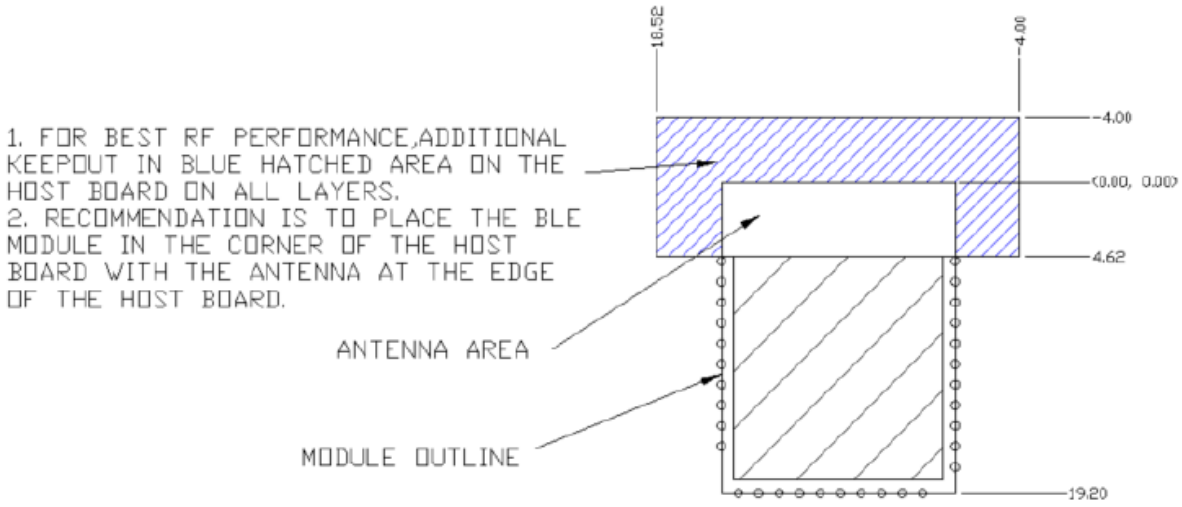


Table 11. Location to Pad Center from Origin (dimensions in mm and mils)

Solder Pad (Center of Pad)	Location (X,Y) from Origin (mm)	Location (X,Y) from Origin (mils)
1	(0.39, 4.88)	(15.35, 192.13)
2	(0.39, 6.15)	(15.35, 242.13)
3	(0.39, 7.42)	(15.35, 292.13)
4	(0.39, 8.69)	(15.35, 342.13)
5	(0.39, 9.96)	(15.35, 392.13)
6	(0.39, 11.23)	(15.35, 442.13)
7	(0.39, 12.50)	(15.35, 492.13)
8	(0.39, 13.77)	(15.35, 542.13)
9	(0.39, 15.04)	(15.35, 592.13)
10	(0.39, 16.31)	(15.35, 642.13)
11	(0.39, 17.58)	(15.35, 492.13)
12	(2.04, 18.82)	(80.31, 740.94)
13	(3.31 , 18.82)	(130.31 , 740.94)
14	(4.58 , 18.82)	(180.31 , 740.94)
15	(5.85 , 18.82)	(230.31 , 740.94)
16	(7.12 , 18.82)	(280.31 , 740.94)
17	(8.39 , 18.82)	(330.31 , 740.94)
18	(9.66 , 18.82)	(380.31 , 740.94)
19	(10.93 , 18.82)	(430.31 , 740.94)
20	(12.20 , 18.82)	(480.31 , 740.94)
21	(13.47, 18.82)	(530.31, 740.94)
22	(14.14, 16.31)	(556.69, 642.12)
23	(14.14, 15.04)	(556.69, 592.12)
24	(14.14, 13.77)	(556.69, 542.12)
25	(14.14, 12.50)	(556.69, 492.12)
26	(14.14, 11.23)	(556.69, 442.12)
27	(14.14, 9.96)	(556.69, 392.12)
28	(14.14, 8.69)	(556.69, 342.12)
29	(14.14, 7.42)	(556.69, 292.12)
30	(14.14, 6.15)	(556.69, 242.12)
31	(14.14, 4.88)	(556.69, 192.12)

Figure 83 below details additional host board keep out area to achieve optimal RF performance with the CYBLE-01201X-X0 module.

Figure 83. Host Board Additional Keep Out Area for Optimal RF Performance



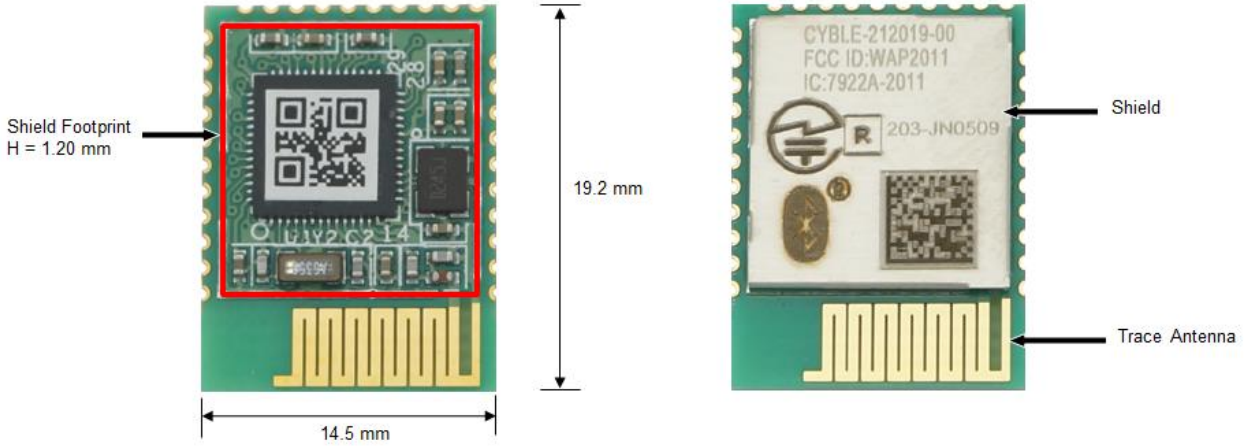
B.1.4 CYBLE-2120XX-XX

The CYBLE-2120XX-XX is a cost-optimized platform with 256-KB Flash designed to minimize system cost for applications that can utilize a larger module form factor. This platform is available in a two fully certified and qualified option (CYBLE-212019-00 for BLE v4.1, CYBLE-212020-01 for BLE v4.2), as well as a subset device that is not certified nor qualified with Bluetooth SIG (CYBLE-212023-10). The CYBLE-212019-00, CYBLE-212023-10, and CYBLE-212020-01 are pin-for-pin compatible with each other. All of these modules are also drop in compatible with the CYBLE-01201X-X0 modules. The CYBLE-212023-10 does not come with the RF metal shield on the top side of the module.

The mechanical drawing and reference layout information contained in this section is identical for both CYBLE-012011-00 and CYBLE-012012-10 modules.

Figure 84 shows a physical picture of the CYBLE-212019-00 EZ-BLE PRoC module. The form factor and image of the CYBLE-212020-01 is identical to the CYBLE-212019-00 with the exception of the laser marking on the top of the shield. The CYBLE-212023-10 module will appear as shown on the left side of Figure 84 with no shield.

Figure 84. CYBLE-212019-00 Module Top View (with and without Shield)

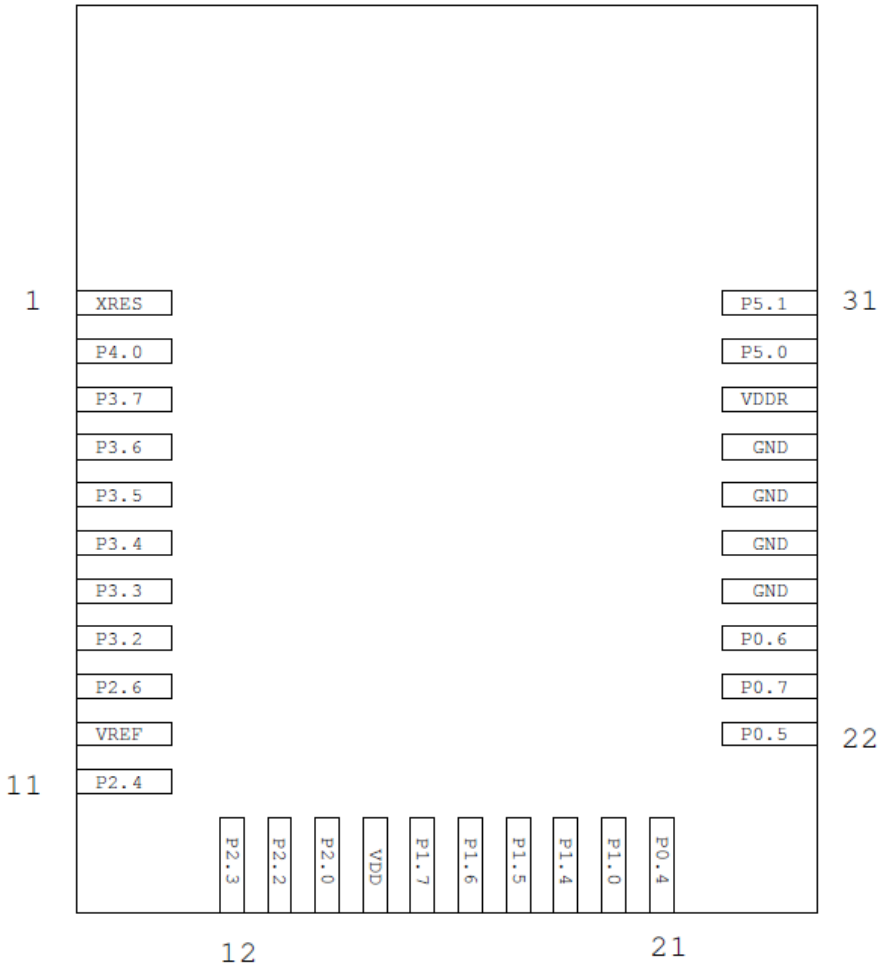


For more details on this module's dimensions, external component connections, and module placement recommendations, see the CYBLE-212019-00, CYBLE-212023-10 datasheet specification or the CYBLE-212020-01 datasheet specification.

B.1.4.1 Pinout and Functionality

The CYBLE-2120XX-XX module is designed to mount as a component on an end-product PCB. Only a portion of the available I/O of the PRoC BLE silicon device is exposed on the CYBLE-2120XX-XX module in order to minimize the module footprint size. The CYBLE-2120XX-XX module contains 31 connections on the bottom side of the module. Figure 85 details the bottom side connections available on the CYBLE-2120XX-XX module.

Figure 85. CYBLE-2120XX-XX Module Bottom View (Seen from Bottom)



A list of the available I/Os and supported functionality for each I/O of the CYBLE-2120XX-XX is shown in Table 12.

Table 12. CYBLE-2120XX-XX Module Available Connections and Functionality

Module Solder Pad Number	Silicon Port Pin	Functionality												
		UART	SPI	I2C	TCPWM[25, 26]	CapSense	LCD Drive	WCO Out	ECO_OUT[27]	SWD	SARMUX	OPAMP	LPCOMP	GPIO[28]
1	GND	Ground Connection												
1	XRES	External Reset Hardware Connection Input												
2	P4[0]	SCB1_RTS	SCB1_MOSI		TCPWM0_P	C_{MOD}	Yes							Yes

[25] Timer, counter, pulse-width modulator (PWM); configurable as 16-bit timer, counter, PWM blocks

[26] TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity. TCPWM connections on ports 4 and 5 are direct and can only be used with the specified TCPWM block and polarity specified above.

[27] External Crystal Oscillator Output from the device/module

[28] General Purpose Input/Output

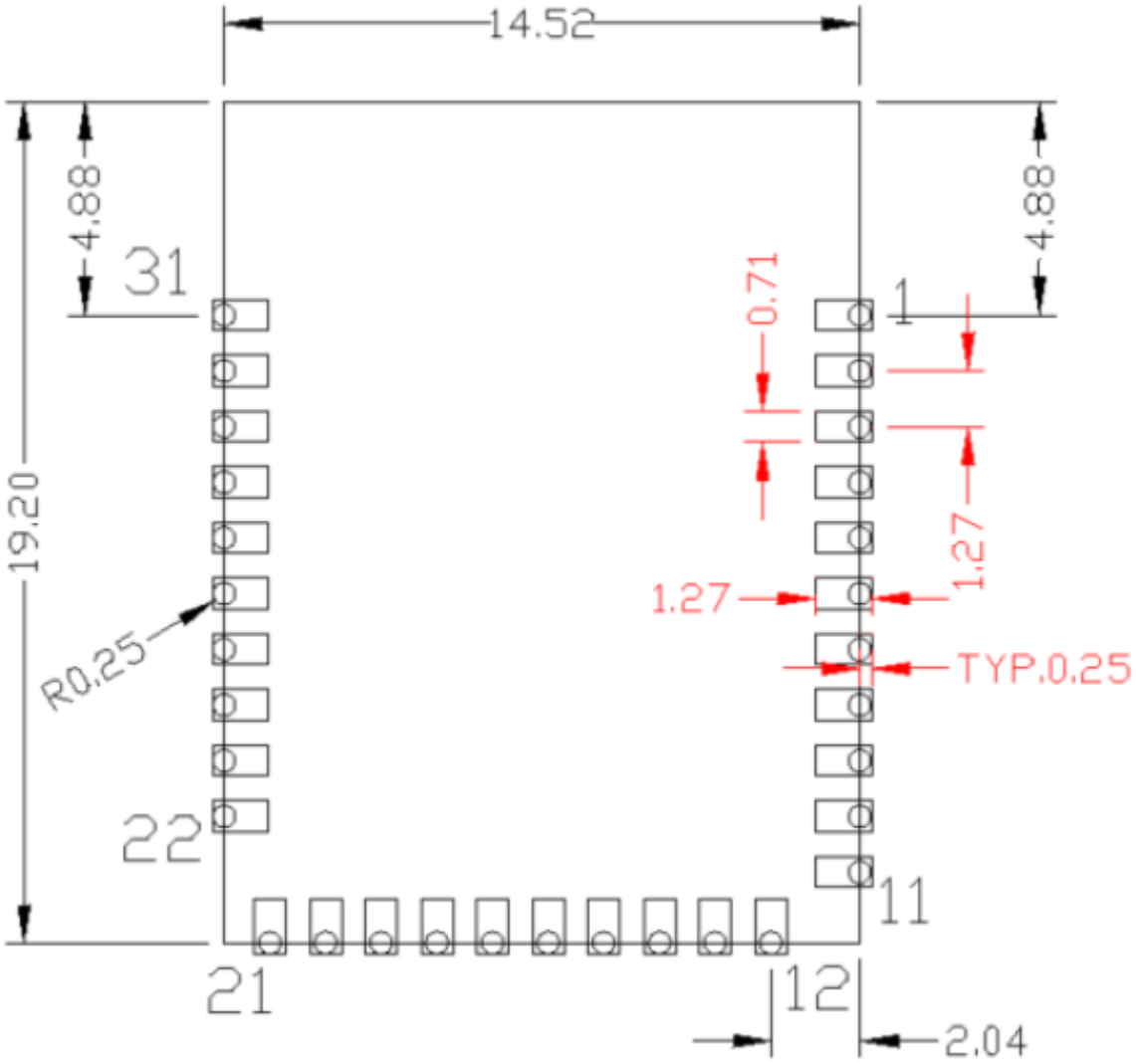
Module Solder Pad Number	Silicon Port Pin	Functionality												
		UART	SPI	I2C	TCPWM[25, 26]	CapSense	LCD Drive	WCO Out	ECO_OUT[27]	SWD	SARMUX	OPAMP	LPCOMP	GPIO[28]
3	P3[7]	SCB1_CTS			TCPWM	Sensor	Yes	Yes			Yes			Yes
4	P3[6]	SCB1_RTS			TCPWM	Sensor	Yes				Yes			Yes
5	P3[5]	SCB1_TX		SCB1_SCL	TCPWM	Sensor	Yes				Yes			Yes
6	P3[4]	SCB1_RX		SCB1_SDA	TCPWM	Sensor	Yes				Yes			Yes
7	P3[3]	SCB0_CTS			TCPWM	Sensor	Yes				Yes			Yes
8	P3[2]	SCB0_RTS			TCPWM	Sensor	Yes				Yes			Yes
9	P2[6]				TCPWM	Sensor	Yes							Yes
10	VREF	Reference Voltage Inputs (Optional)												
11	P2[4]				TCPWM	Sensor	Yes							Yes
12	P2[3]				TCPWM	Sensor	Yes	Yes						Yes
13	P2[2]		SCB0_SS3		TCPWM	Sensor	Yes							Yes
14	P2[0]		SCB0_SS1		TCPWM	Sensor	Yes							Yes
15	VDD	Digital and Analog Power Supply Input 1.71 to 5.5V												
16	P1[7]	SCB0_CTS	SCB0_SCLK		TCPWM	Sensor	Yes							Yes
17	P1[6]	SCB0_RTS	SCB0_SS0		TCPWM	Sensor	Yes							Yes
18	P1[5]	SCB0_TX	SCB0_MISO	SCB0_SCL	TCPWM	Sensor	Yes							Yes
19	P1[4]	SCB0_RX	SCB0_MOSI	SCB0_SDA	TCPWM	Sensor	Yes							Yes
20	P1[0]				TCPWM	Sensor	Yes		Yes					Yes
21	P0[4]	SCB0_RX	SCB0_MOSI	SCB0_SDA	TCPWM	Sensor	Yes		Yes					Yes
22	P0[5]	SCB0_TX	SCB0_MISO	SCB0_SCL	TCPWM	Sensor	Yes							Yes
23	P0[7]	SCB0_CTS	SCB0_SCLK		TCPWM	Sensor	Yes			SWDCLK[29]				Yes
24	P0[6]	SCB0_RTS	SCB0_SS0		TCPWM	Sensor	Yes			SWDIO[29]				Yes
25	GND	Ground Connection												
26	GND	Ground Connection												
27	GND	Ground Connection												
28	GND	Ground Connection												
29	VDDR	Radio Power Supply 1.9 V to 5.5 V												
30	P5[0]	SCB1_RX	SCB1_SS0	SCB1_SDA	TCPWM3_P	Sensor	Yes							Yes
31	P5[1]	SCB1_TX	SCB1_SCLK	SCB1_SCL	TCPWM3_N	Sensor	Yes		Yes					Yes

[29] SDWCLK and SWDIO connections can be multiplexed as the functional options listed in each of the respective rows and can be used for programming without the need to reconfigure the device I/O.

B.1.4.2 Host Recommended PCB Layout

To assist in the host PCB layout design for the CYBLE-2120XX-XX, Cypress provides three host PCB landing pattern reference drawings in Figure 86, Figure 87, Figure 88, and Table 13. Figure 86 provides a dimensioned view of the host PCB layout. Figure 87 provides the location to the center edge of each solder pad relative to the origin of the module (upper right PCB outline). Figure 88 and Table 13 provides the location to each solder pad center location for the host PCB layout. Dimensions shown are in mm unless otherwise stated.

Figure 86. Host Board Required PCB Layout Pattern (Dimensioned View)



Note: Pad length shown includes overhang of the host pad beyond the module pad outline. The minimum recommended pad length on the host PCB is 1.27 mm.

Figure 87. Host Board Required PCB Layout Pattern: To Pad Center Edge Relative to Origin

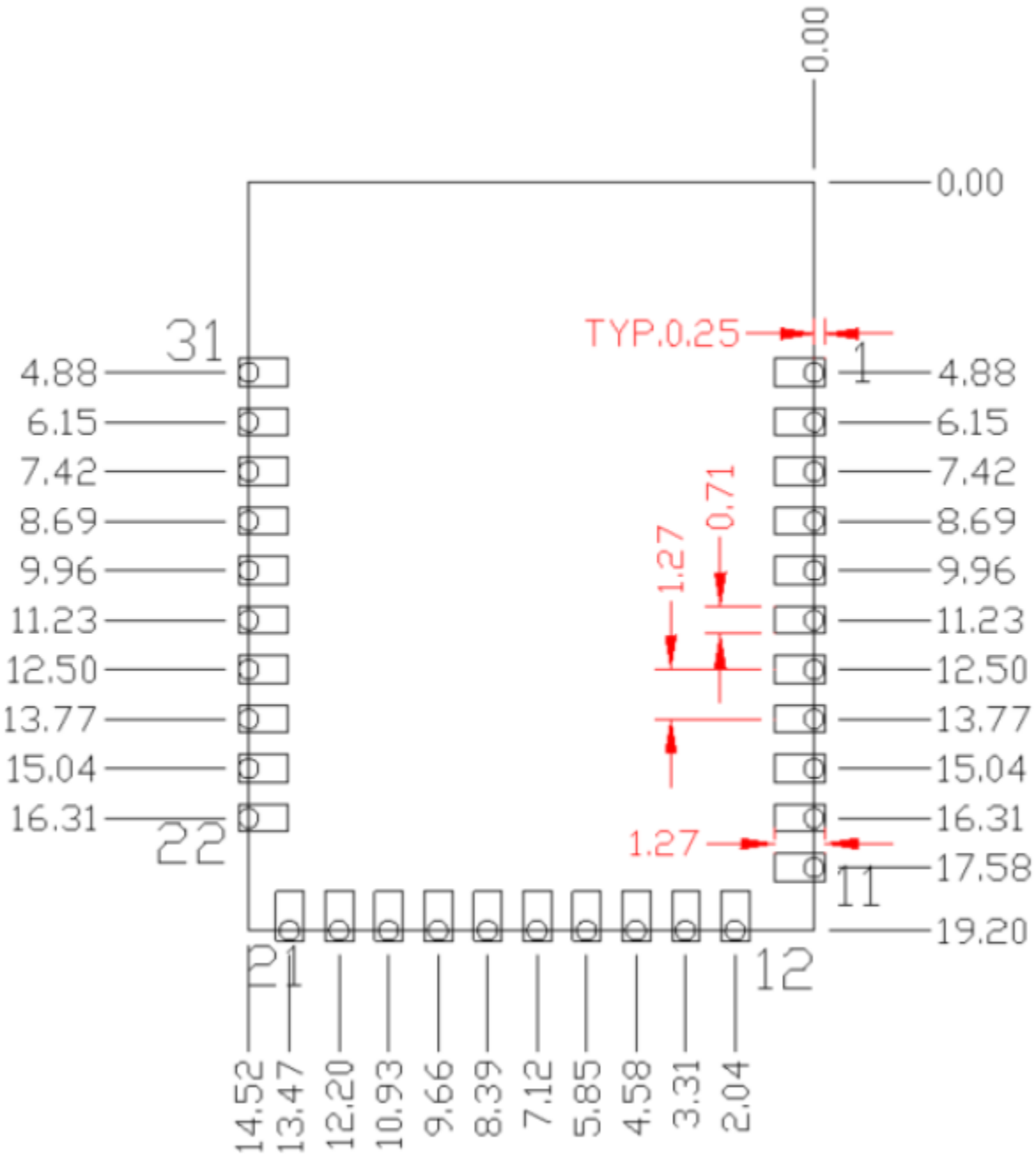


Figure 88. Host Board Required PCB Layout Pattern To Pad Center Relative to Origin

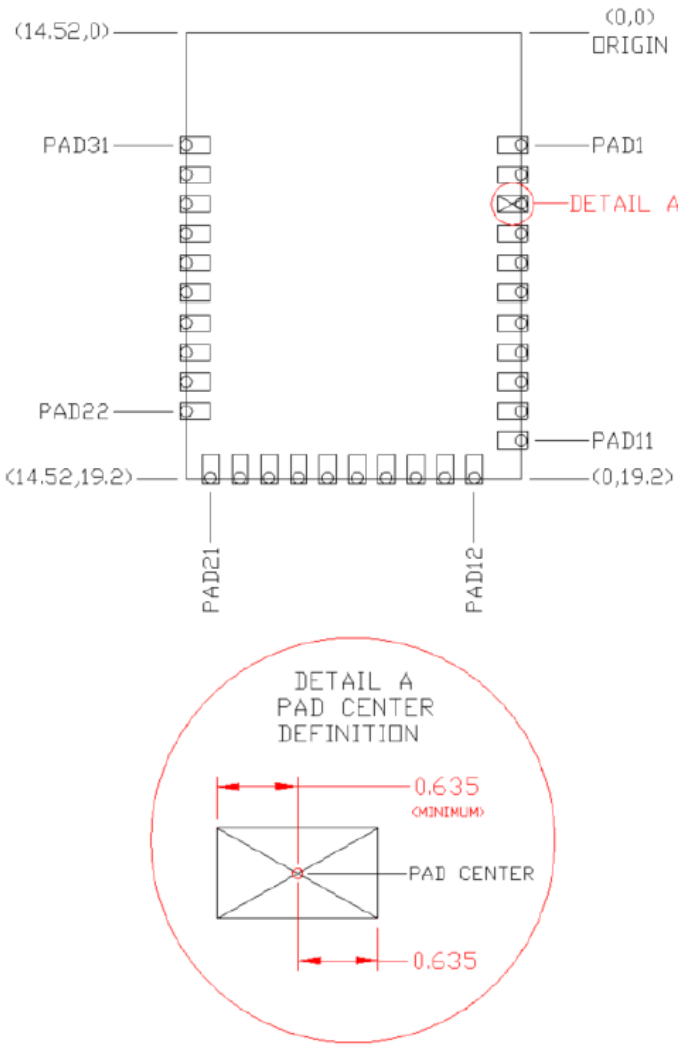
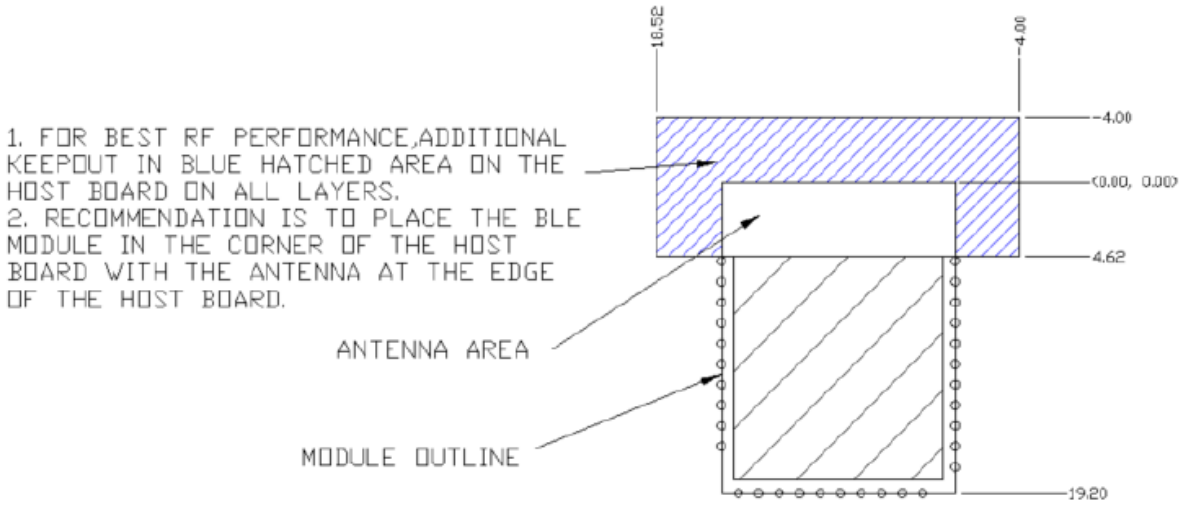


Table 13. Location to Pad Center from Origin (dimensions in mm and mils)

Solder Pad (Center of Pad)	Location (X,Y) from Origin (mm)	Location (X,Y) from Origin (mils)
1	(0.39, 4.88)	(15.35, 192.13)
2	(0.39, 6.15)	(15.35, 242.13)
3	(0.39, 7.42)	(15.35, 292.13)
4	(0.39, 8.69)	(15.35, 342.13)
5	(0.39, 9.96)	(15.35, 392.13)
6	(0.39, 11.23)	(15.35, 442.13)
7	(0.39, 12.50)	(15.35, 492.13)
8	(0.39, 13.77)	(15.35, 542.13)
9	(0.39, 15.04)	(15.35, 592.13)
10	(0.39, 16.31)	(15.35, 642.13)
11	(0.39, 17.58)	(15.35, 492.13)
12	(2.04, 18.82)	(80.31, 740.94)
13	(3.31 , 18.82)	(130.31 , 740.94)
14	(4.58 , 18.82)	(180.31 , 740.94)
15	(5.85 , 18.82)	(230.31 , 740.94)
16	(7.12 , 18.82)	(280.31 , 740.94)
17	(8.39 , 18.82)	(330.31 , 740.94)
18	(9.66 , 18.82)	(380.31 , 740.94)
19	(10.93 , 18.82)	(430.31 , 740.94)
20	(12.20 , 18.82)	(480.31 , 740.94)
21	(13.47, 18.82)	(530.31, 740.94)
22	(14.14, 16.31)	(556.69, 642.12)
23	(14.14, 15.04)	(556.69, 592.12)
24	(14.14, 13.77)	(556.69, 542.12)
25	(14.14, 12.50)	(556.69, 492.12)
26	(14.14, 11.23)	(556.69, 442.12)
27	(14.14, 9.96)	(556.69, 392.12)
28	(14.14, 8.69)	(556.69, 342.12)
29	(14.14, 7.42)	(556.69, 292.12)
30	(14.14, 6.15)	(556.69, 242.12)
31	(14.14, 4.88)	(556.69, 192.12)

Figure 89 below details additional host board keep out area to achieve optimal RF performance with the CYBLE-2120XX-XX module.

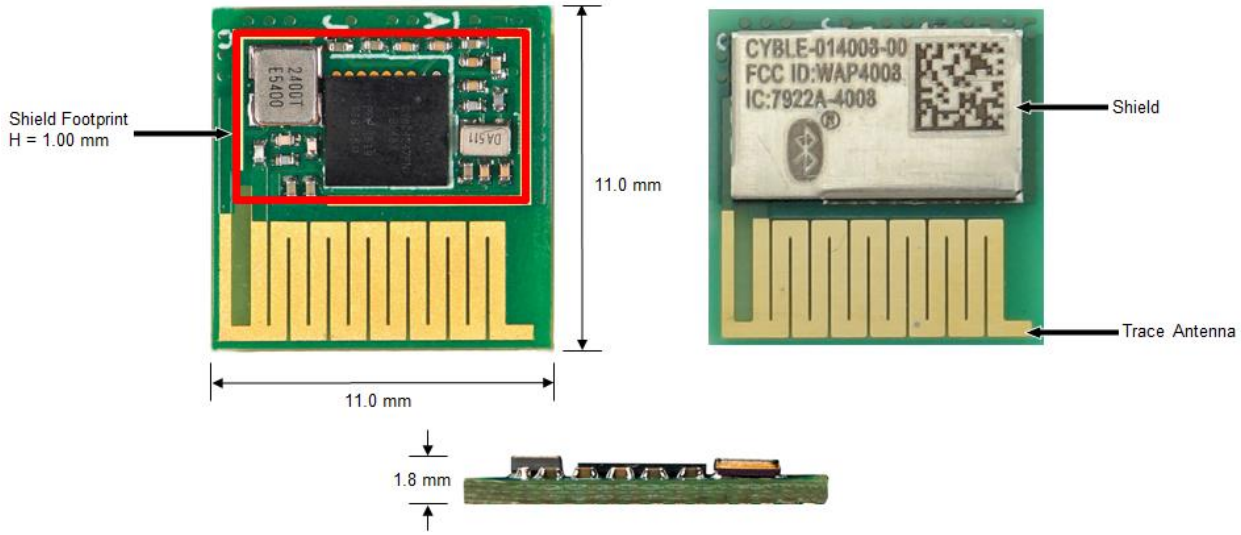
Figure 89. Host Board Additional Keep Out Area for Optimal RF Performance



B.1.5 CYBLE-014008-00

Figure 90 shows a physical picture of the CYBLE-014008-00 EZ-BLE PSoC module.

Figure 90. CYBLE-014008-00 Module Top View (with and without Shield) and Side View

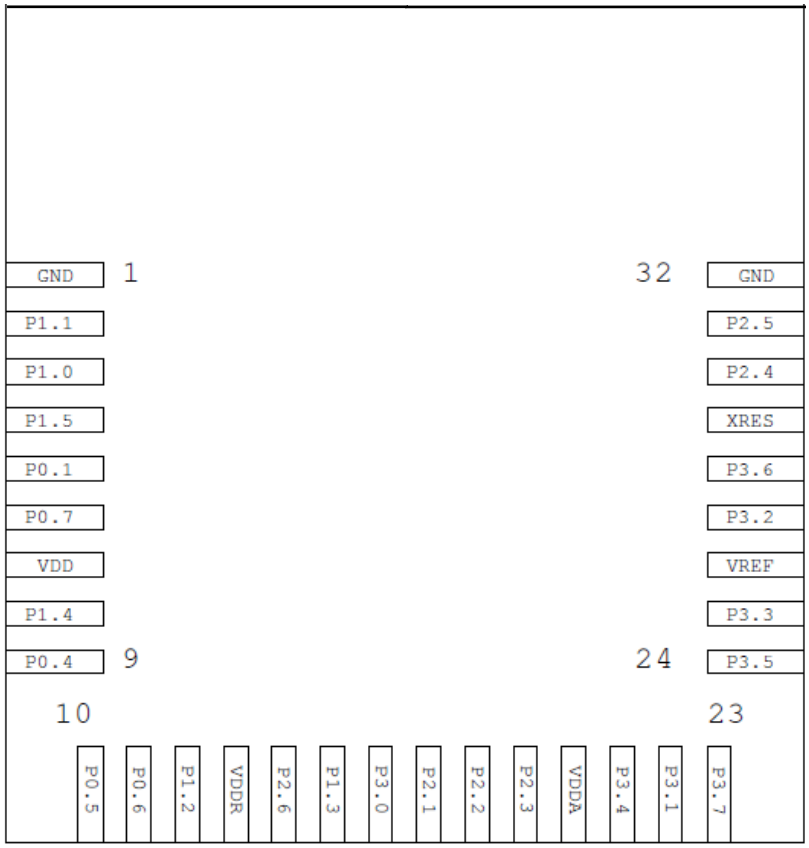


For more details on this module's dimensions, external component connections, and module placement recommendations, see the CYBLE-014008-00 datasheet specification.

B.1.5.1 Pinout and Functionality

The CYBLE-014008-00 module is designed to mount as a component on an end-product PCB. Only a portion of the available I/O of the PSoC BLE silicon device is exposed on the CYBLE-014008-00 module in order to minimize the module footprint size. The CYBLE-014008-00 module contains 32 connections on the bottom side of the module. Figure 91 details the bottom side connections available on the CYBLE-014008-00 module.

Figure 91. CYBLE-014008-00 Module Bottom View (Seen from Bottom)



A list of the available I/Os and supported functionality for each I/O of the CYBLE-014008-00 is shown in Table 14.

Table 14. CYBLE-014008-00 Module Available Connections and Functionality

Module Solder Pad Number	Silicon Port Pin	Functionality												
		UART	SPI	I2C	TCPWM[30, 31]	CapSense	LCD Drive	WCO Out	ECO OUT[32]	SWD	SARMUX	OPAMP	LP-COMP	GPIO[33]
1	GND	Ground Connection												
2	P1[1]		SCB1_SS1		TCPWM	Sensor	Yes					CTBm1_OA0_INN		Yes
3	P1[0]				TCPWM	Sensor	Yes		Yes			CTBm1_OA0_INP		Yes
4	P1[5]	SCB0_TX	SCB0_MISO	SCB0_SCL	TCPWM	Sensor	Yes					CTBm1_OA1_INP		Yes
5	P0[1]	SCB1_TX	SCB1_MISO	SCB1_SCL	TCPWM	Sensor	Yes						COMP0_INN	Yes

[30] Timer, counter, pulse-width modulator (PWM); configurable as 16-bit timer, counter, PWM blocks

[31] TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity. TCPWM connections on ports 4 and 5 are direct and can only be used with the specified TCPWM block and polarity specified above.

[32] External Crystal Oscillator Output from the device/module

[33] General Purpose Input/Output

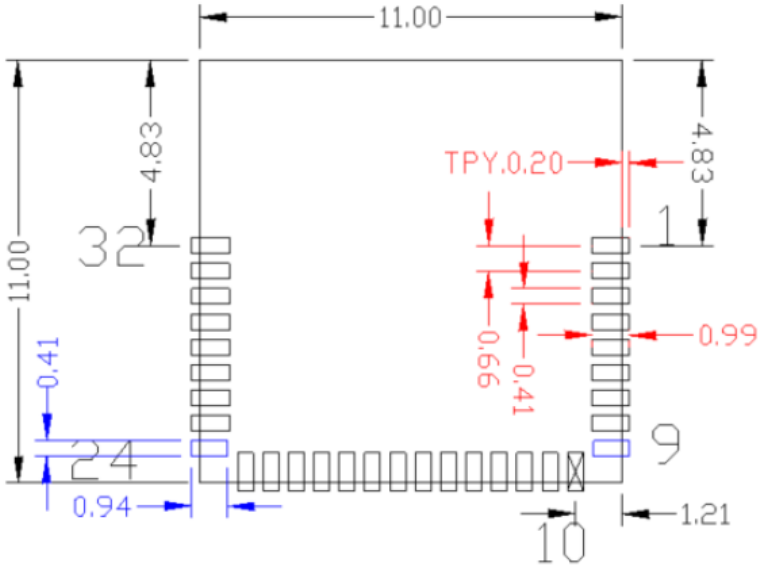
Module Solder Pad Number	Silicon Port Pin	Functionality												
		UART	SPI	I2C	TCPWM[30, 31]	CapSense	LCD Drive	WCO Out	ECO OUT[32]	SWD	SARMUX	OPAMP	LP-COMP	GPIO[33]
6	P0[7]	SCB0_CTS	SCB0_SCLK		TCPWM	Sensor	Yes			SWDCLK[34]				Yes
7	VDD	Digital Power Supply Input 1.71 to 5.5V												
8	P1[4]	SCB0_RX	SCB0_MOSI	SCB0_SDA	TCPWM	Sensor	Yes					CTBm1_OA1_INN		Yes
9	P0[4]	SCB0_RX	SCB0_MOSI	SCB0_SDA	TCPWM	Sensor	Yes		Yes				COMP1_INP	Yes
10	P0[5]	SCB0_TX	SCB0_MISO	SCB0_SCL	TCPWM	Sensor	Yes						COMP1_INN	Yes
11	P0[6]	SCB0_RTS	SCB0_SS0		TCPWM	Sensor	Yes			SWDIO[34]				Yes
12	P1[2]		SCB1_SS2		TCPWM	Sensor	Yes					CTBm1_OA0_OUT		Yes
13	VDDR	Radio Power Supply 1.9 V to 5.5 V												
14	P2[6]				TCPWM	Sensor	Yes					CTBm1_OA0_INP		Yes
15	P1[3]		SCB1_SS		TCPWM	Sensor	Yes					CTBm1_OA1_OUT		Yes
16	P3[0]	SCB0_RX		SCB0_SDA	TCPWM	Sensor	Yes				SARMUX_0			Yes
17	P2[1]		SCB0_SS2		TCPWM	Sensor	Yes					CTBm1_OA0_INN		Yes
18	P2[2]		SCB0_SS3		TCPWM	Sensor	Yes					CTBm1_OA0_OUT		Yes
19	P2[3]				TCPWM	Sensor	Yes	Yes				CTBm1_OA1_OUT		Yes
20	VDDA	Analog Power Supply Input 1.71 to 5.5V												
21	P3[4]	SCB1_RX		SCB1_SDA	TCPWM	Sensor	Yes				SARMUX_4			Yes
22	P3[1]	SCB0_TX		SCB0_SCL	TCPWM	Sensor	Yes				SARMUX_1			Yes
23	P3[7]	SCB1_CTS			TCPWM	Sensor	Yes	Yes			SARMUX_7			Yes
24	P3[5]	SCB1_TX		SCB1_SCL	TCPWM	Sensor	Yes				SARMUX_5			Yes
25	P3[3]	SCB0_CTS			TCPWM	Sensor	Yes				SARMUX_3			Yes
26	VREF	Reference Voltage Inputs (Optional)												
27	P3[2]	SCB0_RTS			TCPWM	Sensor	Yes				SARMUX_2			Yes
28	P3[6]	SCB1_RTS			TCPWM	Sensor	Yes				SARMUX_6			Yes
29	XRES	External Reset Hardware Connection Input												
30	P2[4]				TCPWM	Sensor	Yes					CTBm1_OA1_INN		Yes
31	P2[5]				TCPWM	Sensor	Yes					CTBm1_OA1_INP		Yes
32	GND	Ground Connection												

[34] SDWCLK and SWDIO connections can be multiplexed as the functional options listed in each of the respective rows and can be used for programming without the need to reconfigure the device I/O.

B.1.5.2 Host Recommended PCB Layout

To assist in the host PCB layout design for the CYBLE-014008-00, Cypress provides three host PCB reference drawings in Figure 92, Figure 93, and in Figure 94 and Table 15. Figure 92 provides a dimensions view of the host PCB layout. Figure 93 provides the location to the center edge of each solder pad relative to the origin of the module (upper right PCB outline). Figure 94 and Table 15. provide the location to each solder pad center location for the host PCB layout. Dimensions shown are in mm unless otherwise stated.

Figure 92. Host Board Required PCB Layout Pattern (Dimensioned View)



Note: Pad length shown includes overhang of the host pad beyond the module pad outline. The minimum recommended pad length on the host PCB is 0.99 mm.

Note: Pad 9 and Pad 24 have different dimensions than the rest of the connection pads (denoted in blue).

Figure 93. Host Board Required PCB Layout Pattern: To Pad Center Edge Relative to Origin

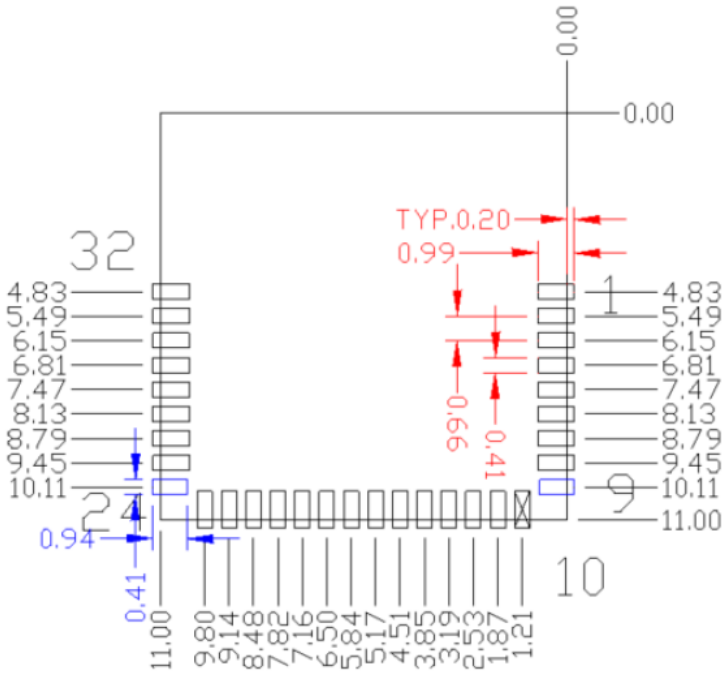


Figure 94. Host Board Required PCB Layout Pattern To Pad Center Relative to Origin

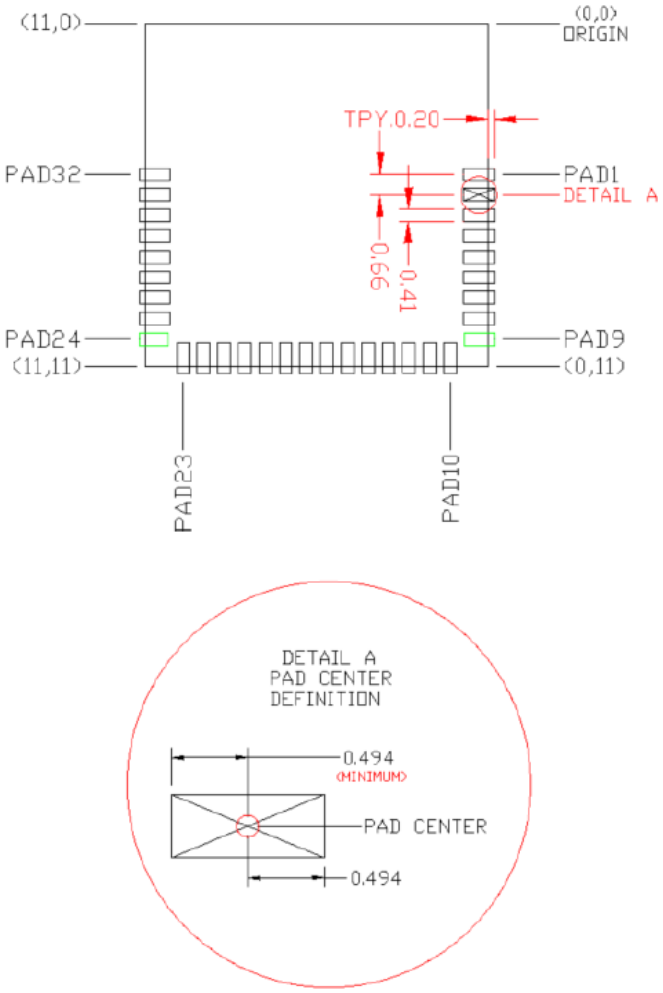
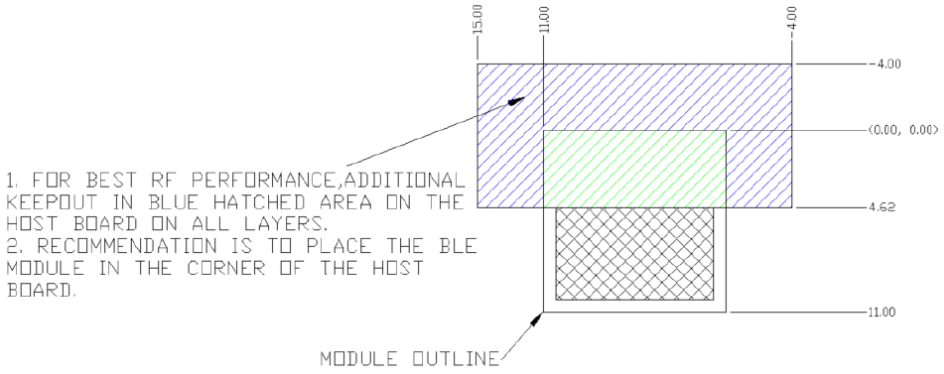


Table 15. Location to Pad Center from Origin (dimensions in mm and mils)

Solder Pad (Center of Pad)	Location (X,Y) from Origin (mm)	Location (X,Y) from Origin (mils)
1	(0.30, 4.83)	(11.81, 190.16)
2	(0.30, 5.49)	(11.81, 216.14)
3	(0.30, 6.15)	(11.81, 242.13)
4	(0.30, 6.81)	(11.81, 268.11)
5	(0.30, 7.47)	(11.81, 294.09)
6	(0.30, 8.13)	(11.81, 320.08)
7	(0.30, 8.79)	(11.81, 346.06)
8	(0.30, 9.45)	(11.81, 372.05)
9	(0.27, 10.11)	(10.63, 398.03)
10	(1.21, 10.70)	(47.64, 421.26)
11	(1.87, 10.70)	(73.62, 421.26)
12	(2.53, 10.70)	(99.61, 421.26)
13	(3.19, 10.70)	(125.59, 421.26)
14	(3.85, 10.70)	(151.57, 421.26)
15	(4.51, 10.70)	(177.56, 421.26)
16	(5.17, 10.70)	(203.54, 421.26)
17	(5.84, 10.70)	(229.92, 421.26)
18	(6.50, 10.70)	(255.91, 421.26)
19	(7.16, 10.70)	(281.89, 421.26)
20	(7.82, 10.70)	(307.87, 421.26)
21	(8.48, 10.70)	(333.86, 421.26)
22	(9.14, 10.70)	(359.84, 421.26)
23	(9.80, 10.70)	(385.83, 421.26)
24	(10.73, 10.11)	(422.44, 398.03)
25	(10.70, 9.45)	(421.26, 372.05)
26	(10.70, 8.79)	(421.26, 346.06)
27	(10.70, 8.13)	(421.26, 320.08)
28	(10.70, 7.47)	(421.26, 294.09)
29	(10.70, 6.81)	(421.26, 268.11)
30	(10.70, 6.15)	(421.26, 242.13)
31	(10.70, 5.49)	(421.26, 216.14)
32	(10.70, 4.83)	(421.26, 190.16)

Figure 95 below details additional host board keep out area to achieve optimal RF performance with the CYBLE-014008-00 module.

Figure 95. Host Board Additional Keep Out Area for Optimal RF Performance

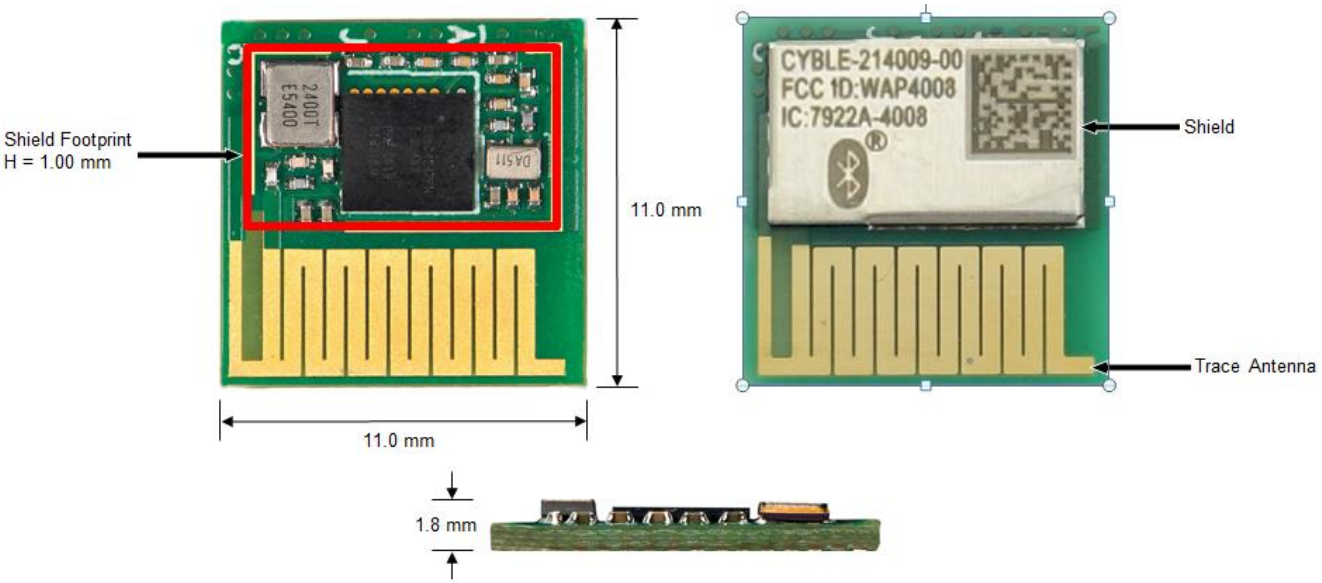


B.1.6 CYBLE-2140XX-0X

The CYBLE-2140XX-0X includes the CYBLE-214009-00 and CYBLE-214015-01 modules. The only difference between these two modules is Bluetooth specification v4.1 (CYBLE-214009-00) and Bluetooth specification v4.2 (CYBLE-214015-01). The CYBLE-2140XX-0X is drop-in compatible with the CYBLE-014008-00 module. The CYBLE-2140XX-0X is a flash and SRAM upgrade to the CYBLE-014008-00, moving from 128-KB flash and 16-KB SRAM to 256-KB flash and 32-KB SRAM, with the added option of moving to BLE specification v4.2 with the CYBLE-214015-01.

Figure 96 shows a physical picture of the CYBLE-214009-00 EZ-BLE PSoC module. The form and image of the CYBLE-214015-01 is identical to the figure below, with the exception of the top side laser marking.

Figure 96. CYBLE-214009-00 Module Top View (with and without Shield) and Side View

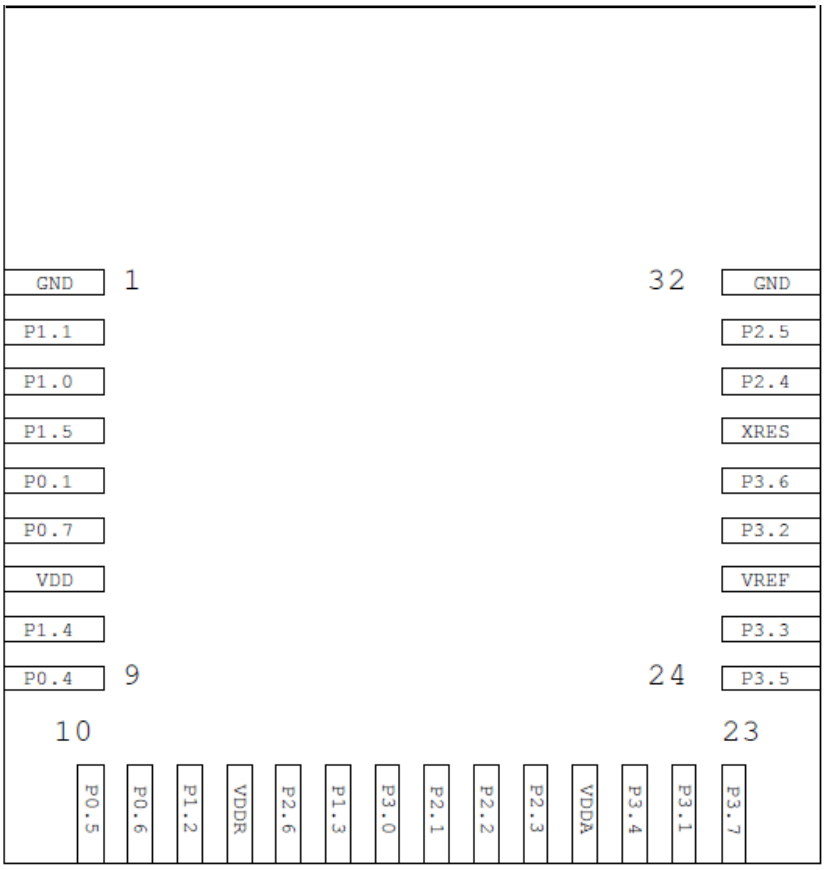


For more details on this module's dimensions, external component connections, and module placement recommendations, see the CYBLE-214009-00 datasheet specification or the CYBLE-214015-01 datasheet specification.

B.1.6.1 Pinout and Functionality

The CYBLE-2140XX-0X module is designed to mount as a component on an end-product PCB. Only a portion of the available I/O of the PSoC BLE silicon device is exposed on the CYBLE-2140XX-0X module in order to minimize the module footprint size. The CYBLE-2140XX-0X module contains 32 connections on the bottom side of the module. Figure 97 details the bottom side connections available on the CYBLE-2140XX-0X module.

Figure 97. CYBLE-2140XX-0X Module Bottom View (Seen from Bottom)



A list of the available I/Os and supported functionality for each I/O of the CYBLE-2140XX-0X is shown in Table 16.

Table 16. CYBLE-2140XX-0X Module Available Connections and Functionality

Module Solder Pad Number	Silicon Port Pin	Functionality												
		UART	SPI	I2C	TCPWM[35, 36]	CapSense	LCD Drive	WCO Out	ECO OUT[37]	SWD	SARMUX	OPAMP	LP-COMP	GPIO[38]
1	GND	Ground Connection												
2	P1[1]		SCB1_SS1		TCPWM	Sensor	Yes					CTBm1_OA0_INN		Yes
3	P1[0]				TCPWM	Sensor	Yes		Yes			CTBm1_OA0_INP		Yes
4	P1[5]	SCB0_TX	SCB0_MISO	SCB0_SCL	TCPWM	Sensor	Yes					CTBm1_OA1_INP		Yes
5	P0[1]	SCB1_TX	SCB1_MISO	SCB1_SCL	TCPWM	Sensor	Yes						COMP0_INN	Yes

[35] Timer, counter, pulse-width modulator (PWM); configurable as 16-bit timer, counter, PWM blocks

[36] TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity. TCPWM connections on ports 4 and 5 are direct and can only be used with the specified TCPWM block and polarity specified above.

[37] External Crystal Oscillator Output from the device/module

[38] General Purpose Input/Output

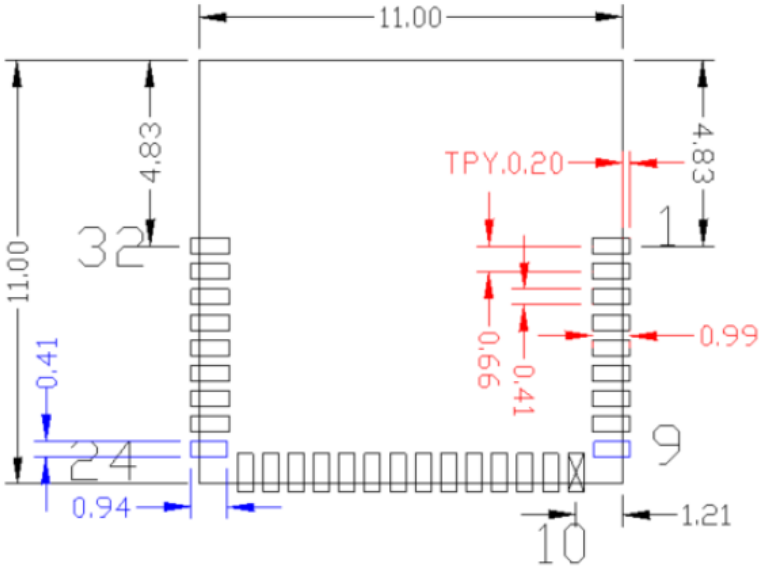
Module Solder Pad Number	Silicon Port Pin	Functionality												
		UART	SPI	I2C	TCPWM[35, 36]	CapSense	LCD Drive	WCO Out	ECO OUT[37]	SWD	SARMUX	OPAMP	LP-COMP	GPIO[38]
6	P0[7]	SCB0_CTS	SCB0_SCLK		TCPWM	Sensor	Yes			SWDCLK[39]				Yes
7	VDD	Digital Power Supply Input 1.71 to 5.5V												
8	P1[4]	SCB0_RX	SCB0_MOSI	SCB0_SDA	TCPWM	Sensor	Yes					CTBm1_OA1_INN		Yes
9	P0[4]	SCB0_RX	SCB0_MOSI	SCB0_SDA	TCPWM	Sensor	Yes		Yes				COMP1_INP	Yes
10	P0[5]	SCB0_TX	SCB0_MISO	SCB0_SCL	TCPWM	Sensor	Yes						COMP1_INN	Yes
11	P0[6]	SCB0_RTS	SCB0_SS0		TCPWM	Sensor	Yes			SWDIO[39]				Yes
12	P1[2]		SCB1_SS2		TCPWM	Sensor	Yes					CTBm1_OA0_OUT		Yes
13	VDDR	Radio Power Supply 1.9 V to 5.5 V												
14	P2[6]				TCPWM	Sensor	Yes					CTBm1_OA0_INP		Yes
15	P1[3]		SCB1_SS		TCPWM	Sensor	Yes					CTBm1_OA1_OUT		Yes
16	P3[0]	SCB0_RX		SCB0_SDA	TCPWM	Sensor	Yes				SARMUX_0			Yes
17	P2[1]		SCB0_SS2		TCPWM	Sensor	Yes					CTBm1_OA0_INN		Yes
18	P2[2]		SCB0_SS3		TCPWM	Sensor	Yes					CTBm1_OA0_OUT		Yes
19	P2[3]				TCPWM	Sensor	Yes	Yes				CTBm1_OA1_OUT		Yes
20	VDDA	Analog Power Supply Input 1.71 to 5.5V												
21	P3[4]	SCB1_RX		SCB1_SDA	TCPWM	Sensor	Yes				SARMUX_4			Yes
22	P3[1]	SCB0_TX		SCB0_SCL	TCPWM	Sensor	Yes				SARMUX_1			Yes
23	P3[7]	SCB1_CTS			TCPWM	Sensor	Yes	Yes			SARMUX_7			Yes
24	P3[5]	SCB1_TX		SCB1_SCL	TCPWM	Sensor	Yes				SARMUX_5			Yes
25	P3[3]	SCB0_CTS			TCPWM	Sensor	Yes				SARMUX_3			Yes
26	VREF	Reference Voltage Inputs (Optional)												
27	P3[2]	SCB0_RTS			TCPWM	Sensor	Yes				SARMUX_2			Yes
28	P3[6]	SCB1_RTS			TCPWM	Sensor	Yes				SARMUX_6			Yes
29	XRES	External Reset Hardware Connection Input												
30	P2[4]				TCPWM	Sensor	Yes					CTBm1_OA1_INN		Yes
31	P2[5]				TCPWM	Sensor	Yes					CTBm1_OA1_INP		Yes
32	GND	Ground Connection												

[39] SDWCLK and SWDIO connections can be multiplexed as the functional options listed in each of the respective rows and can be used for programming without the need to reconfigure the device I/O.

B.1.6.2 Host Recommended PCB Layout

To assist in the host PCB layout design for the CYBLE-2140XX-0X, Cypress provides three host PCB reference drawings in Figure 98, Figure 99, and in Figure 100 and Table 17. Figure 98 provides a dimensions view of the host PCB layout. Figure 99 provides the location to the center edge of each solder pad relative to the origin of the module (upper right PCB outline). Figure 100 and Table 17. provide the location to each solder pad center location for the host PCB layout. Dimensions shown are in mm unless otherwise stated.

Figure 98. Host Board Required PCB Layout Pattern (Dimensioned View)



Note: Pad length shown includes overhang of the host pad beyond the module pad outline. The minimum recommended pad length on the host PCB is 0.99 mm.

Note: Pad 9 and Pad 24 have different dimensions than the rest of the connection pads (denoted in blue).

Figure 99. Host Board Required PCB Layout Pattern: To Pad Center Edge Relative to Origin

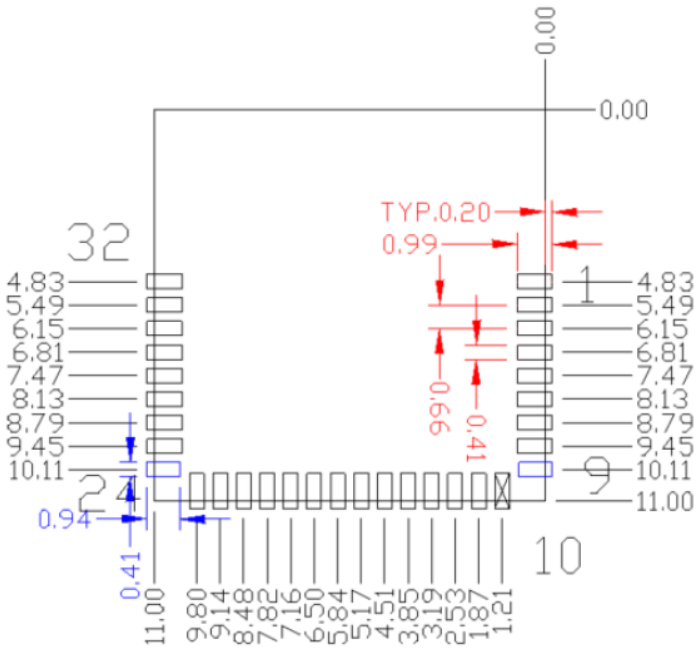


Figure 100. Host Board Required PCB Layout Pattern To Pad Center Relative to Origin

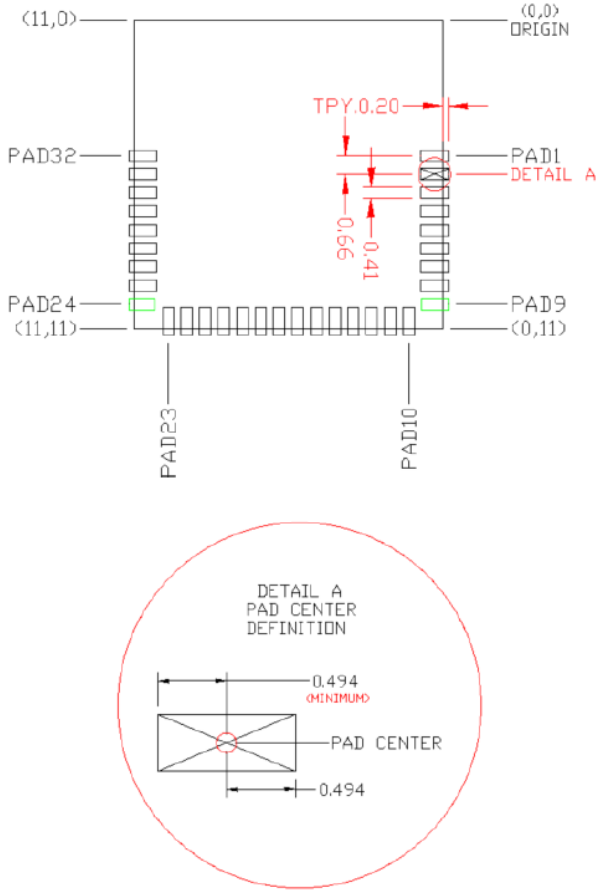
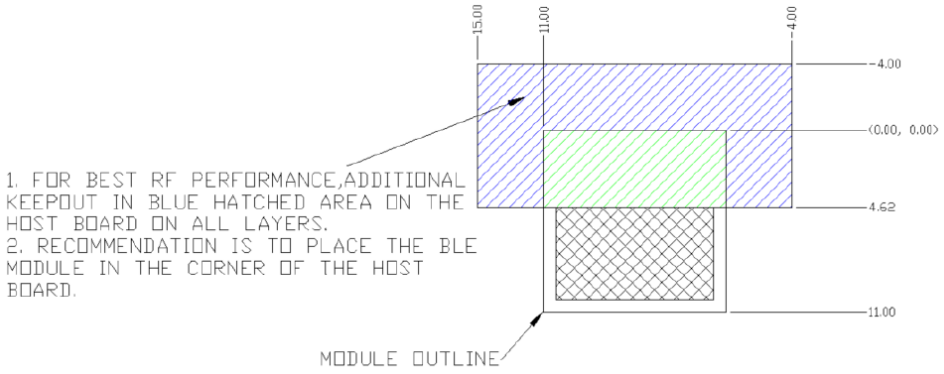


Table 17. Location to Pad Center from Origin (dimensions in mm and mils)

Solder Pad (Center of Pad)	Location (X,Y) from Origin (mm)	Location (X,Y) from Origin (mils)
1	(0.30, 4.83)	(11.81, 190.16)
2	(0.30, 5.49)	(11.81, 216.14)
3	(0.30, 6.15)	(11.81, 242.13)
4	(0.30, 6.81)	(11.81, 268.11)
5	(0.30, 7.47)	(11.81, 294.09)
6	(0.30, 8.13)	(11.81, 320.08)
7	(0.30, 8.79)	(11.81, 346.06)
8	(0.30, 9.45)	(11.81, 372.05)
9	(0.27, 10.11)	(10.63, 398.03)
10	(1.21, 10.70)	(47.64, 421.26)
11	(1.87, 10.70)	(73.62, 421.26)
12	(2.53, 10.70)	(99.61, 421.26)
13	(3.19, 10.70)	(125.59, 421.26)
14	(3.85, 10.70)	(151.57, 421.26)
15	(4.51, 10.70)	(177.56, 421.26)
16	(5.17, 10.70)	(203.54, 421.26)
17	(5.84, 10.70)	(229.92, 421.26)
18	(6.50, 10.70)	(255.91, 421.26)
19	(7.16, 10.70)	(281.89, 421.26)
20	(7.82, 10.70)	(307.87, 421.26)
21	(8.48, 10.70)	(333.86, 421.26)
22	(9.14, 10.70)	(359.84, 421.26)
23	(9.80, 10.70)	(385.83, 421.26)
24	(10.73, 10.11)	(422.44, 398.03)
25	(10.70, 9.45)	(421.26, 372.05)
26	(10.70, 8.79)	(421.26, 346.06)
27	(10.70, 8.13)	(421.26, 320.08)
28	(10.70, 7.47)	(421.26, 294.09)
29	(10.70, 6.81)	(421.26, 268.11)
30	(10.70, 6.15)	(421.26, 242.13)
31	(10.70, 5.49)	(421.26, 216.14)
32	(10.70, 4.83)	(421.26, 190.16)

Figure 101 below details additional host board keep out area to achieve optimal RF performance with the CYBLE-2140XX-0X module.

Figure 101. Host Board Additional Keep Out Area for Optimal RF Performance



B.1.7 CYBLE-2X20XX-X1 XR

The CYBLE-2X20XX-X1 is an EZ-BLE PRoC module providing extended communication range (up to 400 meters line-of-sight). The CYBLE-2X20XX-X1 family contains three modules, each providing alternative antenna connection options:

- CYBLE-212006-01: Provides an integrated PCB Trace Antenna.
- CYBLE-202007-01: Provides a micro-FL (u.FL) connector for use with an external antenna.
- CYBLE-202013-11: Provides a module solder pad RF output connection to an external antenna.

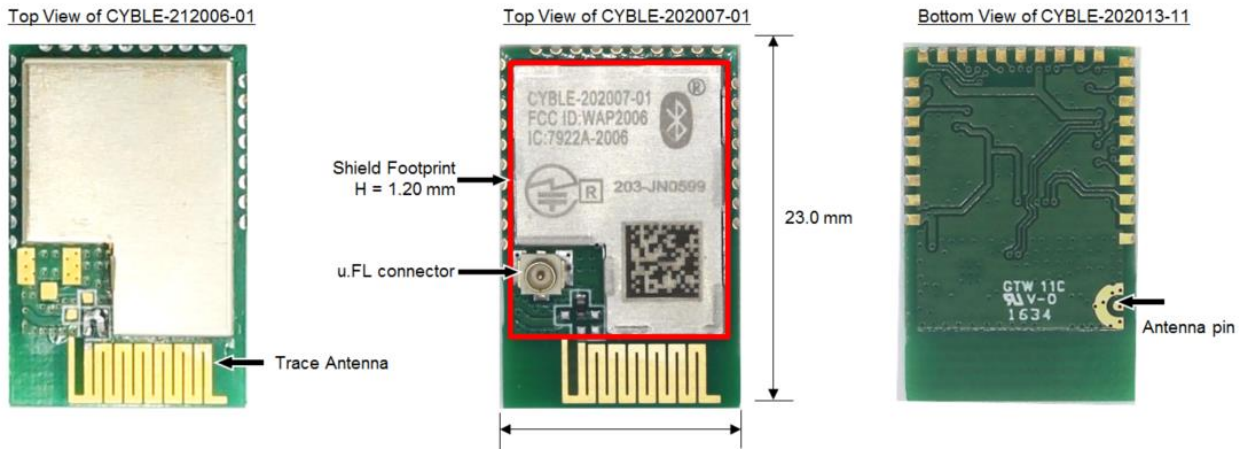
Note: CYBLE-202007-01 is certified for regulatory compliance, however, external antenna gain requirements must be met for the certification of the module to be valid. Please refer to the datasheet specification for details on the approved antennas used for this design.

Note: CYBLE-202013-11 is not certified for regulatory compliance, but is qualified with Bluetooth SIG for specification v4.2. An antenna matching network (AMN) is required to be present off-module in order to achieve desired performance. For reference AMN circuit designs, please refer to the datasheet specification.

In order to operate the CYBLE-2X20XX-X1 modules in extended range mode, please refer to the Process for Enabling and Activating Power Amplifier/Low-Noise Amplifier in this section of the application note.

Figure 102 shows a physical picture of the top side of the CYBLE-212006-01, the top side of the CYBLE-202007-01, and the backside view of the CYBLE-202013-11 modules.

Figure 102. CYBLE-2X20XX-X1 Module Images (with and without Shield)

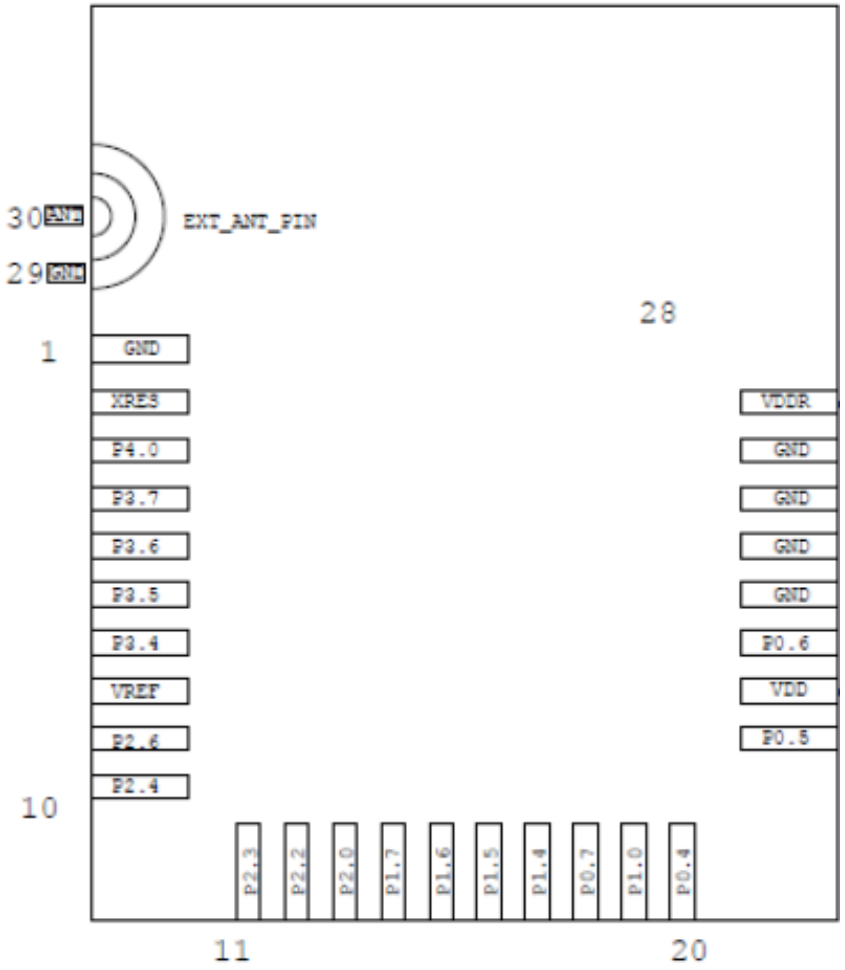


For more details on this module's dimensions, external component connections, and module placement recommendations, see the CYBLE-2X0XX-X1 datasheet specification.

B.1.7.1 Pinout and Functionality

The CYBLE-2X20XX-X1 module is designed to mount as a component on an end-product PCB. Only a portion of the available I/O of the BLE silicon device is exposed on the CYBLE-2X20XX-X1 module in order to minimize the module footprint size. The CYBLE-2X20XX-X1 module contains 30 connections on the bottom side of the module. Figure 103 details the bottom side connections available on the CYBLE-2X20XX-X1 module.

Figure 103. CYBLE-2X20XX-X1 Module Bottom View (Seen from Bottom)



A list of the available I/Os and supported functionality for each I/O of the CYBLE-2X20XX-X1 is shown in Table 18.

Table 18. CYBLE-2X20XX-X1 Module Available Connections and Functionality

Module Solder Pad Number	Silicon Port Pin	Functionality												
		UART	SPI	I2C	TCPWM[40, 41]	CapSense	LCD Drive	WCO Out	ECO OUT[42]	SWD	SARMUX	OPAMP	LP-COMP	GPIO[43]
1	GND	Ground Connection												
2	XRES	External Reset Hardware Connection Input												
3	P4[0]	SCB1_RTS	SCB1_MOSI		TCPWM0_P	C_{MOD}	Yes							Yes
4	P3[7]	SCB1_CTS			TCPWM	Sensor	Yes	Yes			SARMUX_7			Yes

[40] Timer, counter, pulse-width modulator (PWM); configurable as 16-bit timer, counter, PWM blocks

[41] TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity. TCPWM connections on ports 4 and 5 are direct and can only be used with the specified TCPWM block and polarity specified above.

[42] External Crystal Oscillator Output from the device/module

[43] General Purpose Input/Output

Module Solder Pad Number	Silicon Port Pin	Functionality												
		UART	SPI	I2C	TCPWM[40, 41]	CapSense	LCD Drive	WCO Out	ECO OUT[42]	SWD	SARMUX	OPAMP	LP-COMP	GPIO[43]
5	P3[6]	SCB1_RTS			TCPWM	Sensor	Yes				SARMUX_6			Yes
6	P3[5]	SCB1_TX		SCB1_SCL	TCPWM	Sensor	Yes				SARMUX_5			Yes
7	P3[4]	SCB1_RX		SCB1_SDA	TCPWM	Sensor	Yes				SARMUX_4			Yes
8	VREF	Reference Voltage Inputs (Optional)												
9	P2[6]				TCPWM	Sensor	Yes							Yes
10	P2[4]				TCPWM	Sensor	Yes							Yes
11	P2[3]				TCPWM	Sensor	Yes	Yes						Yes
12	P2[2]		SCB0_SS3		TCPWM	Sensor	Yes							Yes
13	P2[0]		SCB0_SS1		TCPWM	Sensor	Yes							Yes
14	P1[7]	SCB0_CTS	SCB0_SCLK		TCPWM	Sensor	Yes							Yes
15	P1[6]	SCB0_RTS	SCB0_SS0		TCPWM	Sensor	Yes							Yes
16	P1[5]	SCB0_TX	SCB0_MISO	SCB0_SCL	TCPWM	Sensor	Yes							Yes
17	P1[4]	SCB0_RX	SCB0_MOSI	SCB0_SDA	TCPWM	Sensor	Yes							Yes
18	P0[7]	SCB0_CTS	SCB0_SCLK		TCPWM	Sensor	Yes			SWDCLK[44]				Yes
19	P1[0]				TCPWM	Sensor	Yes		Yes					Yes
20	P0[4]	SCB0_RX	SCB0_MOSI	SCB0_SDA	TCPWM	Sensor	Yes		Yes					Yes
21	P0[5]	SCB0_TX	SCB0_MISO	SCB0_SCL	TCPWM	Sensor	Yes							Yes
22	VDD	Digital Power Supply Input 1.71 to 3.6V												
23	P0[6]	SCB0_RTS	SCB0_SS0		TCPWM	Sensor	Yes			SWDIO[45]				Yes
24	GND	Ground												
25	GND	Ground												
26	GND	Ground												
27	GND	Ground												
28	VDDR	Radio Power Supply 2.0 V to 3.6 V												
29	GND	RF Ground Connection for use with CYBLE-202013-11 only; No Connect for CYBLE-212006-01 and CYBLE-202007-01												
30	ANT	RF Pin to External Antenna for use with CYBLE-202013-11 only; No Connect for CYBLE-212006-01 and CYBLE-202007-01												

[44] SDWCLK and SWDIO connections can be multiplexed as the functional options listed in each of the respective rows and can be used for programming without the need to reconfigure the device I/O.

B.1.7.2 Process for Enabling and Activating Power Amplifier/Low-Noise Amplifier

The CYBLE-2X20XX-X1 modules come with an integrated Power Amplifier/Low Noise Amplifier to allow for extended communication range of up to 400 meters full line-of-sight. This section describes the firmware steps required to enable extended range operation of the CYBLE-2X20XX-X1 modules.

The Skyworks RFX2401C PA/LNA is controlled by PRoC BLE silicon and uses two GPIOs:

1. One GPIO to control the PA enable (P3[2]). The PA enable GPIO is controlled directly by the BLE Link Layer.
2. One GPIO to control the LNA enable (P3[3]). The LNA enable GPIO is controlled directly by the BLE Link Layer.

Ensure that the PRoC BLE silicon device “Adv/Scan TX Power Level (dBm)” and “Connection TX Power Level (dBm)” in the BLE Component are both set to -12 dBm, which is the silicon output power level that this module has been certified for (total output power of the module is +7.5 dBm).

To enable the extended range functionality, follow the steps outlined below.

- Open your project's *main.c* file and write the following code to define the register at the top of the code:

```
/* define the test register to switch the PA/LNA hardware control pins */
#define     CYREG_SRSS_TST_DDFT_CTRL    0x40030008
```

- Locate/add the event “CYBLE_EVT_STACK_ON" in the application code and insert the following two lines of code to enable the Skyworks RFX2401C.

```
/* Mandatory events to be handled by Find Me Target design */
case CYBLE_EVT_STACK_ON:
   /* Configure the Link Layer to automatically switch PA
    * control pin P3[2] and LNA control pin P3[3] */
   CY_SET_XTND_REG32((void CYFAR *)(CYREG_BLE_BLESS_RF_CONFIG), 0x0331);
   CY_SET_XTND_REG32((void CYFAR *)(CYREG_SRSS_TST_DDFT_CTRL),
0x80000302);
```

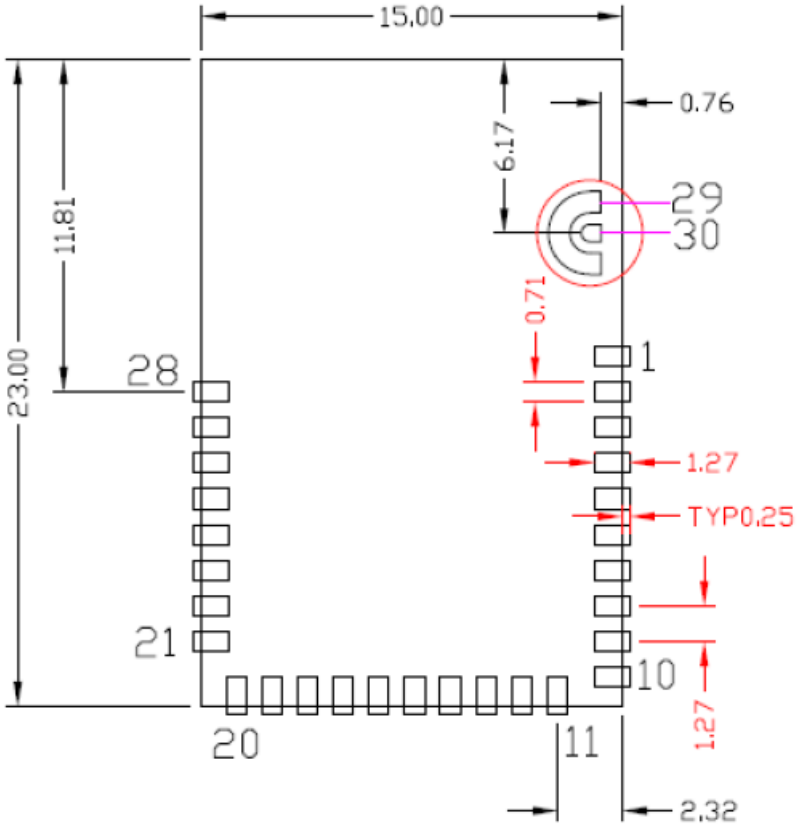
B.1.7.3 Low Power Operation

The CYBLE-2X20XX-X1 module is already optimized for low power operation when in high output power, high gain mode. The Cypress BLE Link Layer will automatically enable TX high power operation, as well as RX high gain operation. When the radio TX or RX operation is not in use (that is, Sleep), the PA/LNA will be set to shutdown mode by the BLE Link Layer. This occurs during sleep modes of the Cypress PRoC BLE silicon device.

B.1.7.4 Host Recommended PCB Layout

To assist in the host PCB layout design for the CYBLE-2X20XX-X1, Cypress provides three host PCB reference drawings in Figure 104, Figure 105, and in Figure 106 and Table 19. Figure 104 provides a dimensions view of the host PCB layout. Figure 105 provides the location to the center edge of each solder pad relative to the origin of the module (upper right PCB outline). Figure 106 and Table 19 provide the location to each solder pad center location for the host PCB layout. Dimensions shown are in mm unless otherwise stated.

Figure 104. Host Board Required PCB Layout Pattern (Dimensioned View)



Note: Pad length shown includes overhang of the host pad beyond the module pad outline. The minimum recommended pad length on the host PCB is 1.27 mm.

Figure 105. Host Board Required PCB Layout Pattern: To Pad Center Edge Relative to Origin

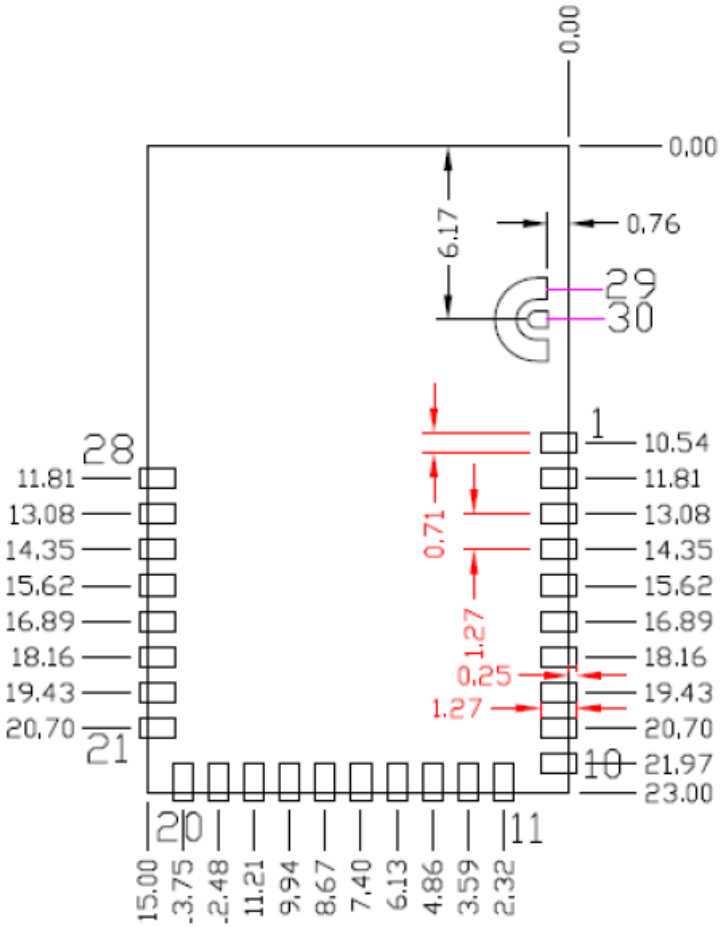


Figure 106. Host Board Required PCB Layout Pattern To Pad Center Relative to Origin

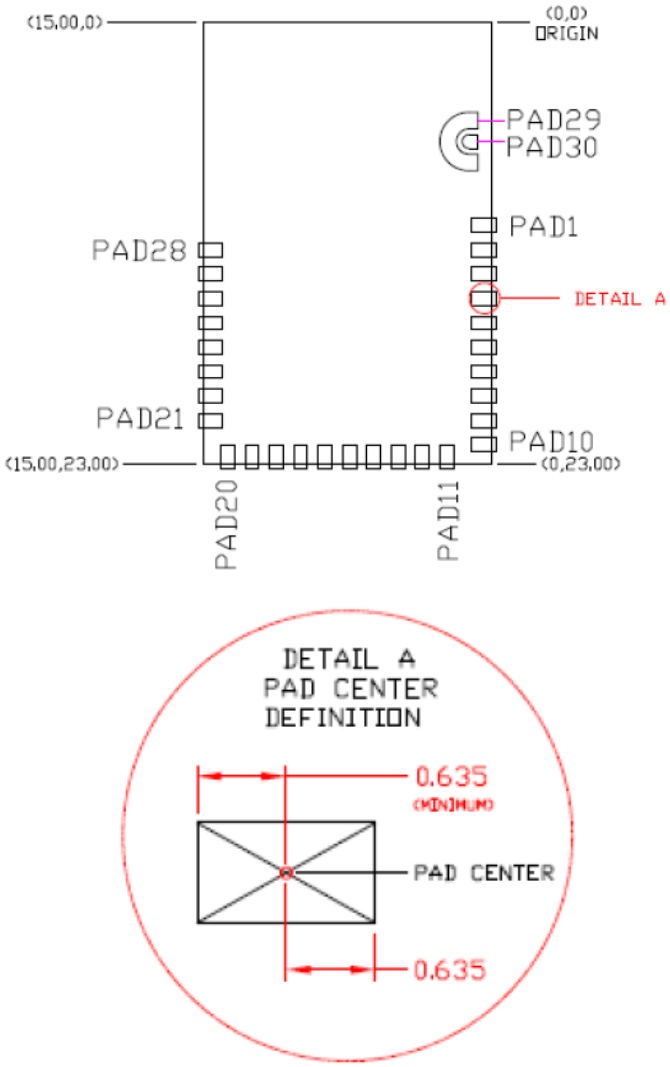
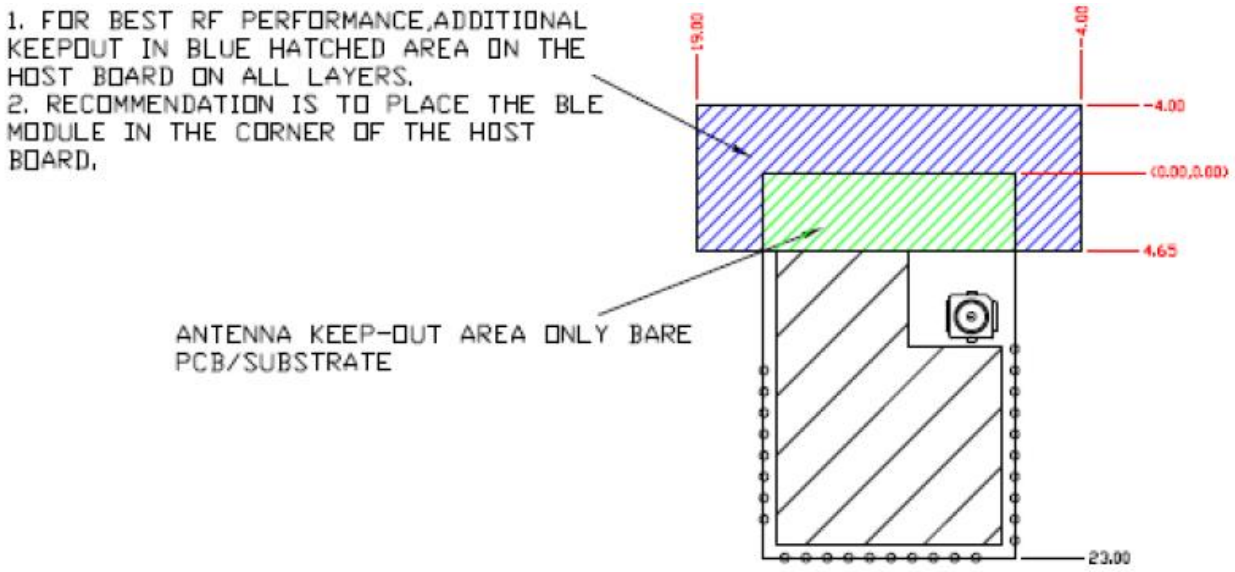


Table 19. Location to Pad Center from Origin (dimensions in mm and mils)

Solder Pad (Center of Pad)	Location (X,Y) from Origin (mm)	Location (X,Y) from Origin (mils)
1	(0.38, 10.54)	(14.96, 414.96)
2	(0.38, 11.81)	(14.96, 464.96)
3	(0.38, 13.08)	(14.96, 514.96)
4	(0.38, 14.35)	(14.96, 564.96)
5	(0.38, 15.62)	(14.96, 614.96)
6	(0.38, 16.89)	(14.96, 664.96)
7	(0.38, 18.16)	(14.96, 714.96)
8	(0.38, 19.43)	(14.96, 764.96)
9	(0.38, 20.70)	(14.96, 814.96)
10	(0.38, 21.97)	(14.96, 864.96)
11	(2.32, 22.62)	(91.34, 890.55)
12	(3.59, 22.62)	(141.34, 890.55)
13	(4.86, 22.62)	(191.34, 890.55)
14	(6.13, 22.62)	(241.34, 890.55)
15	(7.40, 22.62)	(291.34, 890.55)
16	(8.67, 22.62)	(341.34, 890.55)
17	(9.94, 22.62)	(391.34,8 90.55)
18	(11.21, 22.62	(441.34, 890.55)
19	(12.48, 22.62	(491.34, 890.55)
20	(13.75, 22.62	(541.34, 890.55)
21	(14.62, 20.70	(575.59, 814.96)
22	(14.62, 19.43	(575.59, 764.96)
23	(14.62, 18.16	(575.59, 714.96)
24	(14.62, 16.89	(575.59, 664.96)
25	(14.62, 15.62	(575.59, 614.96)
26	(14.62, 14.35	(575.59, 564.96)
27	(14.62, 13.08	(575.59, 514.96)
28	(14.62, 11.81	(575.59, 464.96)
29	See Figure 2 of Datasheet	
30		

Figure 107 details additional host board keep out area to achieve optimal RF performance with the CYBLE-2X20XX-X1 module.

Figure 107. Host Board Additional Keep Out Area for Optimal RF Performance



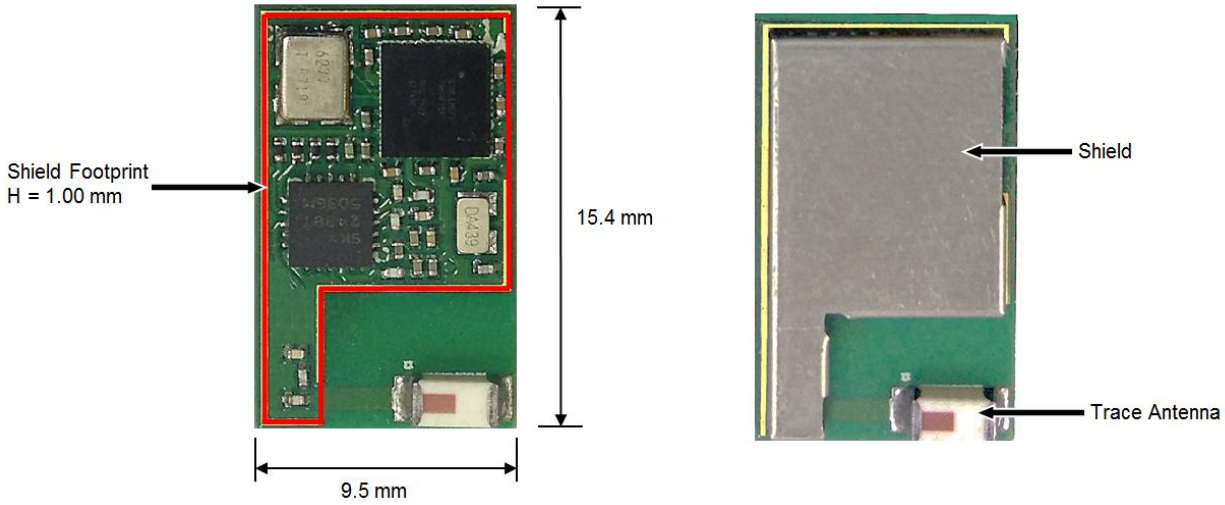
B.1.8 CYBLE-22411X-0X XT/XR

The CYBLE-22411X-0X includes the CYBLE-224110-00 and the CYBLE-224116-01 modules. The only difference between these modules is the Bluetooth specification support (v4.1 for the CYBLE-224110-00 and v4.2 for the CYBLE-224116-01). The CYBLE-22411X-0X is an EZ-BLE PSoC module, providing extended temperature range (up to 105 C) and extended communication range (up to 400 meters line-of-sight) in addition to the integration capability of the PSoC 4 BLE architecture.

In order to operate the CYBLE-224110-00 module in extended range mode, please refer to the Firmware Process for Enabling and Activating Power Amplifier/Low-Noise Amplifier in this section of the application note.

Figure 108 shows a physical picture of the CYBLE-22411X-0X EZ-BLE PSoC XT/XR module.

Figure 108. CYBLE-22411X-0X Module Top View (with and without Shield)

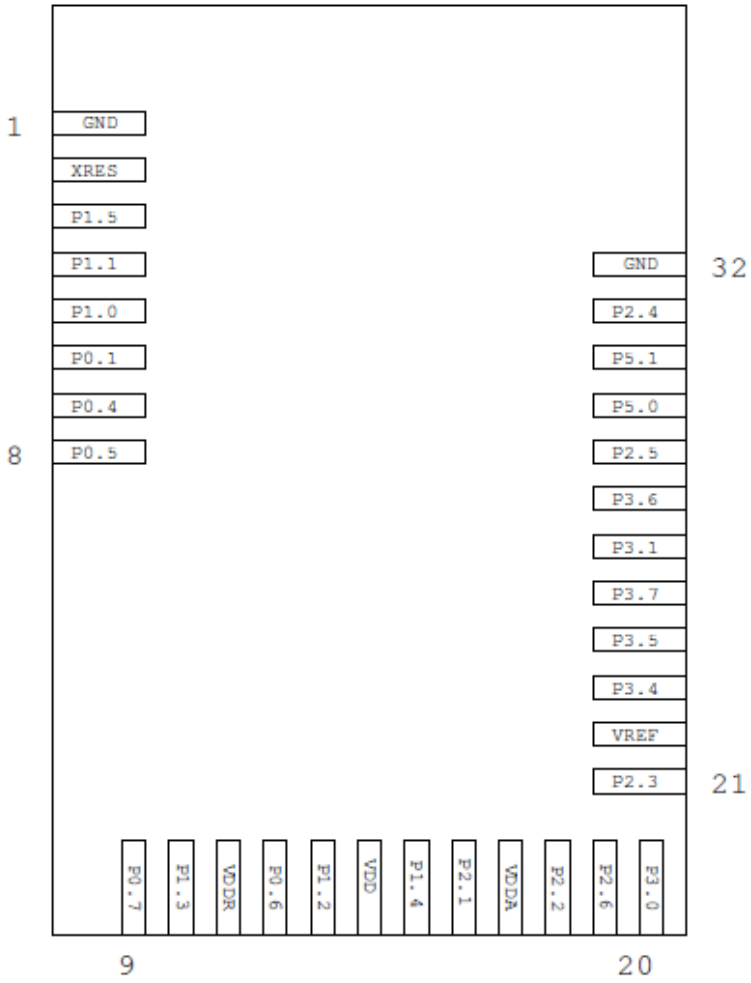


For more details on this module's dimensions, external component connections, and module placement recommendations, see the CYBLE-224110-00 datasheet specification or the CYBLE-224116-01 datasheet specification.

B.1.8.1 Pinout and Functionality

The CYBLE-22411X-0X module is designed to mount as a component on an end-product PCB. Only a portion of the available I/O of the PSoC BLE silicon device is exposed on the CYBLE-22411X-0X module in order to minimize the module footprint size. The CYBLE-22411X-0X module contains 32 connections on the bottom side of the module. Figure 109 details the bottom side connections available on the CYBLE-22411X-0X module.

Figure 109. CYBLE-22411X-0X Module Bottom View (Seen from Bottom)



A list of the available I/Os and supported functionality for each I/O of the CYBLE-22411X-0X is shown in Table 20.

Table 20. CYBLE-22411X-0X Module Available Connections and Functionality

Module Solder Pad Number	Silicon Port Pin	Functionality												
		UART	SPI	I2C	TCPWM[45, 46]	CapSense	LCD Drive	WCO Out	ECO OUT[47]	SWD	SARMUX	OPAMP	LP-COMP	GPIO[48]
1	GND	Ground Connection												
2	XRES	External Reset Hardware Connection Input												
3	P1[5]	SCB0_TX	SCB0_MISO	SCB0_SCL	TCPWM	Sensor	Yes					CTBm1_OA1_INP		Yes

[45] Timer, counter, pulse-width modulator (PWM); configurable as 16-bit timer, counter, PWM blocks

[46] TCPWM connections on ports 0, 1, 2, and 3 can be routed through the Digital Signal Interconnect (DSI) to any of the TCPWM blocks and can be either positive or negative polarity. TCPWM connections on ports 4 and 5 are direct and can only be used with the specified TCPWM block and polarity specified above.

[47] External Crystal Oscillator Output from the device/module

[48] General Purpose Input/Output

Module Solder Pad Number	Silicon Port Pin	Functionality												
		UART	SPI	I2C	TCPWM[45, 46]	CapSense	LCD Drive	WCO Out	ECO OUT[47]	SWD	SARMUX	OPAMP	LP-COMP	GPIO[48]
4	P1[1]		SCB1_SS1		TCPWM	Sensor	Yes					CTBm1_OA0_INN		Yes
5	P1[0]				TCPWM	Sensor	Yes		Yes			CTBm1_OA0_INP		Yes
6	P0[1]	SCB1_TX	SCB1_MISO	SCB1_SCL	TCPWM	Sensor	Yes						COMP0_INN	Yes
7	P0[4]	SCB0_RX	SCB0_MOSI	SCB0_SDA	TCPWM	Sensor	Yes		Yes				COMP1_INP	Yes
8	P0[5]	SCB0_TX	SCB0_MISO	SCB0_SCL	TCPWM	Sensor	Yes						COMP1_INN	Yes
9	P0[7]	SCB0_CTS	SCB0_SCLK		TCPWM	Sensor	Yes			SWDCLK[49]				Yes
10	P1[3]		SCB1_SS		TCPWM	Sensor	Yes					CTBm1_OA1_OUT		Yes
11	VDDR	Radio Power Supply 2.0 V to 3.6 V												
12	P0[6]	SCB0_RTS	SCB0_SS0		TCPWM	Sensor	Yes			SWDIO[49]				Yes
13	P1[2]		SCB1_SS2		TCPWM	Sensor	Yes					CTBm1_OA0_OUT		Yes
14	VDD	Digital Power Supply Input 2.0 to 3.6V												
15	P1[4]	SCB0_RX	SCB0_MOSI	SCB0_SDA	TCPWM	Sensor	Yes					CTBm1_OA1_INN		Yes
16	P2[1]		SCB0_SS2		TCPWM	Sensor	Yes					CTBm1_OA0_INN		Yes
17	VDDA	Analog Power Supply Input 2.0 to 3.6V												
18	P2[2]		SCB0_SS3		TCPWM	Sensor	Yes					CTBm1_OA0_OUT		Yes
19	P2[6]				TCPWM	Sensor	Yes					CTBm1_OA0_INP		Yes
20	P3[0]	SCB0_RX		SCB0_SDA	TCPWM	Sensor	Yes				SARMUX_0			Yes
21	P2[3]				TCPWM	Sensor	Yes	Yes				CTBm1_OA1_OUT		Yes
22	VREF	Reference Voltage Inputs (Optional)												
23	P3[4]	SCB1_RX		SCB1_SDA	TCPWM	Sensor	Yes				SARMUX_4			Yes
24	P3[5]	SCB1_TX		SCB1_SCL	TCPWM	Sensor	Yes				SARMUX_5			Yes
25	P3[7]	SCB1_CTS			TCPWM	Sensor	Yes	Yes			SARMUX_7			Yes
26	P3[1]	SCB0_TX		SCB0_SCL	TCPWM	Sensor	Yes				SARMUX_1			Yes
27	P3[6]	SCB1_RTS			TCPWM	Sensor	Yes				SARMUX_6			Yes
28	P2[5]				TCPWM	Sensor	Yes					CTBm1_OA1_INP		Yes
29	P5[0]	SCB1_RX	SCB1_SS0	SCB1_SDA	TCPWM3_P	Sensor	Yes							Yes
30	P5[1]	SCB1_TX	SCB1_SCLK	SCB1_SCL	TCPWM3_N	Sensor	Yes		Yes					Yes
31	P2[4]				TCPWM	Sensor	Yes					CTBm1_OA1_INN		Yes
32	GND	Ground Connection												

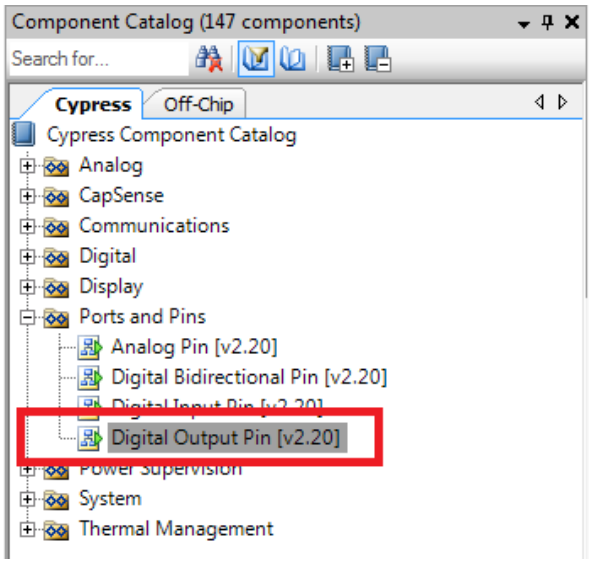
[49] SDWCLK and SWDIO connections can be multiplexed as the functional options listed in each of the respective rows and can be used for programming without the need to reconfigure the device I/O.

B.1.8.2 Process for Enabling and Activating Power Amplifier/Low-Noise Amplifier

The CYBLE-22411X-0X module comes with an integrated Power Amplifier/Low Noise Amplifier to allow the user to extend the reach of BLE communication up to 400 meters line-of-sight. This section will describe the firmware steps required to enable the extended range operation of the CYBLE-22411X-0X module. To enable the extended range functionality, follow the steps outlined below.

- Drag and drop two “Digital Output Pin” components from the Component Catalog to the schematic page as shown in Figure 110.

Figure 110. Drag Digital Output Pins from Component Catalog



- Double-click the pins and rename them as CPS and CSD as shown in Figure 111 and Figure 112. The HW connection option in the component configuration should be unchecked as these are Firmware GPIOs.

Figure 111. Renaming the Pins

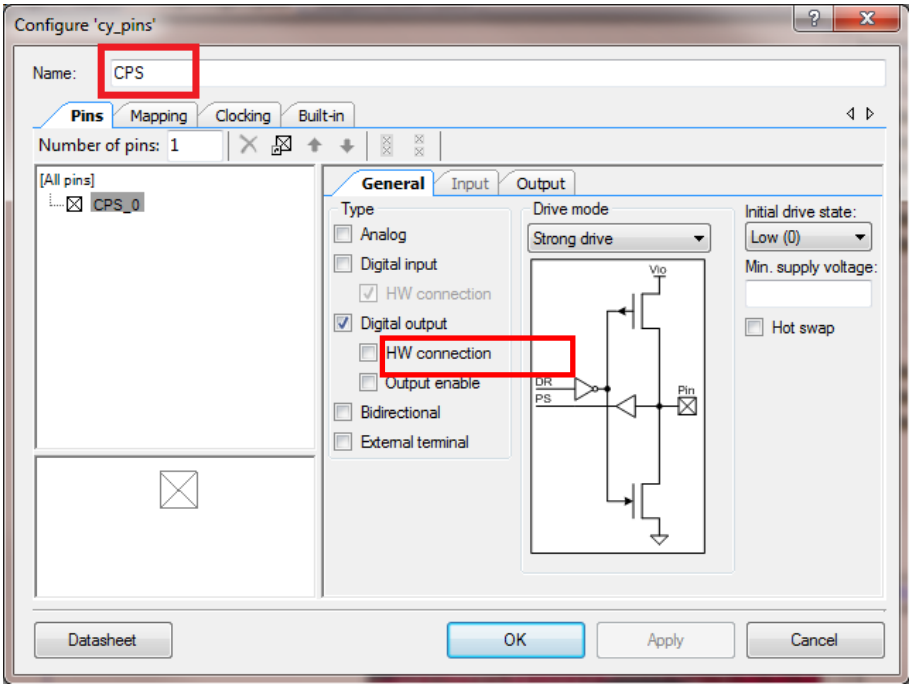
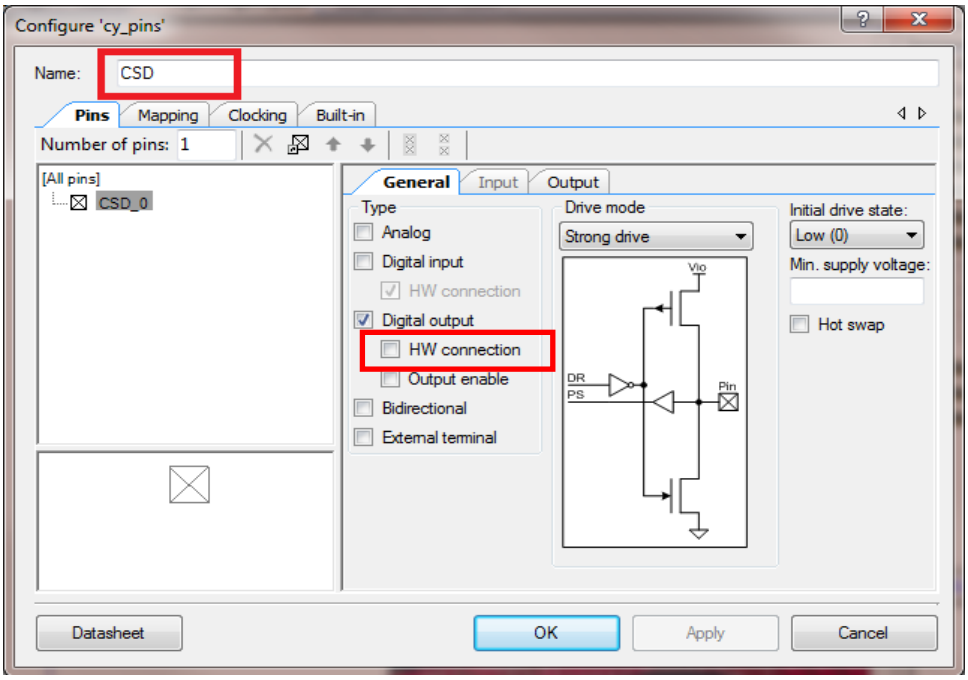
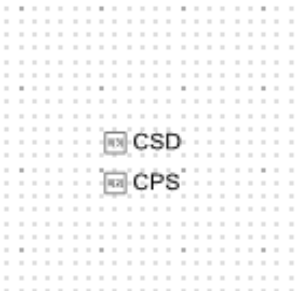


Figure 112. Renaming the Pins



- The final schematic page should include the two pins, as shown in Figure 113.

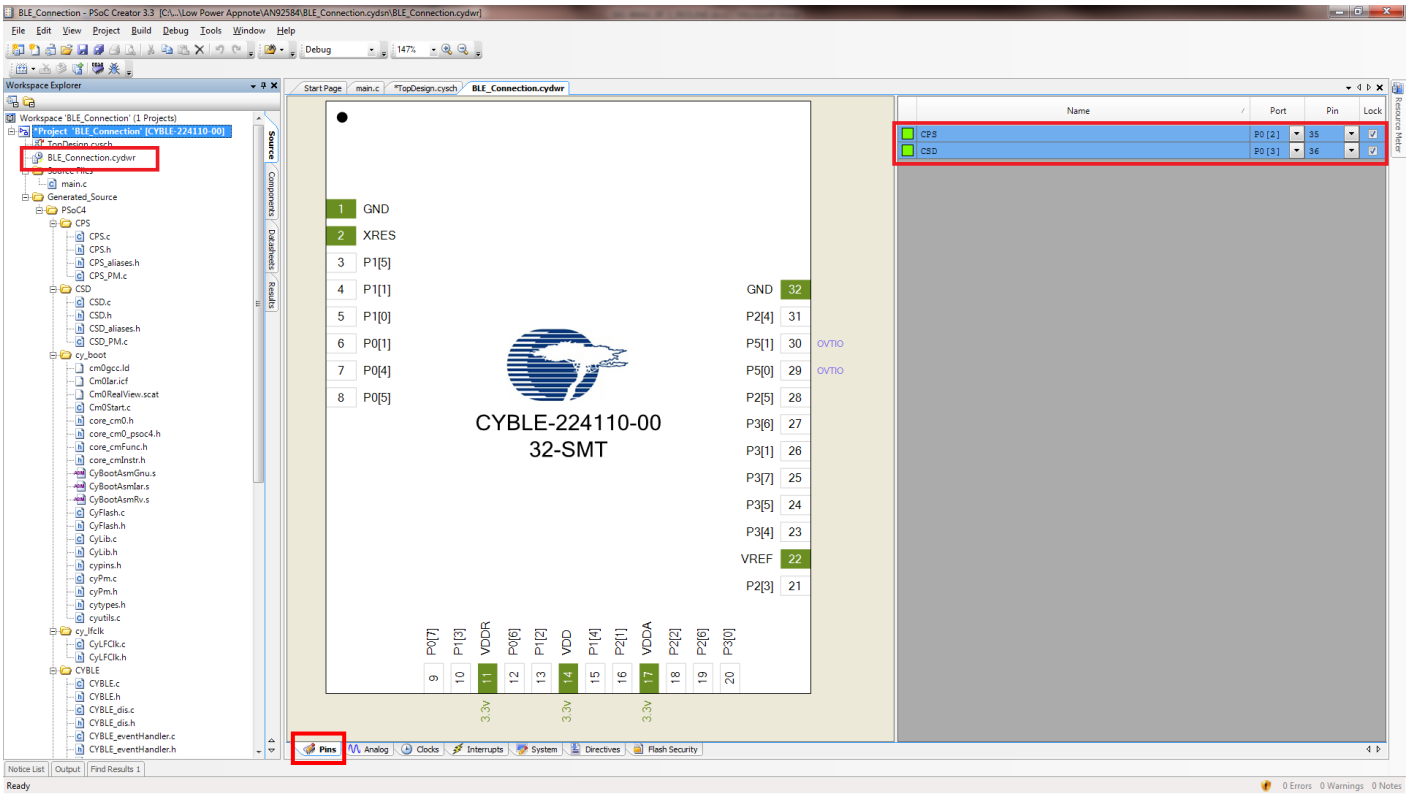
Figure 113. Final Schematic View of the Pins



The Skyworks SE2438T is controlled by PSoC4 BLE and uses four pins: 1) two pins for radio enable (CPS – P0[2], CSD – P0[3]), 2) one pin to control the PA enable (P3[2]), and 3) one pin to control the LNA enable (P3[3]). The PA and LNA enable pins are controlled directly by the BLE Link Layer. The CPS and CSD pins are controlled in the firmware application code.

- To configure the CPS and CSD pins, open your project's Design-Wide Resources file (e.g. "Project_Name.cydwr") from your Workspace Explorer and click the "Pins" tab. The "Pins" tab is used to select the physical device connections for the outputs (CPS, CSD) as shown in Figure 114. These pins are connected to the enable pins of the Skyworks SE2438T Power Amplifier. In order for extended range operation to function, it is required to configure the CPS and CSD pins to P0[2] and P0[3] respectively. This connection can be seen in Figure 114.

Figure 114. Pin Selection for CPS and CSD (Shown for CYBLE-224110-00)



- Open your project's main.c file and write the below code to define the register at the top of the code.

```
/* define the test register to switch the PA/LNA hardware control pins */
#define     CYREG_SRSS_TST_DDFT_CTRL    0x40030008
```

- Browse to the event "CYBLE_EVT_STACK_ON" in the code and insert the below four lines of code to enable the Skyworks SE2438T.

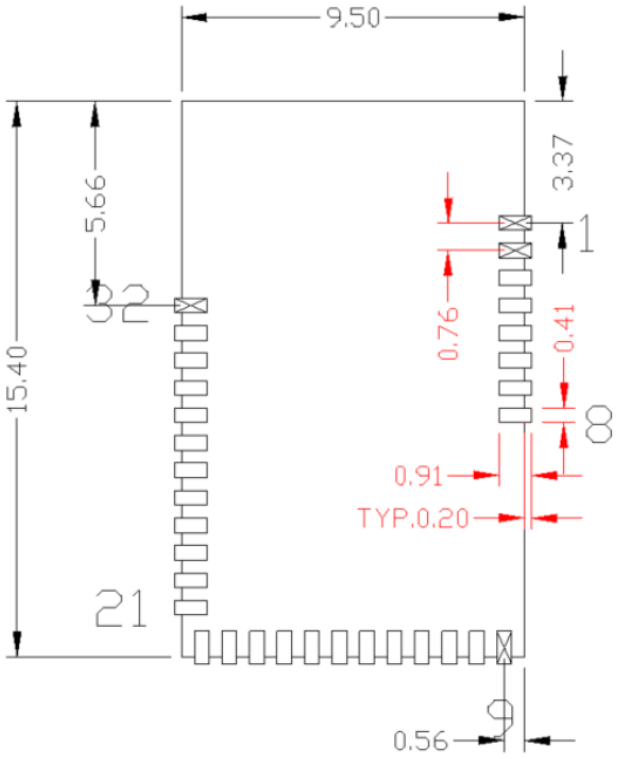
```
/* Mandatory events to be handled by Find Me Target design */
case CYBLE_EVT_STACK_ON:
    /* Enable the Skyworks SE2438T PA/LNA */
    CSD_Write(1);
    CPS_Write(1);

    /* Configure the Link Layer to automatically switch PA
     * control pin P3[2] and LNA control pin P3[3] */
    CY_SET_XTND_REG32((void CYFAR *)(CYREG_BLE_BLESS_RF_CONFIG), 0x0331);
    CY_SET_XTND_REG32((void CYFAR *)(CYREG_SRSS_TST_DDFT_CTRL), 0x80000302);
```

B.1.8.3 Host Recommended PCB Layout

To assist in the host PCB layout design for the CYBLE-22411X-0X, Cypress provides three host PCB reference drawings in Figure 115, Figure 116, and in Figure 117 and Table 21. Figure 115 provides a dimensions view of the host PCB layout. Figure 116 provides the location to the center edge of each solder pad relative to the origin of the module (upper right PCB outline). Figure 117 and Table 21 provide the location to each solder pad center location for the host PCB layout. Dimensions shown are in mm unless otherwise stated.

Figure 115. Host Board Required PCB Layout Pattern (Dimensioned View)



Note: Pad length shown includes overhang of the host pad beyond the module pad outline. The minimum recommended pad length on the host PCB is 0.91 mm.

Figure 116. Host Board Required PCB Layout Pattern: To Pad Center Edge Relative to Origin

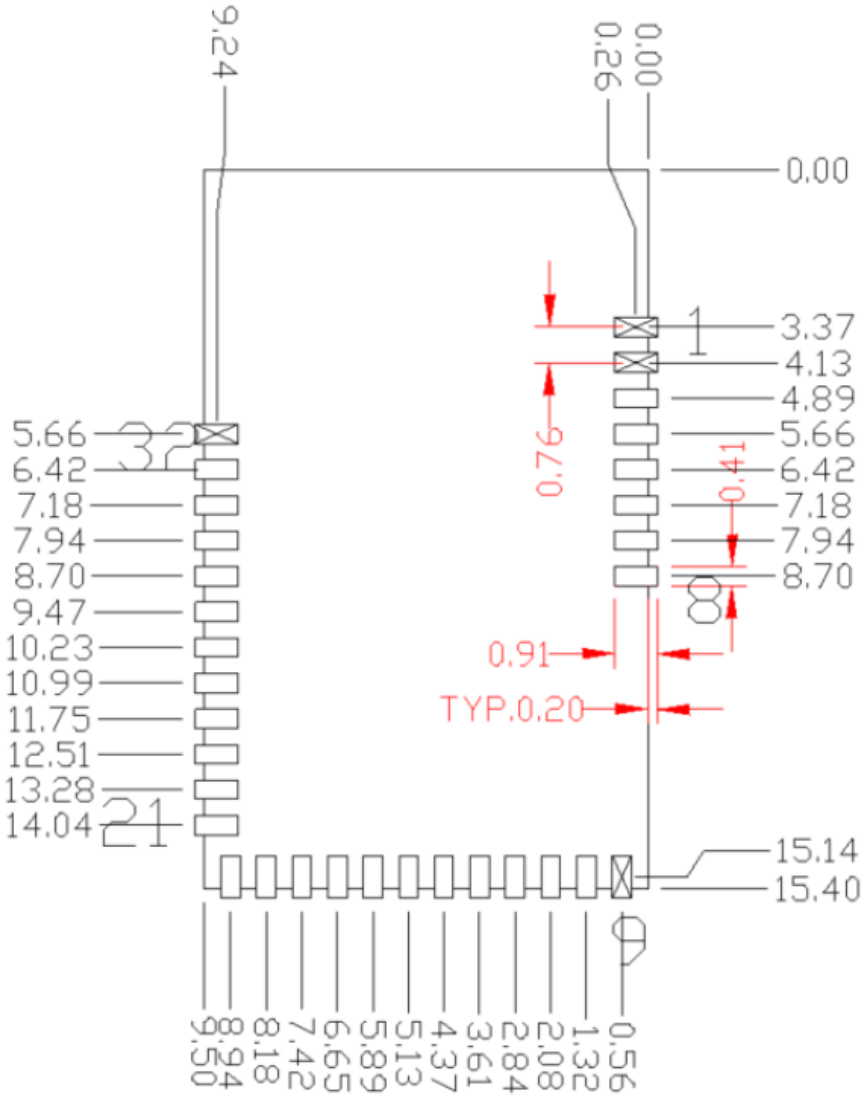


Figure 117. Host Board Required PCB Layout Pattern To Pad Center Relative to Origin

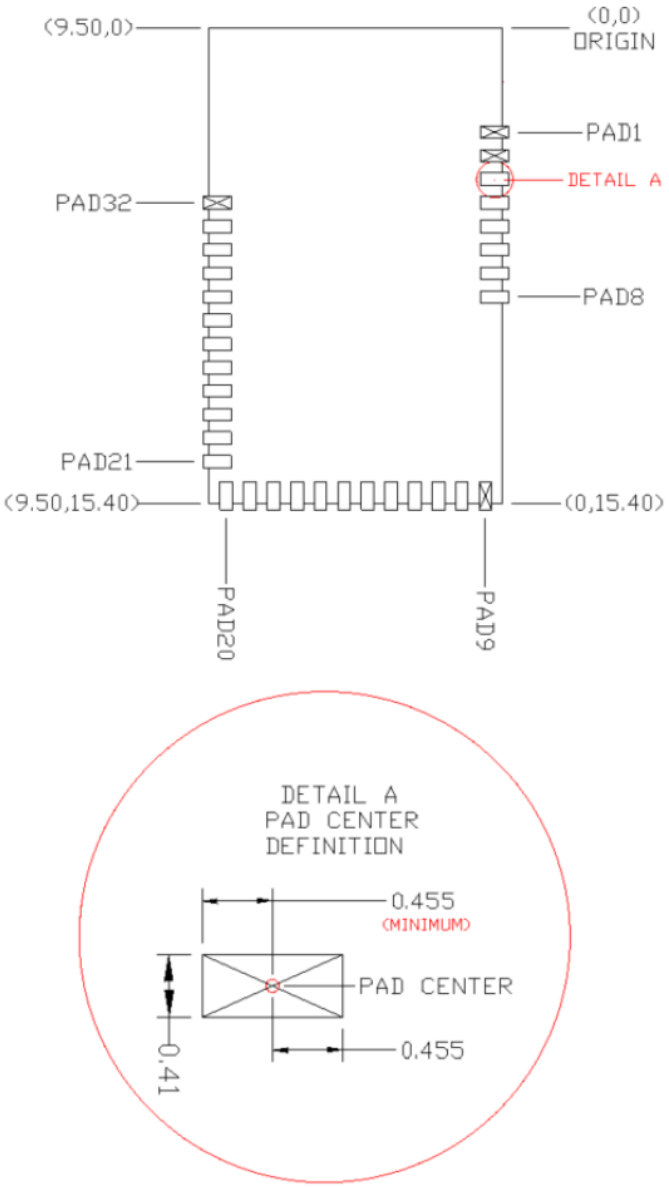
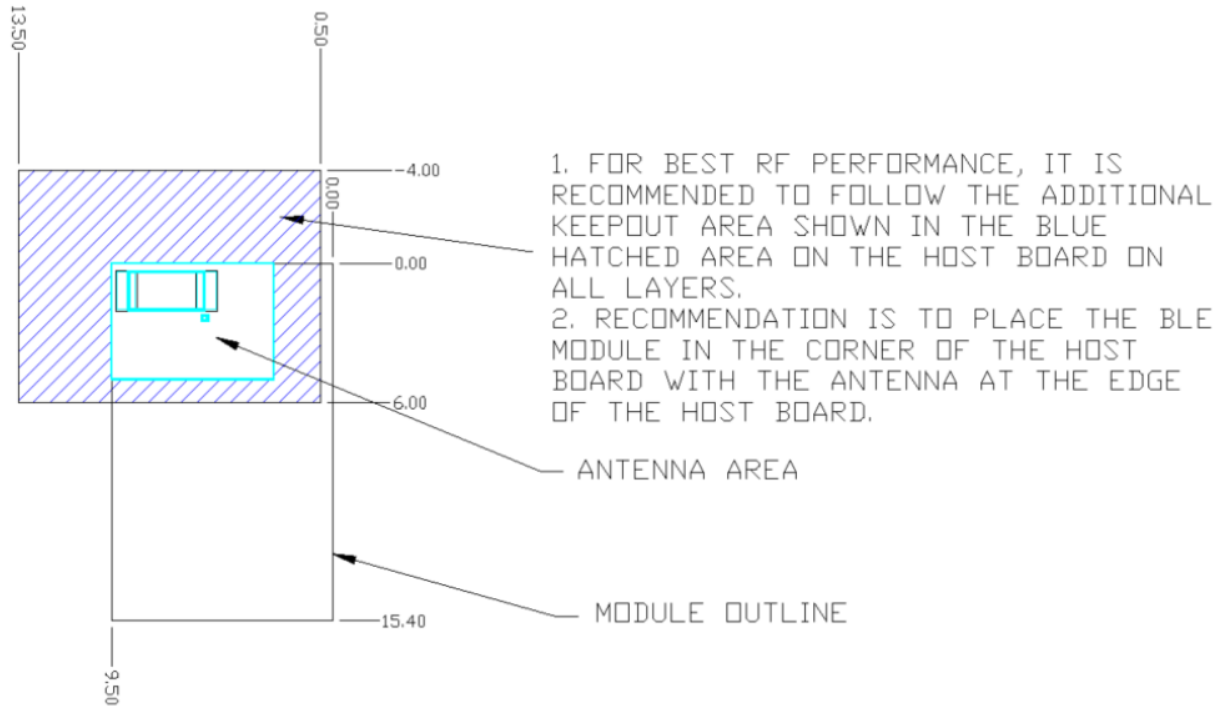


Table 21. Location to Pad Center from Origin (dimensions in mm and mils)

Solder Pad (Center of Pad)	Location (X,Y) from Origin (mm)	Location (X,Y) from Origin (mils)
1	(0.26, 3.37)	(10.24, 132.68)
2	(0.26, 4.13)	(10.24, 162.68)
3	(0.26, 4.89)	(10.24, 192.68)
4	(0.26, 5.66)	(10.24, 222.68)
5	(0.26, 6.42)	(10.24, 252.68)
6	(0.26, 7.18)	(10.24, 282.68)
7	(0.26, 7.94)	(10.24, 312.68)
8	(0.26, 8.70)	(10.24, 342.68)
9	(0.56, 15.14)	(22.05, 596.06)
10	(1.32,15.14)	(51.97, 596.06)
11	(2.08, 15.14)	(81.89, 596.06)
12	(2.84,15.14)	(111.81, 596.06)
13	(3.61, 15.14)	(142.13, 596.06)
14	(4.37, 15.14)	(172.13, 596.06)
15	(5.13, 15.14)	(202.13, 596.06)
16	(5.89, 15.14)	(231.89, 596.06)
17	(6.65,15.14)	(261.81, 596.06)
18	(7.42, 15.14)	(292.13, 596.06)
19	(8.18, 15.14)	(322.05, 596.06)
20	(8.94, 15.14)	(351.97, 596.06)
21	(9.24, 14.04)	(363.78, 552.76)
22	(9.24, 13.28)	(363.78, 522.83)
23	(9.24, 12.51)	(363.78,492.52)
24	(9.24, 11.75)	(363.78, 462.60)
25	(9.24,10.99)	(363.78, 432.68)
26	(9.24,10.23)	(363.78, 402.76)
27	(9.24, 9.47)	(363.78, 372.83)
28	(9.24, 8.70)	(363.78, 342.52)
29	(9.24, 7.94)	(363.78, 312.60)
30	(9.24, 7.18)	(363.78, 282.68)
31	(9.24, 6.42)	(363.78, 252.76)
32	(9.24,5.66)	(363.78, 222.83)

Figure 118 below details additional host board keep out area to achieve optimal RF performance with the CYBLE-22411X-0X module.

Figure 118. Host Board Additional Keep Out Area for Optimal RF Performance



Appendix C. EZ-BLE Evaluation Board Details

Appendix C provides detailed information on each EZ-BLE Evaluation Board. The information contained for each subsection below includes the following:

- Physical image for each EZ-BLE Evaluation marketing part number
- What's included on the specific EZ-BLE Evaluation board
- EZ-BLE Evaluation board connections to CY8CKIT-042-BLE-A

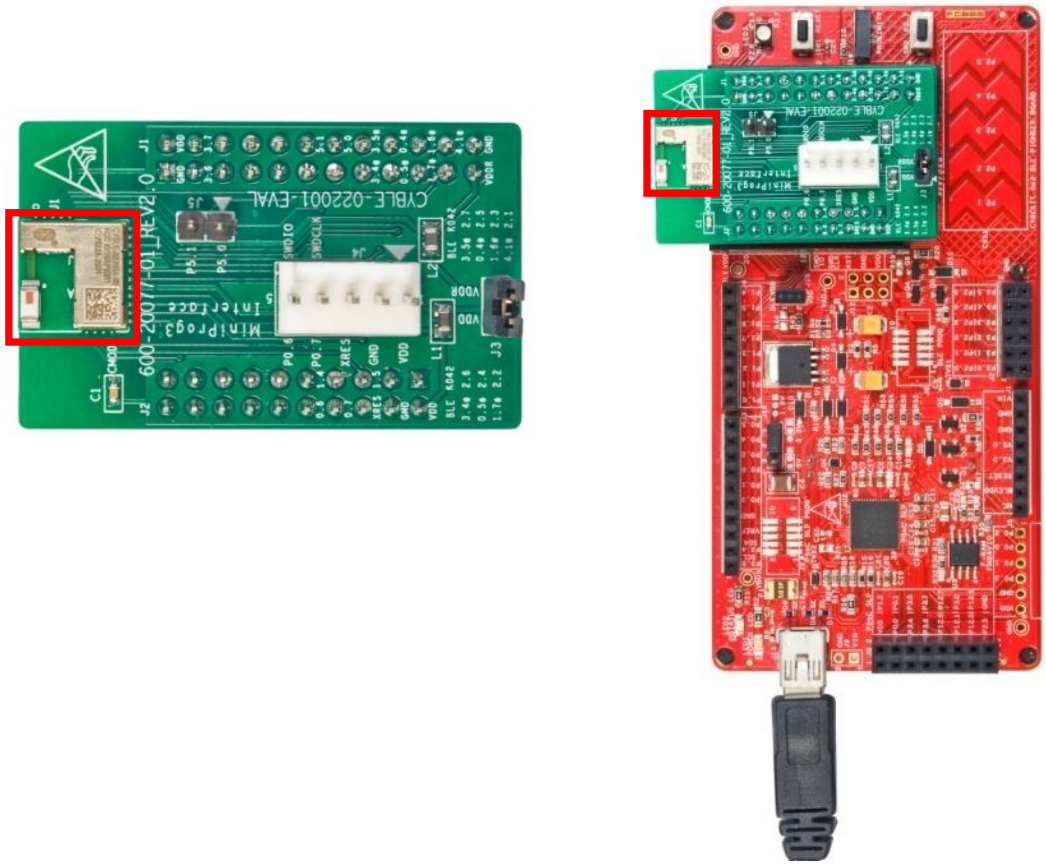
To jump to your specific EZ-BLE Evaluation board, click the marketing part number in the below list:

C.1 EZ-BLE Module Evaluation Board Details

C.1.1 CYBLE-022001-EVAL

Figure 119 shows the CYBLE-022001-EVAL connected to the CY8CKIT-042-BLE Kit. The EZ-BLE PRoC Module (CYBLE-022001-00) is shown in the red box in Figure 119.

Figure 119. CYBLE-022001-EVAL (Left) Connected to CY8CKIT-042-BLE (Right)

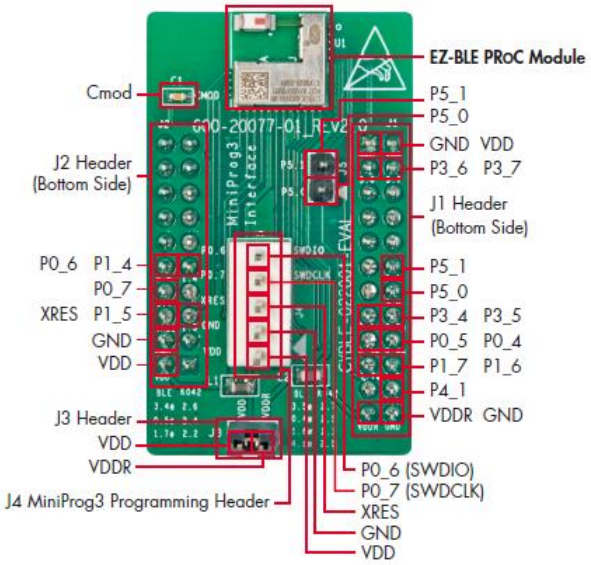


C.1.1.1 CYBLE-022001-EVAL Connections to CY8CKIT-042-BLE

The CYBLE-022001-00 module contains 21 connections on the bottom of the module. All but one of these connections is present on the CYBLE-022001-EVAL evaluation board (Port 4[0] is connected to C_{mod} to enable capacitive sensing on the CY8CKIT-042-BLE Pioneer Kit).

Figure 120 shows the CYBLE-022001-EVAL and highlights the elements on the top side of the board. The port-pin connections shown below denote the EZ-BLE module connections on the evaluation board, not the CY8CKIT-042-BLE baseboard connections.

Figure 120. CYBLE-022001-EVAL Board Top Side



Note: Connections not called out on J1 and J2 connection headers are NC (No Connect), where no physical connection is present between the CYBLE-022001-00 EZ-BLE PRoC Module and the CYBLE-022001-EVAL board J1 and J2 headers.

Note: The EZ-BLE PRoC Module includes only 16 GPIOs. In order to maintain full capability of the CY8CKIT-042-BLE Pioneer Kit functionality, seven of the Port-Pin connections do not completely match the CY8CKIT-042-BLE baseboard pin out. See Table 22 for the complete list of GPIOs available on the CYBLE-022001-EVAL and the corresponding Port-Pin connection to the CY8CKIT-042-EVAL baseboard.

The CYBLE-022001-EVAL includes the following elements:

- C_{mod}: A 2.2-nF capacitor mounted on the evaluation board used with the CY8CKIT-042-BLE capacitive sensing slider, buttons, and proximity sensors. C_{mod} is connected to P4[0] on the CYBLE-022001-00 EZ-BLE PRoC Module to enable capacitive sensing when connected to the CY8CKIT-042-BLE Kit.
- J3 Header: A two-pin header that exposes VDD and VDDR. This header can be used to short the VDD and VDDR. This jumper must be shorted when using the CYBLE-022001-EVAL with the MiniProg3 kit due to the fact that the MiniProg3 kit only supplies VDD to the evaluation board. When using the CYBLE-022001-EVAL in conjunction with the CY8CKIT-042-BLE Pioneer kit, this jumper connection does not matter, and it can be connected or disconnected.
- J4 Header: A five-pin header that exposes connections used for programming the EZ-BLE PRoC Module Evaluation board by using the MiniProg3 kit, as shown in Figure 121.

Figure 121. CYBLE-022001-EVAL Using CY8CKIT-002 MiniProg3

Pin Mapping	
CY8CKIT-002	CYBLE-022001-EVAL
VTARG	VDD
GND	GND
RES	XRES
SCLK	P0_7
SDAT	P0_6

- J5: A header that exposes P5[0] and P5[1], which can be used for I^2C communication (including high-speed I^2C) to the CYBLE-022001-00 EZ-BLE PRoC Module.

As mentioned previously, the port-pin connections do not completely match the CY8CKIT-042-BLE baseboard pin out. Seven such connections exist on the CYBLE-022001-EVAL that do not align with the CY8CKIT-042-BLE baseboard (highlighted in red in Table 22). Fortunately, PRoC BLE is configurable so that pin functions can be easily re-assigned.

Table 22 details all connections on the CY8CKIT-042-BLE baseboard and provides the equivalent Port-Pin connection on the CYBLE-022001-EVAL board. The port-pin list order is according on the CY8CKIT-042-BLE baseboard physical connection pinout.

Table 22. CYBLE-022001-EVAL Port-Pin Connections to CY8CKIT-042-BLE Baseboard

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-022001-EVAL Connection Port-Pin
J11	P0[0]	NC
J11	P0[1]	NC
J11	P0[2]	NC
J11	P0[3]	NC
J11	P0[4]	NC
J11	P0[5]	NC
J11	VREF	VREF
J11	P1[0]	NC
J11	P1[1]	NC
J11	P1[2]	NC
J11	P1[4]	P1[4]
J11	P0[6]	P0[6]
J11	P1[3]	NC
J11	P0[7]	P0[7]
J11	P1[5]	P1[5]
J11	XRES	XRES
J11	P1[7]	NC
J11	GND	GND
J11	P1[6]	NC
J11	VDD	VDD
J12	GND	GND
J10	VDD	VDD
J10	P3[6]	P3[6]
J10	P3[7]	P3[7]
J10	P3[4]	NC
J10	P3[5]	NC
J10	P3[2]	NC
J10	P3[3]	NC
J10	P3[0]	NC
J10	P3[1]	NC

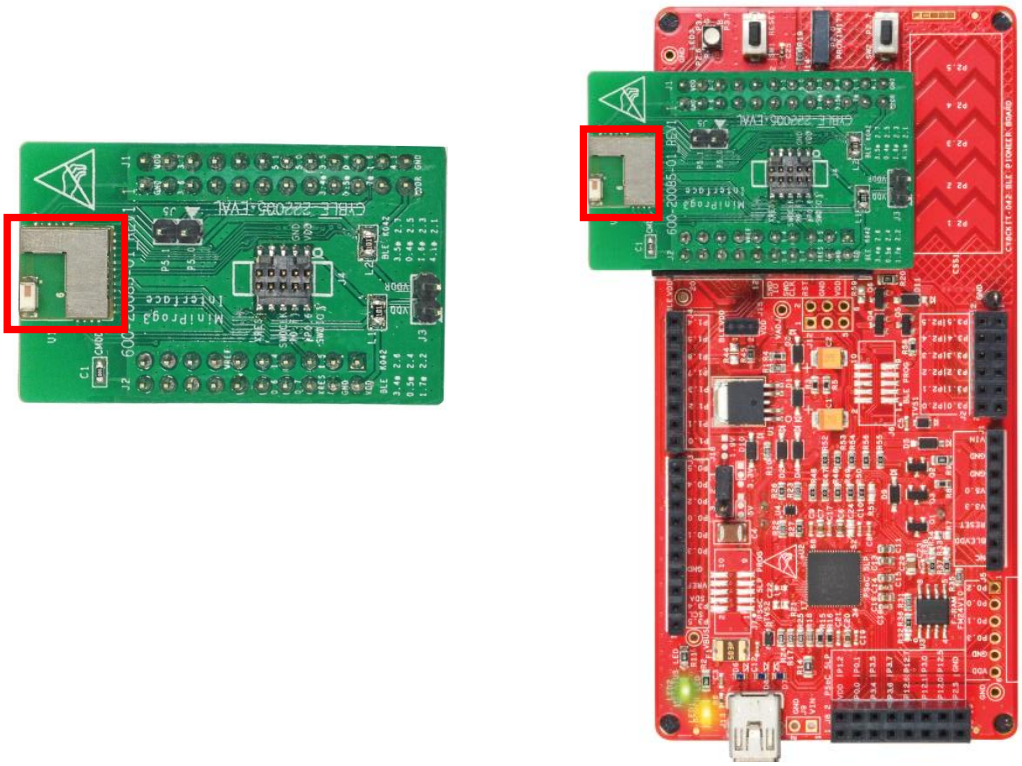
CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-022001-EVAL Connection Port-Pin
J10	P4[0][50]	NC[50]
J10	P5[1]	P5[1]
J10	P4[1]	NC
J10	P5[0]	P5[0]
J10	P2[6]	P3[4]
J10	P2[7]	P3[5]
J10	P2[4]	P0[5]
J10	P2[5]	P0[4]
J10	P2[2]	P1[7]
J10	P2[3]	P1[6]
J10	P2[0]	NC
J10	P2[1]	P4[1]
J10	VDDR	VDDR
J10	GND	GND

[50] P4[0] is available on the EZ-BLE PRoC Module (CYBLE-022001-00). However, the CYBLE-022001-EVAL board utilizes this pin to connect the C_{mod} capacitor to enable capacitive sensing functionality on the CY8CKIT-042-BLE Baseboard.

C.1.2 CYBLE-222005-EVAL

Figure 122 shows the CYBLE-222005-EVAL connected to the CY8CKIT-042-BLE Kit. The EZ-BLE PRoC Module (CYBLE-222005-00) is shown in the red box in Figure 122.

Figure 122. CYBLE-222005-EVAL (Left) Connected to CY8CKIT-042-BLE (Right)

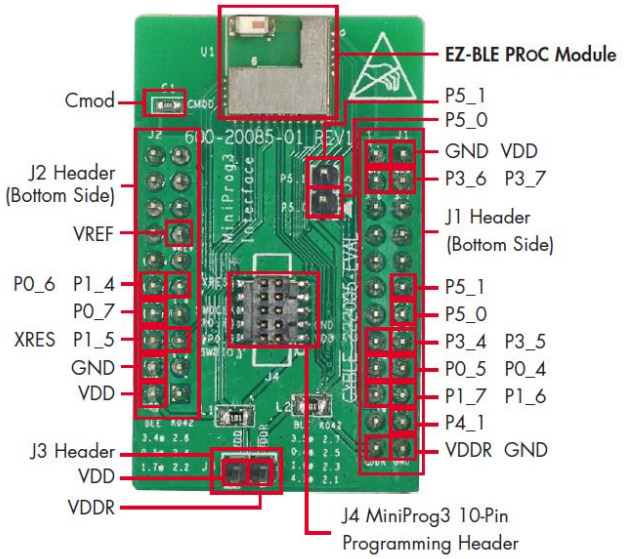


C.1.2.1 CYBLE-222005-EVAL Connections to CY8CKIT-042-BLE

The CYBLE-222005-00 module contains 22 connections on the bottom side of the module. All but one of these connections is present on the CYBLE-222005-EVAL evaluation board (Port 4[0] is connected to C_{mod} to enable capacitive sensing on the CY8CKIT-042-BLE Pioneer Kit).

Figure 123 shows the CYBLE-222005-EVAL and highlights the elements on the top side of the board. The port-pin connections shown below denote the EZ-BLE module connections on the evaluation board, not the CY8CKIT-042-BLE baseboard connections.

Figure 123. CYBLE-222005-EVAL Board Top Side



Note: Connection not called out on J1 and J2 connection headers are NC (No Connect), where no physical connection is present between the CYBLE-222005-00 EZ-BLE PRoC Module and the CYBLE-222005-EVAL board J1 and J2 headers.

Note: The CYBLE-222005-00 EZ-BLE PRoC Module includes only 16 GPIOs. In order to maintain full capability of the CY8CKIT-042-BLE Pioneer Kit functionality, seven of the Port-Pin connections do not completely match the CY8CKIT-042-BLE baseboard pin out. See Table 23 for the complete list of GPIOs available on the CYBLE-222005-EVAL and the corresponding Port-Pin connection to the CY8CKIT-042-EVAL baseboard.

The CYBLE-222005-EVAL includes the following elements:

- C_{mod}: A 2.2-nF capacitor mounted on the evaluation board used with the CY8CKIT-042-BLE capacitive sensing slider, buttons, and proximity sensors. C_{mod} is connected to P4[0] on the CYBLE-222005-00 EZ-BLE PRoC Module to enable capacitive sensing when connected to the CY8CKIT-042-BLE Kit.
- J3 Header: A two-pin header that exposes VDD and VDDR. This header can be used to short the VDD and VDDR. This jumper must be shorted when using the CYBLE-222005-EVAL with the MiniProg3 kit due to the fact that the MiniProg3 kit only supplies VDD to the evaluation board. When using the CYBLE-222005-EVAL in conjunction with the CY8CKIT-042-BLE Pioneer kit, this jumper connection does not matter, and it can be connected or disconnected.
- J4 Header: A 10-pin header is included on the CYBLE-222005-EVAL kit that exposes connections used for programming and debug with the MiniProg3 kit, as shown in Figure 124. The 10-pin ribbon cable included in the MiniProg3 kit must be used for this connection.

Figure 124. CYBLE-222005-EVAL Using CY8CKIT-002 MiniProg3

- J5: A header that exposes P5[0] and P5[1], which can be used for I^2C communication (including high speed I^2C) to the CYBLE-222005-00 EZ-BLE PRoC Module.

As mentioned previously, the Port-Pin connections do not completely match the CY8CKIT-042-BLE baseboard pin out. Seven such connections exist that do not align with the CY8CKIT-042-BLE baseboard (highlighted in red in Table 23). Fortunately, PRoC BLE is configurable so that pin functions can be easily re-assigned.

Table 23 details all connections on the CY8CKIT-042-BLE baseboard and provides the equivalent Port-Pin connection on the CYBLE-222005-EVAL board. The port-pin list order is according on the CY8CKIT-042-BLE baseboard physical connection pinout.

Table 23. CYBLE-222005-EVAL Port-Pin Connections to CY8CKIT-042-BLE Baseboard

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-222005-EVAL Connection Port-Pin
J11	P0[0]	NC
J11	P0[1]	NC
J11	P0[2]	NC
J11	P0[3]	NC
J11	P0[4]	NC
J11	P0[5]	NC
J11	VREF	VREF
J11	P1[0]	NC
J11	P1[1]	NC
J11	P1[2]	NC
J11	P1[4]	P1[4]
J11	P0[6]	P0[6]
J11	P1[3]	NC
J11	P0[7]	P0[7]
J11	P1[5]	P1[5]
J11	XRES	XRES
J11	P1[7]	NC
J11	GND	GND
J11	P1[6]	NC

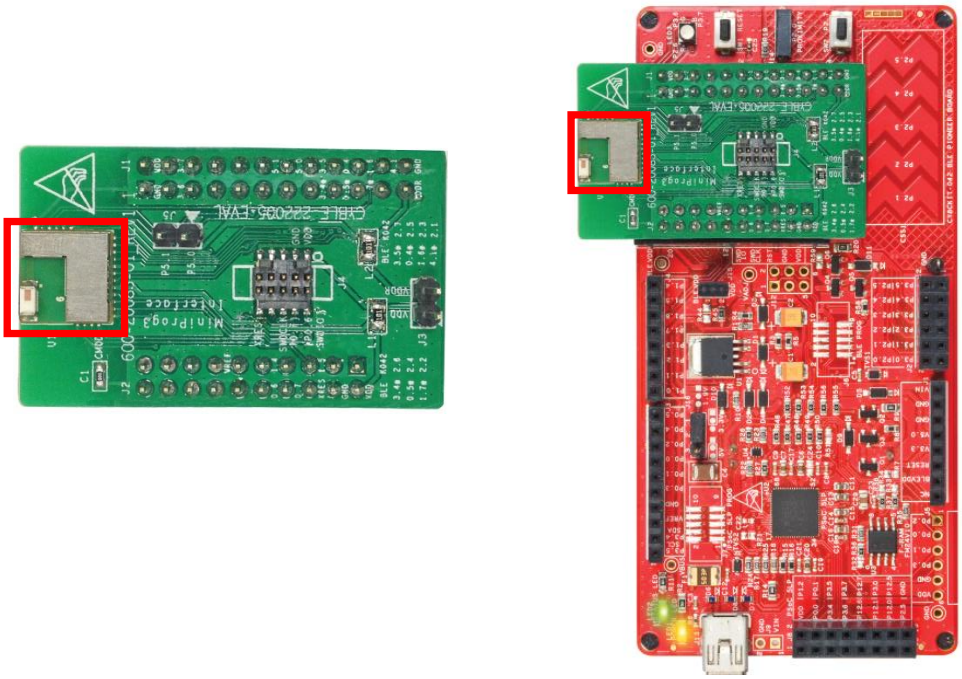
CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-222005-EVAL Connection Port-Pin
J11	VDD	VDD
J12	GND	GND
J10	VDD	VDD
J10	P3[6]	P3[6]
J10	P3[7]	P3[7]
J10	P3[4]	NC
J10	P3[5]	NC
J10	P3[2]	NC
J10	P3[3]	NC
J10	P3[0]	NC
J10	P3[1]	NC
J10	P4[0][51]	NC[51]
J10	P5[1]	P5[1]
J10	P4[1]	NC
J10	P5[0]	P5[0]
J10	P2[6]	P3[4]
J10	P2[7]	P3[5]
J10	P2[4]	P0[5]
J10	P2[5]	P0[4]
J10	P2[2]	P1[7]
J10	P2[3]	P1[6]
J10	P2[0]	NC
J10	P2[1]	P4[1]
J10	VDDR	VDDR
J10	GND	GND

[51] P4[0] is available on the EZ-BLE PRoC Module (CYBLE-222005-00). However, the CYBLE-222005-EVAL board utilizes this pin to connect the C_{mod} capacitor to enable capacitive sensing functionality on the CY8CKIT-042-BLE Baseboard.

C.1.3 CYBLE-222014-EVAL

Figure 125 shows the CYBLE-222014-EVAL connected to the CY8CKIT-042-BLE Kit. The EZ-BLE PRoC BT 4.2 Module (CYBLE-222014-01) is shown in the red box in Figure 125.

Figure 125. CYBLE-222014-EVAL (Left) Connected to CY8CKIT-042-BLE (Right)

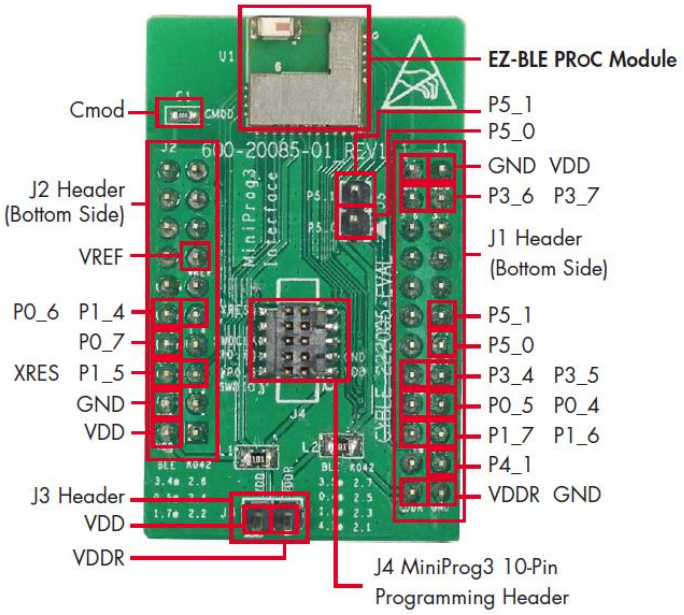


12.1.1.1 CYBLE-222014-EVAL Connections to CY8CKIT-042-BLE

The CYBLE-222014-01 module contains 22 connections on the bottom side of the module. All but one of these connections is present on the CYBLE-222014-EVAL evaluation board (Port 4[0] is connected to C_{mod} to enable capacitive sensing on the CY8CKIT-042-BLE Pioneer Kit).

Figure 126 shows the CYBLE-222014-EVAL and highlights the elements on the top side of the board. The port-pin connections shown below denote the EZ-BLE module connections on the evaluation board, not the CY8CKIT-042-BLE baseboard connections.

Figure 126. CYBLE-222014-EVAL Board Top Side



Note: Connection not called out on J1 and J2 connection headers are NC (No Connect), where no physical connection is present between the CYBLE-222014-01 EZ-BLE PRoC BT 4.2 Module and the CYBLE-222014-EVAL board J1 and J2 headers.

Note: The CYBLE-222014-00 EZ-BLE BT 4.2 PRoC Module includes only 16 GPIOs. In order to maintain full capability of the CY8CKIT-042-BLE Pioneer Kit functionality, seven of the Port-Pin connections do not completely match the CY8CKIT-042-BLE baseboard pin out. See Table 24 for the complete list of GPIOs available on the CYBLE-222014-EVAL and the corresponding Port-Pin connection to the CY8CKIT-042-EVAL baseboard.

The CYBLE-222014-EVAL includes the following elements:

- C_{mod}: A 2.2-nF capacitor mounted on the evaluation board used with the CY8CKIT-042-BLE capacitive sensing slider, buttons, and proximity sensors. C_{mod} is connected to P4[0] on the CYBLE-222014-01 EZ-BLE PRoC BT 4.2 Module to enable capacitive sensing when connected to the CY8CKIT-042-BLE Kit.
- J3 Header: A two-pin header that exposes VDD and VDDR. This header can be used to short the VDD and VDDR. This jumper must be shorted when using the CYBLE-222014-EVAL with the MiniProg3 kit due to the fact that the MiniProg3 kit only supplies VDD to the evaluation board. When using the CYBLE-222014-EVAL in conjunction with the CY8CKIT-042-BLE Pioneer kit, this jumper connection does not matter, and it can be connected or disconnected.
- J4 Header: A 10-pin header is included on the CYBLE-222014-EVAL kit that exposes connections used for programming and debug with the MiniProg3 kit, as shown in Figure 127. The 10-pin ribbon cable included in the MiniProg3 kit must be used for this connection.

Figure 127. CYBLE-222014-EVAL Using CY8CKIT-002 MiniProg3

- J5: A header that exposes P5[0] and P5[1], which can be used for I^2C communication (including high speed I^2C) to the CYBLE-222014-01 EZ-BLE PRoC BT 4.2 Module.

As mentioned previously, the Port-Pin connections do not completely match the CY8CKIT-042-BLE baseboard pin out. Seven such connections exist that do not align with the CY8CKIT-042-BLE baseboard (highlighted in red in Table 24). Fortunately, PRoC BLE is configurable so that pin functions can be easily re-assigned.

Table 24 details all connections on the CY8CKIT-042-BLE baseboard and provides the equivalent Port-Pin connection on the CYBLE-222014-EVAL board. The port-pin list order is according on the CY8CKIT-042-BLE baseboard physical connection pinout.

Table 24. CYBLE-222014-EVAL Port-Pin Connections to CY8CKIT-042-BLE Baseboard

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-222014-EVAL Connection Port-Pin
J11	P0[0]	NC
J11	P0[1]	NC
J11	P0[2]	NC
J11	P0[3]	NC
J11	P0[4]	NC
J11	P0[5]	NC
J11	VREF	VREF
J11	P1[0]	NC
J11	P1[1]	NC
J11	P1[2]	NC
J11	P1[4]	P1[4]
J11	P0[6]	P0[6]
J11	P1[3]	NC
J11	P0[7]	P0[7]
J11	P1[5]	P1[5]
J11	XRES	XRES
J11	P1[7]	NC
J11	GND	GND
J11	P1[6]	NC
J11	VDD	VDD
J12	GND	GND
J10	VDD	VDD
J10	P3[6]	P3[6]
J10	P3[7]	P3[7]
J10	P3[4]	NC
J10	P3[5]	NC
J10	P3[2]	NC
J10	P3[3]	NC
J10	P3[0]	NC

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-222014-EVAL Connection Port-Pin
J10	P3[1]	NC
J10	P4[0][52]	NC[52]
J10	P5[1]	P5[1]
J10	P4[1]	NC
J10	P5[0]	P5[0]
J10	P2[6]	P3[4]
J10	P2[7]	P3[5]
J10	P2[4]	P0[5]
J10	P2[5]	P0[4]
J10	P2[2]	P1[7]
J10	P2[3]	P1[6]
J10	P2[0]	NC
J10	P2[1]	P4[1]
J10	VDDR	VDDR
J10	GND	GND

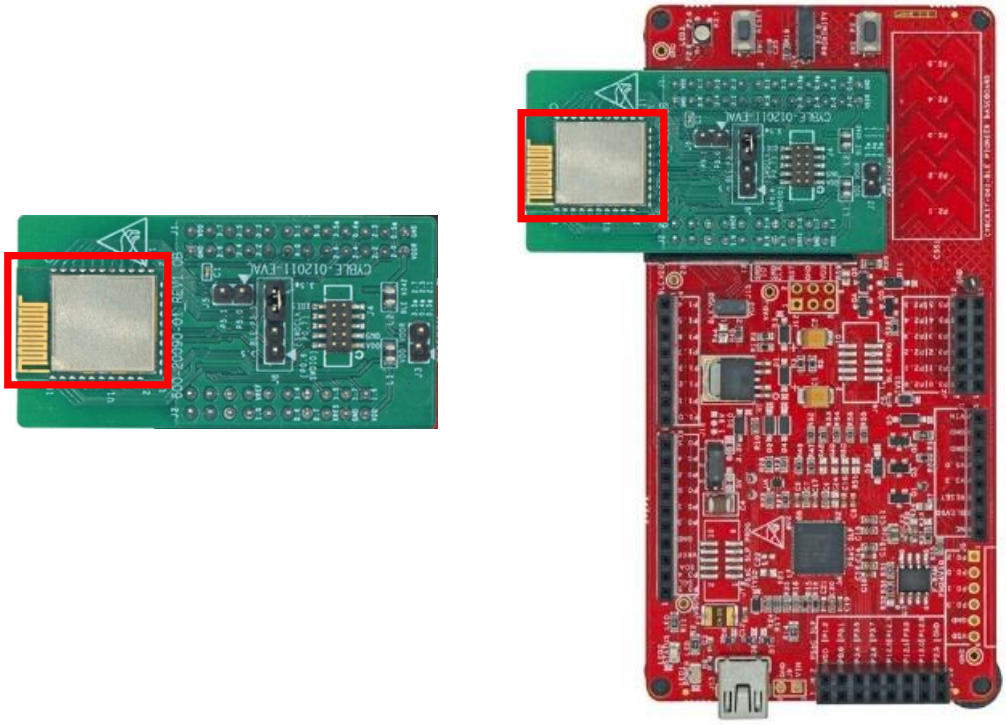
[52] P4[0] is available on the EZ-BLE PRoC BT 4.2 Module (CYBLE-222014-01). However, the CYBLE-222014-EVAL board utilizes this pin to connect the C_{mod} capacitor to enable capacitive sensing functionality on the CY8CKIT-042-BLE Baseboard.

C.1.4 CYBLE-012011-EVAL

The CYBLE-012011-EVAL is the evaluation board for both the CYBLE-012011-00 and the CYBLE-012012-10 EZ-BLE PRoC modules. The CYBLE-012011-EVAL evaluation board contains the CYBLE-012011-00 module.

Figure 128 shows the CYBLE-012011-EVAL connected to the CY8CKIT-042-BLE Kit. The EZ-BLE PRoC Module (CYBLE-012011-00) is shown in the red box in Figure 128.

Figure 128. CYBLE-012011-EVAL (Left) Connected to CY8CKIT-042-BLE (Right)

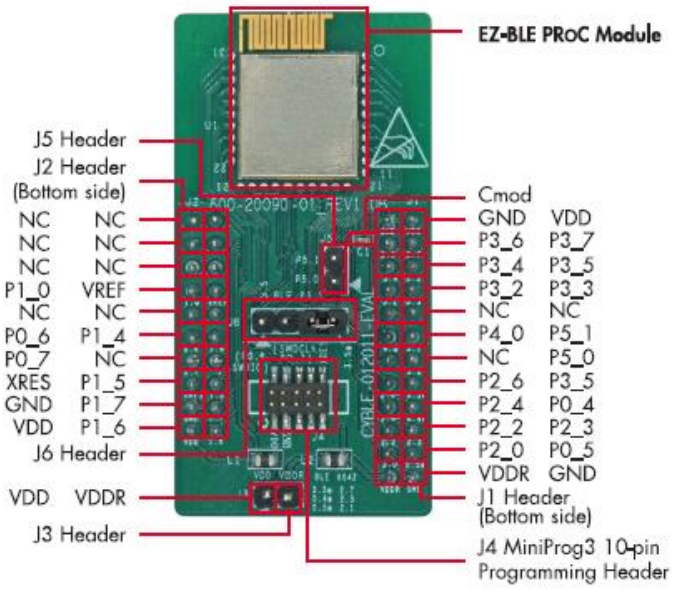


C.1.4.1 CYBLE-012011-EVAL Connections to CY8CKIT-042-BLE

The CYBLE-012011-00 module contains 31 connections on the bottom side of the module. All of these connections are present on the CYBLE-012011-EVAL evaluation board.

Figure 129 shows the CYBLE-012011-EVAL and highlights the elements on the top side of the board. The port-pin connections shown below denote the EZ-BLE module connections on the evaluation board, not the CY8CKIT-042-BLE baseboard connections.

Figure 129. CYBLE-012011-EVAL Board Top Side



Note: Connections denoted as NC (No Connect) indicates that there is no physical connection present between the CYBLE-012011-00 EZ-BLE PRoC Module and the CYBLE-012011-EVAL board J1 and J2 headers.

Note: The EZ-BLE PRoC Module includes only 23 GPIOs. In order to maintain full capability of the CY8CKIT-042-BLE Pioneer Kit functionality, three of the Port-Pin connections do not completely match the CY8CKIT-042-BLE baseboard pin out. See Table 26 for the complete list of GPIOs available on the CYBLE-012011-EVAL and the corresponding Port-Pin connection to the CY8CKIT-042-EVAL baseboard.

The CYBLE-012011-EVAL includes the following elements:

- C_{mod}: A 2.2-nF capacitor mounted on the evaluation board used with the CY8CKIT-042-BLE capacitive sensing slider, buttons, and proximity sensors. C_{mod} is connected to P4[0] on the CYBLE-022001-00 EZ-BLE PRoC Module to enable capacitive sensing when connected to the CY8CKIT-042-BLE Kit.
- J3 Header: A two-pin header that exposes VDD and VDDR. This headers can be used to short the VDDR power connection to VDD. These jumpers must be shorted when using the CYBLE-012011-EVAL with the MiniProg3 kit due to the fact that the MiniProg3 kit only supplies VDD to the evaluation board. When using the CYBLE-012011-EVAL in conjunction with the CY8CKIT-042-BLE Pioneer kit, these jumper connections do not matter, and they can be connected or disconnected.
- J4 Header: A 10-pin header is included on the CYBLE-012011-EVAL kit that exposes connections used for programming and debug with the MiniProg3 kit, as shown in Figure 130. The 10-pin ribbon cable included in the MiniProg3 kit must be used for this connection.

Figure 130. CYBLE-012011-EVAL Using CY8CKIT-002 MiniProg3 and 10-Pin Ribbon Cable

- J5: A header that exposes P5[0] and P5[1], which can be used for I^2C communication (including high-speed I^2C) to the CYBLE-012011-00 EZ-BLE PRoC Module.
- J6 Header: A four-pin header is included on the CYBLE-012011-EVAL kit that exposes the P3[5] connection of the CYBLE-012011-00 module and the P3[5] and P2[7] connections of the CY8CKIT-042-BLE baseboard. Two jumpers are provided to short the connection as needed. Table 25 outlines the four connection options that are possible with the two jumpers provided.

Table 25. J6 Header and Jumper Connection Options

Header Position	1	2	3	4	Resulting Configuration
Header Name (Silkscreen)	"K042 3.5"	"BLE 3.5*"		"K042 2.7"	
Connection Option #1	Short Pin 1 to Pin 2	Short Pin 2 to Pin 1	Open	Open	Module connection P3.5 is routed to the CY8CKIT042-BLE Baseboard P3.5 output.
Connection Option #2	Open	Short Pin 2 to Pin 3	Short Pin 3 to Pin 2	Open	Module connection P3.5 is not routed out to any of the CY8CKIT042-BLE Baseboard outputs. This is not a useful configuration.
Connection Option #3	Open	Open	Short Pin 3 to Pin 4	Short Pin 4 to Pin 3	Module connection P3.5 is routed to the CY8CKIT042-BLE Baseboard P2.7 [SW2] output.
Connection Option #4	Short Pin 1 to Pin 2	Short Pin 2 to Pin 1	Short Pin 3 to Pin 4	Short Pin 4 to Pin 3	Module connection P3.5 is routed to the CY8CKIT042-BLE Baseboard P3.5 AND P2.7 [SW2] output.

For example, if SW2 on the CY8CKIT-042-BLE is desired to be connected to the EZ-BLE module, then configuration #3 in Table 25 should be used.

As mentioned previously, the port-pin connections of the CYBLE-012011-EVAL do not completely match the CY8CKIT-042-BLE baseboard pin out. Three such connections exist on the CYBLE-012011-EVAL that do not align with the CY8CKIT-042-BLE baseboard (highlighted in red in Table 26). Fortunately, PRoC BLE is configurable so that pin functions can be easily re-assigned.

Table 26 details all connections on the CY8CKIT-042-BLE baseboard and provides the equivalent Port-Pin connection on the CYBLE-012011-EVAL board. The port-pin list order is according on the CY8CKIT-042-BLE baseboard physical connection pinout.

Table 26. CYBLE-012011-EVAL Port-Pin Connections to CY8CKIT-042-BLE Baseboard

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-012011-EVAL Connection Port-Pin
J11	P0[0]	NC
J11	P0[1]	NC
J11	P0[2]	NC
J11	P0[3]	NC
J11	P0[4]	NC
J11	P0[5]	NC
J11	VREF	VREF

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-012011-EVAL Connection Port-Pin
J11	P1[0]	P1[0]
J11	P1[1]	NC
J11	P1[2]	NC
J11	P1[4]	P1[4]
J11	P0[6]	P0[6]
J11	P1[3]	NC
J11	P0[7]	P0[7]
J11	P1[5]	P1[5]
J11	XRES	XRES
J11	P1[7]	P1[7]
J11	GND	GND
J11	P1[6]	P1[6]
J11	VDD	VDD
J12	GND	GND
J10	VDD	VDD
J10	P3[6]	P3[6]
J10	P3[7]	P3[7]
J10	P3[4]	P3[4]
J10	P3[5][53]	P3[5][53] / NC
J10	P3[2]	P3[2]
J10	P3[3]	P3[3]
J10	P3[0]	NC
J10	P3[1]	NC
J10	P4[0][31]	NC[31]
J10	P5[1]	P5[1]
J10	P4[1]	NC
J10	P5[0]	P5[0]
J10	P2[6]	P2[6]
J10	P2[7][54]	P3[5] / NC[54]
J10	P2[4]	P2[4]
J10	P2[5]	P0[4]
J10	P2[2]	P2[2]
J10	P2[3]	P2[3]

[53] P3[5] is routed to both P3[5] of the Pioneer kit as well as P2[7] of the pioneer kit. This is done in order to maintain the SW2 switch connection on the baseboard and still allow for DTM mode operation on P3[5]. The J6 header is used to select if P3[5] of the module is routed to P2[7] of the CY8CKIT-042-BLE or to P3[5] of the CY8CKIT-042-BLE

[54] P4[0] is available on the EZ-BLE PRoC Module (CYBLE-012011-00). However, the CYBLE-012011-EVAL board utilizes this pin to connect to the C_{mod} capacitor to enable capacitive sensing functionality on the CY8CKIT-042-BLE Baseboard.

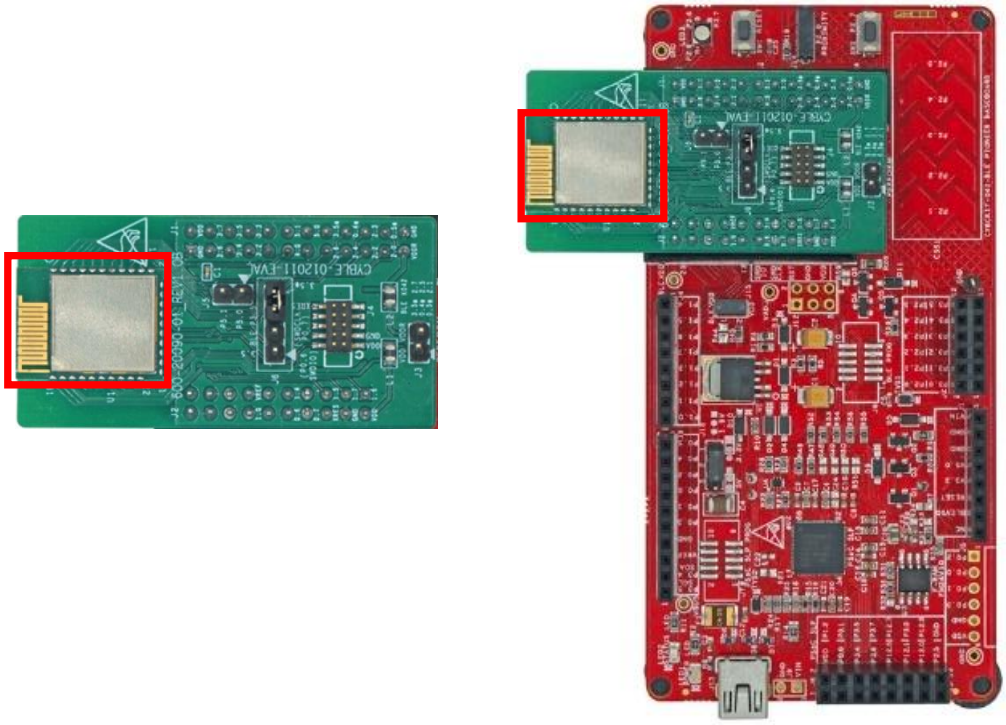
CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-012011-EVAL Connection Port-Pin
J10	P2[0]	P2[0]
J10	P2[1]	P0[5]
J10	VDDR	VDDR
J10	GND	GND

C.1.5 CYBLE-212019-EVAL

The CYBLE-212019-EVAL is the evaluation board for both the CYBLE-212019-00 and the CYBLE-212023-10 EZ-BLE PRoC modules. The CYBLE-212019-EVAL evaluation board contains the CYBLE-212019-00 module.

Figure 131 shows the CYBLE-212019-EVAL connected to the CY8CKIT-042-BLE Kit. The EZ-BLE PRoC Module (CYBLE-212019-00) is shown in the red box in Figure 131.

Figure 131. CYBLE-212019-EVAL (Left) Connected to CY8CKIT-042-BLE (Right)

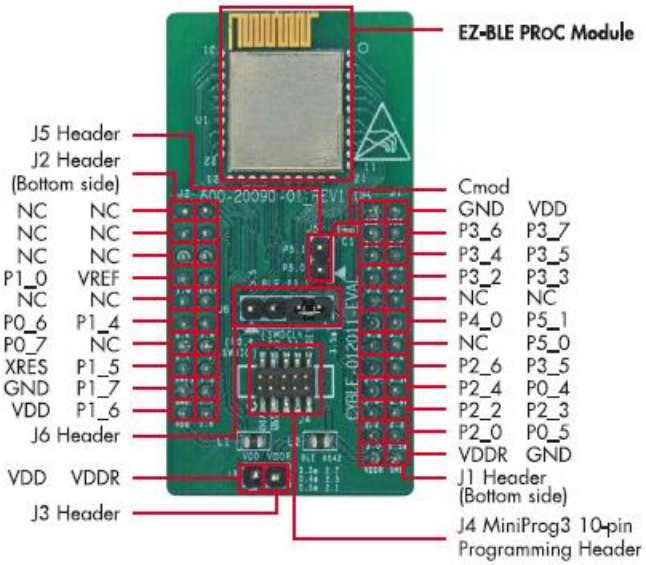


C.1.5.1 CYBLE-212019-EVAL Connections to CY8CKIT-042-BLE

The CYBLE-212019-00 module contains 31 connections on the bottom side of the module. All of these connections are present on the CYBLE-212019-EVAL evaluation board.

Figure 132 shows the CYBLE-212019-EVAL and highlights the elements on the top side of the board. The port-pin connections shown below denote the EZ-BLE module connections on the evaluation board, not the CY8CKIT-042-BLE baseboard connections.

Figure 132. CYBLE-212019-EVAL Board Top Side



Note: Connections denoted as NC (No Connect) indicates that there is no physical connection present between the CYBLE-212019-00 EZ-BLE PRoC Module and the CYBLE-212019-EVAL board J1 and J2 headers.

Note: The EZ-BLE PRoC Module includes only 23 GPIOs. In order to maintain full capability of the CY8CKIT-042-BLE Pioneer Kit functionality, three of the Port-Pin connections do not completely match the CY8CKIT-042-BLE baseboard pin out. See Table 28 for the complete list of GPIOs available on the CYBLE-212019-EVAL and the corresponding Port-Pin connection to the CY8CKIT-042-EVAL baseboard.

The CYBLE-212019-EVAL includes the following elements:

- C_{mod}: A 2.2-nF capacitor mounted on the evaluation board used with the CY8CKIT-042-BLE capacitive sensing slider, buttons, and proximity sensors. C_{mod} is connected to P4[0] on the CYBLE-212019-00 EZ-BLE Module to enable capacitive sensing when connected to the CY8CKIT-042-BLE Kit.
- J3 Header: A two-pin header that exposes VDD and VDDR. This header can be used to short the VDDR power connection to VDD. This jumper must be shorted when using the CYBLE-212019-EVAL with the MiniProg3 kit due to the fact that the MiniProg3 kit only supplies VDD to the evaluation board. When using the CYBLE-212019-EVAL in conjunction with the CY8CKIT-042-BLE Pioneer kit, these jumper connections do not matter, and they can be connected or disconnected.
- J4 Header: A 10-pin header is included on the CYBLE-212019-EVAL kit that exposes connections used for programming and debug with the MiniProg3 kit, as shown in Figure 133. The 10-pin ribbon cable included in the MiniProg3 kit must be used for this connection.

Figure 133. CYBLE-212019-EVAL Using CY8CKIT-002 MiniProg3 and 10-Pin Ribbon Cable

- J5: A header that exposes P5[0] and P5[1], which can be used for I^2C communication (including high-speed I^2C) to the CYBLE-212019-00 EZ-BLE PRoC Module.
- J6 Header: A four-pin header is included on the CYBLE-212019-EVAL kit that exposes the P3[5] connection of the CYBLE-212019-00 module and the P3[5] and P2[7] connections of the CY8CKIT-042-BLE baseboard. Two jumpers are provided to short the connection as needed. Table 27 outlines the four connection options that are possible with the two jumpers provided.

Table 27. J6 Header and Jumper Connection Options

Header Position	1	2	3	4	Resulting Configuration
Header Name (Silkscreen)	"K042 3.5"	"BLE 3.5*"		"K042 2.7"	
Connection Option #1	Short Pin 1 to Pin 2	Short Pin 2 to Pin 1	Open	Open	Module connection P3.5 is routed to the CY8CKIT042-BLE Baseboard P3.5 output.
Connection Option #2	Open	Short Pin 2 to Pin 3	Short Pin 3 to Pin 2	Open	Module connection P3.5 is not routed out to any of the CY8CKIT042-BLE Baseboard outputs. This is not a useful configuration.
Connection Option #3	Open	Open	Short Pin 3 to Pin 4	Short Pin 4 to Pin 3	Module connection P3.5 is routed to the CY8CKIT042-BLE Baseboard P2.7 [SW2] output.
Connection Option #4	Short Pin 1 to Pin 2	Short Pin 2 to Pin 1	Short Pin 3 to Pin 4	Short Pin 4 to Pin 3	Module connection P3.5 is routed to the CY8CKIT042-BLE Baseboard P3.5 AND P2.7 [SW2] output.

For example, if SW2 on the CY8CKIT-042-BLE is desired to be connected to the EZ-BLE module, then configuration #3 in Table 27 should be used.

As mentioned previously, the port-pin connections of the CYBLE-212019-EVAL do not completely match the CY8CKIT-042-BLE baseboard pin out. Three such connections exist on the CYBLE-212019-EVAL that do not align with the CY8CKIT-042-BLE baseboard (highlighted in red in Table 28). Fortunately, PRoC BLE is configurable so that pin functions can be easily re-assigned.

Table 28 details all connections on the CY8CKIT-042-BLE baseboard and provides the equivalent Port-Pin connection on the CYBLE-212019-EVAL board. The port-pin list order is according on the CY8CKIT-042-BLE baseboard physical connection pinout.

Table 28. CYBLE-212019-EVAL Port-Pin Connections to CY8CKIT-042-BLE Baseboard

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-212019-EVAL Connection Port-Pin
J11	P0[0]	NC
J11	P0[1]	NC
J11	P0[2]	NC
J11	P0[3]	NC
J11	P0[4]	NC
J11	P0[5]	NC

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-212019-EVAL Connection Port-Pin
J11	VREF	VREF
J11	P1[0]	P1[0]
J11	P1[1]	NC
J11	P1[2]	NC
J11	P1[4]	P1[4]
J11	P0[6]	P0[6]
J11	P1[3]	NC
J11	P0[7]	P0[7]
J11	P1[5]	P1[5]
J11	XRES	XRES
J11	P1[7]	P1[7]
J11	GND	GND
J11	P1[6]	P1[6]
J11	VDD	VDD
J12	GND	GND
J10	VDD	VDD
J10	P3[6]	P3[6]
J10	P3[7]	P3[7]
J10	P3[4]	P3[4]
J10	P3[5][55]	P3[5][55] / NC
J10	P3[2]	P3[2]
J10	P3[3]	P3[3]
J10	P3[0]	NC
J10	P3[1]	NC
J10	P4[0][34]	NC[34]
J10	P5[1]	P5[1]
J10	P4[1]	NC
J10	P5[0]	P5[0]
J10	P2[6]	P2[6]
J10	P2[7][56]	P3[5] / NC[56]
J10	P2[4]	P2[4]
J10	P2[5]	P0[4]
J10	P2[2]	P2[2]
J10	P2[3]	P2[3]
J10	P2[0]	P2[0]
J10	P2[1]	P0[5]

[55] P3[5] is routed to both P3[5] of the Pioneer kit as well as P2[7] of the pioneer kit. This is done in order to maintain the SW2 switch connection on the baseboard and still allow for DTM mode operation on P3[5]. The J6 header is used to select if P3[5] of the module is routed to P2[7] of the CY8CKIT-042-BLE or to P3[5] of the CY8CKIT-042-BLE

[56] P4[0] is available on the EZ-BLE PRoC Module (CYBLE-212019-00). However, the CYBLE-212019-EVAL board utilizes this pin to connect to the C_{mod} capacitor to enable capacitive sensing functionality on the CY8CKIT-042-BLE Baseboard.

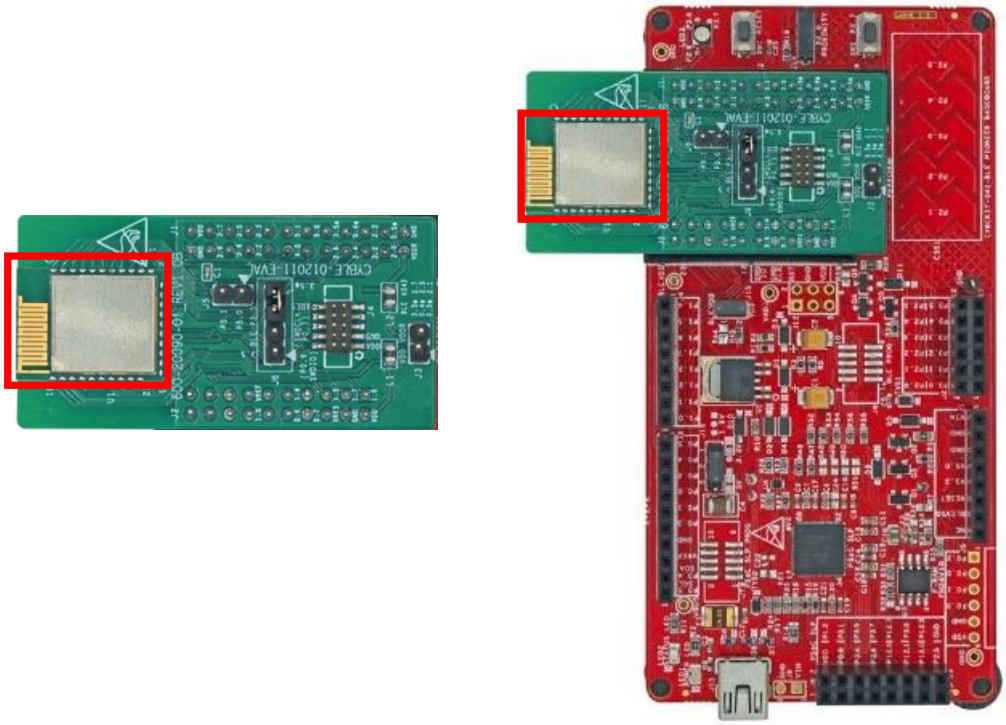
CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-212019-EVAL Connection Port-Pin
J10	VDDR	VDDR
J10	GND	GND

C.1.6 CYBLE-212020-EVAL

The CYBLE-212020-EVAL is the evaluation board for the CYBLE-212020-01 EZ-BLE module.

Figure 134 shows the CYBLE-212020-EVAL connected to the CY8CKIT-042-BLE Kit. The EZ-BLE Module (CYBLE-212020-01) is shown in the red box in Figure 134.

Figure 134. CYBLE-212020-EVAL (Left) Connected to CY8CKIT-042-BLE (Right)

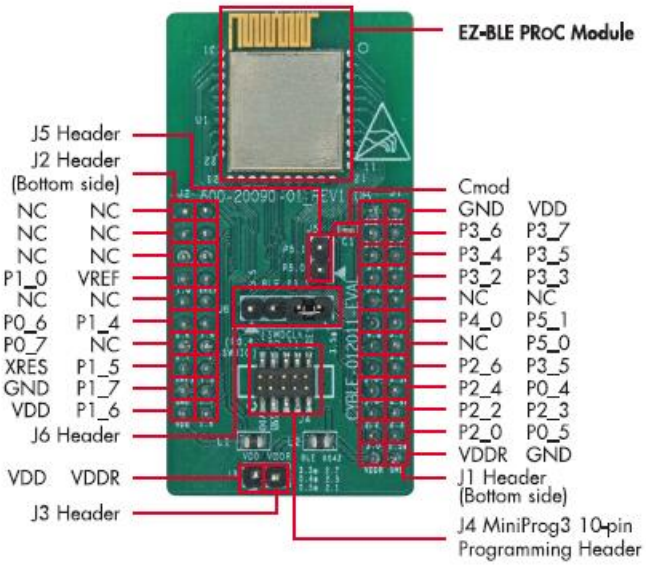


C.1.6.1 CYBLE-212020-EVAL Connections to CY8CKIT-042-BLE

The CYBLE-212020-00 module contains 31 connections on the bottom side of the module. All of these connections are present on the CYBLE-212020-EVAL evaluation board.

Figure 135 shows the CYBLE-212020-EVAL and highlights the elements on the top side of the board. The port-pin connections shown below denote the EZ-BLE module connections on the evaluation board, not the CY8CKIT-042-BLE-A baseboard connections.

Figure 135. CYBLE-212020-EVAL Board Top Side



Note: Connections denoted as NC (No Connect) indicates that there is no physical connection present between the CYBLE-212020-01 EZ-BLE Module and the CYBLE-212020-EVAL board J1 and J2 headers.

Note: The EZ-BLE Module includes only 23 GPIOs. In order to maintain full capability of the CY8CKIT-042-BLE Pioneer Kit functionality, three of the Port-Pin connections do not completely match the CY8CKIT-042-BLE baseboard pin out. See Table 29 for the complete list of GPIOs available on the CYBLE-212020-EVAL and the corresponding Port-Pin connection to the CY8CKIT-042-EVAL baseboard.

The CYBLE-212020-EVAL includes the following elements:

- C_{mod}: A 2.2-nF capacitor mounted on the evaluation board used with the CY8CKIT-042-BLE capacitive sensing slider, buttons, and proximity sensors. C_{mod} is connected to P4[0] on the CYBLE-212020-01 EZ-BLE Module to enable capacitive sensing when connected to the CY8CKIT-042-BLE Kit.
- J3 Header: A two-pin header that exposes VDD and VDDR. This header can be used to short the VDDR power connection to VDD. This jumper must be shorted when using the CYBLE-212020-EVAL with the MiniProg3 kit due to the fact that the MiniProg3 kit only supplies VDD to the evaluation board. When using the CYBLE-212020-EVAL in conjunction with the CY8CKIT-042-BLE Pioneer kit, these jumper connections do not matter, and they can be connected or disconnected.
- J4 Header: A 10-pin header is included on the CYBLE-212020-EVAL kit that exposes connections used for programming and debug with the MiniProg3 kit, as shown in Figure 136. The 10-pin ribbon cable included in the MiniProg3 kit must be used for this connection.

Figure 136. CYBLE-212020-EVAL Using CY8CKIT-002 MiniProg3 and 10-Pin Ribbon Cable

As mentioned previously, the port-pin connections of the CYBLE-212020-EVAL do not completely match the CY8CKIT-042-BLE baseboard pin out. Three such connections exist on the CYBLE-212020-EVAL that do not align with the CY8CKIT-042-BLE baseboard (highlighted in red in Table 29). Fortunately, Cypress BLE silicon is configurable so that pin functions can be easily re-assigned.

Table 29 details all connections on the CY8CKIT-042-BLE baseboard and provides the equivalent Port-Pin connection on the CYBLE-212020-EVAL board. The port-pin list order is according on the CY8CKIT-042-BLE baseboard physical connection pinout.

Table 29. CYBLE-212020-EVAL Port-Pin Connections to CY8CKIT-042-BLE Baseboard

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-212020-EVAL Connection Port-Pin
J11	P0[0]	NC
J11	P0[1]	NC
J11	P0[2]	NC
J11	P0[3]	NC
J11	P0[4]	NC
J11	P0[5]	NC
J11	VREF	VREF
J11	P1[0]	P1[0]
J11	P1[1]	NC
J11	P1[2]	NC
J11	P1[4]	P1[4]
J11	P0[6]	P0[6]
J11	P1[3]	NC
J11	P0[7]	P0[7]
J11	P1[5]	P1[5]
J11	XRES	XRES
J11	P1[7]	P1[7]
J11	GND	GND
J11	P1[6]	P1[6]
J11	VDD	VDD
J12	GND	GND
J10	VDD	VDD
J10	P3[6]	P3[6]
J10	P3[7]	P3[7]
J10	P3[4]	P3[4]

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-212020-EVAL Connection Port-Pin
J10	P3[5][57]	P3[5][55] / NC
J10	P3[2]	P3[2]
J10	P3[3]	P3[3]
J10	P3[0]	NC
J10	P3[1]	NC
J10	P4[0][34]	NC[34]
J10	P5[1]	P5[1]
J10	P4[1]	NC
J10	P5[0]	P5[0]
J10	P2[6]	P2[6]
J10	P2[7][58]	P3[5] / NC[56]
J10	P2[4]	P2[4]
J10	P2[5]	P0[4]
J10	P2[2]	P2[2]
J10	P2[3]	P2[3]
J10	P2[0]	P2[0]
J10	P2[1]	P0[5]
J10	VDDR	VDDR
J10	GND	GND

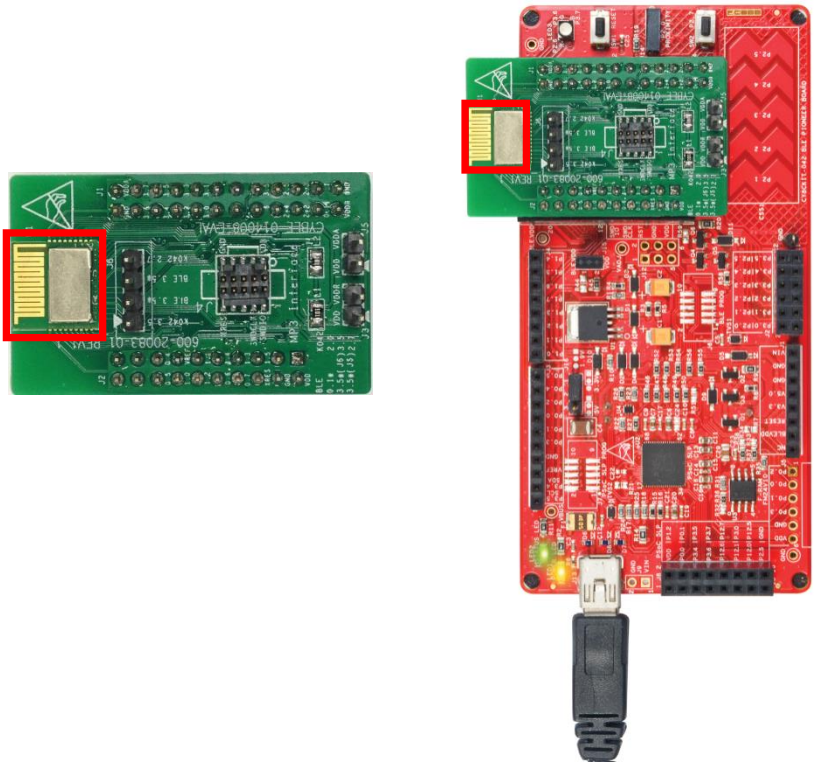
[57] P3[5] is routed to both P3[5] of the Pioneer kit as well as P2[7] of the pioneer kit. This is done in order to maintain the SW2 switch connection on the baseboard and still allow for DTM mode operation on P3[5]. The J6 header is used to select if P3[5] of the module is routed to P2[7] of the CY8CKIT-042-BLE or to P3[5] of the CY8CKIT-042-BLE

[58] P4[0] is available on the EZ-BLE PRoC Module (CYBLE-212020-01). However, the CYBLE-212020-EVAL board utilizes this pin to connect to the C_{mod} capacitor to enable capacitive sensing functionality on the CY8CKIT-042-BLE Baseboard.

C.1.7 CYBLE-014008-EVAL

Figure 137 shows the CYBLE-014008-EVAL connected to the CY8CKIT-042-BLE Kit. The EZ-BLE PSoC Module (CYBLE-014008-00) is shown in the red box in Figure 137.

Figure 137. CYBLE-014008-EVAL (Left) Connected to CY8CKIT-042-BLE (Right)

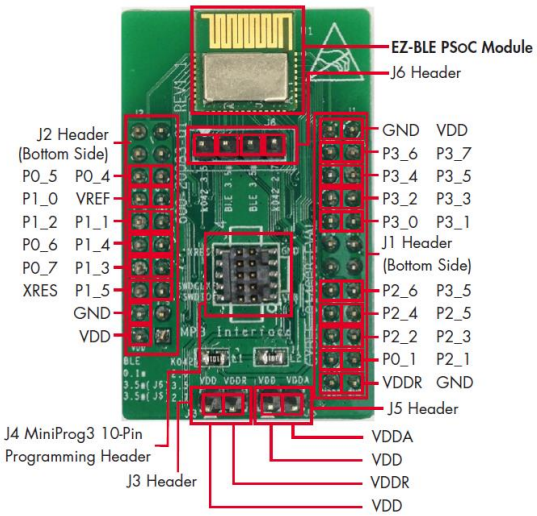


C.1.7.1 CYBLE-014008-EVAL Connections to CY8CKIT-042-BLE

The CYBLE-014008-00 module contains 32 connections on the bottom side of the module. All of these connections are present on the CYBLE-014008-EVAL evaluation board.

Figure 138 shows the CYBLE-014008-EVAL and highlights the elements on the top side of the board. The port-pin connections shown below denote the EZ-BLE module connections on the evaluation board, not the CY8CKIT-042-BLE baseboard connections.

Figure 138. CYBLE-014008-EVAL Board Top Side



Note: Connections not called out on J1 and J2 connection headers are NC (No Connect), where no physical connection is present between the CYBLE-014008-00 EZ-BLE PSoC Module and the CYBLE-014008-EVAL board J1 and J2 headers.

Note: The EZ-BLE PSoC Module includes only 25 GPIOs. In order to maintain full capability of the CY8CKIT-042-BLE Pioneer Kit functionality, three of the Port-Pin connections do not completely match the CY8CKIT-042-BLE baseboard pin out. See Table 31 for the complete list of GPIOs available on the CYBLE-014008-EVAL and the corresponding Port-Pin connection to the CY8CKIT-042-EVAL baseboard.

The CYBLE-014008-EVAL includes the following elements:

- J3 and J5 Header: 2x two-pin headers that exposes VDD, VDDA and VDDR. These headers can be used to short the VDDA and VDDR power connections to VDD. These jumpers must be shorted when using the CYBLE-014008-EVAL with the MiniProg3 kit due to the fact that the MiniProg3 kit only supplies VDD to the evaluation board. When using the CYBLE-014008-EVAL in conjunction with the CY8CKIT-042-BLE Pioneer kit, these jumper connections do not matter, and they can be connected or disconnected.
- J4 Header: A 10-pin header is included on the CYBLE-014008-EVAL kit that exposes connections used for programming and debug with the MiniProg3 kit, as shown in Figure 139. The 10-pin ribbon cable included in the MiniProg3 kit must be used for this connection.

Figure 139. CYBLE-014008-EVAL Using CY8CKIT-002 MiniProg3 and 10-Pin Ribbon Cable

- J6 Header: A four-pin header is included on the CYBLE-014008-EVAL kit that exposes the P3[5] connection of the CYBLE-014008-00 module and the P3[5] and P2[7] connections of the CY8CKIT-042-BLE baseboard. Two jumpers are provided to short the connection as needed. Table 30 outlines the four connection options that are possible with the two jumpers provided.

Table 30. J6 Header and Jumper Connection Options

Header Position	1	2	3	4	Resulting Configuration
Header Name (Silkscreen)	"K042 3.5"	"BLE 3.5*"		"K042 2.7"	
Connection Option #1	Short Pin 1 to Pin 2	Short Pin 2 to Pin 1	Open	Open	Module connection P3.5 is routed to the CY8CKIT042-BLE Baseboard P3.5 output.
Connection Option #2	Open	Short Pin 2 to Pin 3	Short Pin 3 to Pin 2	Open	Module connection P3.5 is not routed out to any of the CY8CKIT042-BLE Baseboard outputs. This is not a useful configuration.
Connection Option #3	Open	Open	Short Pin 3 to Pin 4	Short Pin 4 to Pin 3	Module connection P3.5 is routed to the CY8CKIT042-BLE Baseboard P2.7 [SW2] output.
Connection Option #4	Short Pin 1 to Pin 2	Short Pin 2 to Pin 1	Short Pin 3 to Pin 4	Short Pin 4 to Pin 3	Module connection P3.5 is routed to the CY8CKIT042-BLE Baseboard P3.5 AND P2.7 [SW2] output.

For example, if SW2 on the CY8CKIT-042-BLE is desired to be connected to the EZ-BLE module, then configuration #3 in Table 30 should be used.

As mentioned previously, the port-pin connections of the CYBLE-014008-EVAL do not completely match the CY8CKIT-042-BLE baseboard pin out. Three such connections exist on the CYBLE-014008-EVAL that do not align with the CY8CKIT-042-BLE baseboard (highlighted in red in Table 31). Fortunately, PSoC BLE is configurable so that pin functions can be easily re-assigned. Note: P3[5] of the CYBLE-014008-00 module is routed to both the P3[5] and P2[7] CY8CKIT-042-BLE baseboard connections as stated in the J6 header description.

Table 31 details all connections on the CY8CKIT-042-BLE baseboard and provides the equivalent Port-Pin connection on the CYBLE-014008-EVAL board. The port-pin list order is according on the CY8CKIT-042-BLE baseboard physical connection pinout.

Table 31. CYBLE-014008-EVAL Port-Pin Connections to CY8CKIT-042-BLE Baseboard

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-014008-EVAL Connection Port-Pin
J11	P0[0]	NC
J11	P0[1][59]	NC
J11	P0[2]	NC
J11	P0[3]	NC
J11	P0[4]	P0[4]
J11	P0[5]	P0[5]
J11	VREF	VREF
J11	P1[0]	P1[0]
J11	P1[1]	P1[1]
J11	P1[2]	P1[2]
J11	P1[4]	P1[4]
J11	P0[6]	P0[6]
J11	P1[3]	P1[3]
J11	P0[7]	P0[7]
J11	P1[5]	P1[5]
J11	XRES	XRES
J11	P1[7]	NC
J11	GND	GND
J11	P1[6]	NC
J11	VDD	VDD
J12	GND	GND
J10	VDD	VDD
J10	P3[6]	P3[6]
J10	P3[7]	P3[7]
J10	P3[4]	P3[4]
J10	P3[5][60]	P3[5][60] / NC
J10	P3[2]	P3[2]
J10	P3[3]	P3[3]
J10	P3[0]	P3[0]
J10	P3[1]	P3[1]
J10	P4[0][61]	NC[61]

[59] P0[1] is routed to the P2[0] connection on the CY8CKIT-042-BLE baseboard in order to allow for connection to the Proximity Sensor element on the baseboard (if desired).

[60] P3[5] is routed to both P3[5] of the Pioneer kit as well as P2[7] of the pioneer kit. This is done in order to maintain the SW2 switch connection on the baseboard and still allow for DTM mode operation on P3[5]. The J6 header is used to select if P3[5] of the module is routed to P2[7] of the CY8CKIT-042-BLE or to P3[5] of the CY8CKIT-042-BLE.

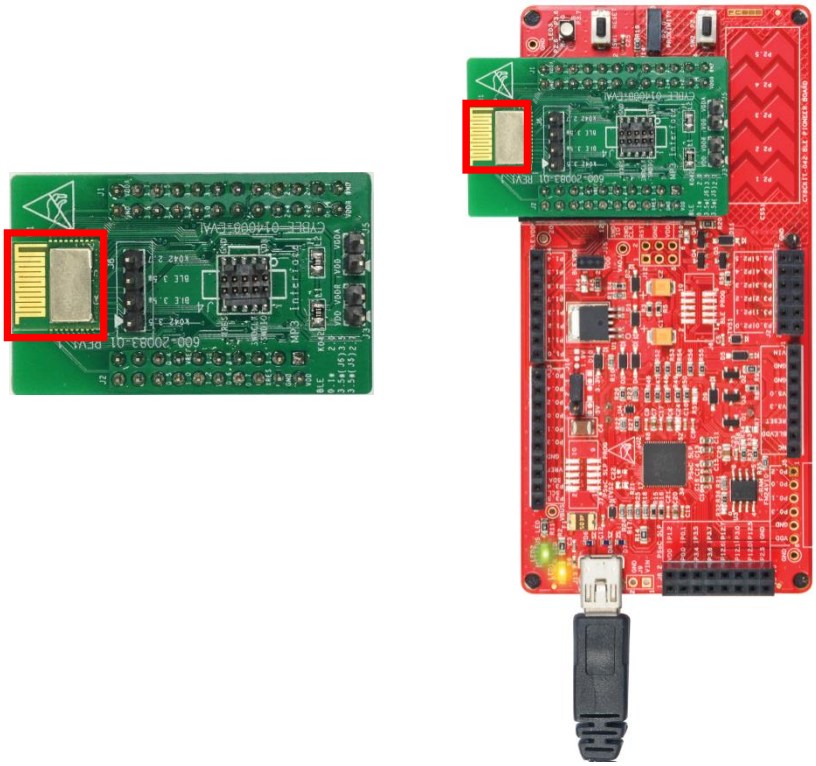
[61] P4[0] and P4[1] are connected on the PSoC4A BLE Module to an on-board 2.2nF and 10nF capacitor respectively, so they are not available on the module or the CYBLE-014008-EVAL board for connection.

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-014008-EVAL Connection Port-Pin
J10	P5[1]	P5[1]
J10	P4[1][61]	NC[61]
J10	P5[0]	P5[0]
J10	P2[6]	P2[6]
J10	P2[7]	P3[5] / NC
J10	P2[4]	P2[4]
J10	P2[5]	P2[5]
J10	P2[2]	P2[2]
J10	P2[3]	P2[3]
J10	P2[0][59]	P0[1][59]
J10	P2[1]	P2[1]
J10	VDDR	VDDR
J10	GND	GND

C.1.8 CYBLE-214009-EVAL

Figure 140 shows the CYBLE-214009-EVAL connected to the CY8CKIT-042-BLE Kit. The EZ-BLE PSoC Module (CYBLE-214009-00) is shown in the red box in Figure 140.

Figure 140. CYBLE-214009-EVAL (Left) Connected to CY8CKIT-042-BLE (Right)

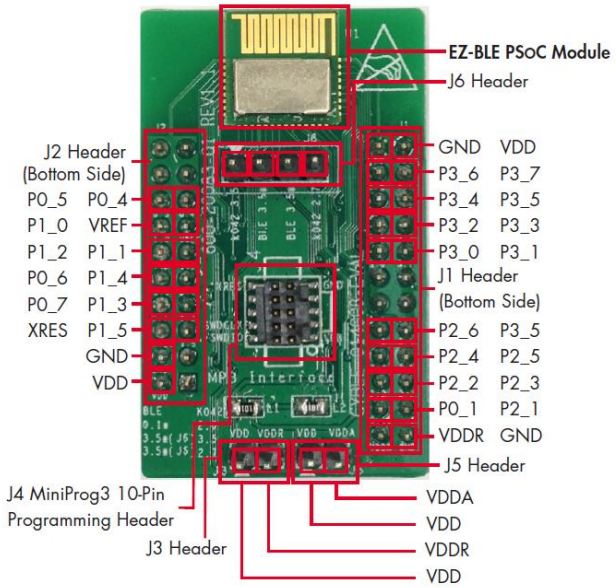


C.1.8.1 CYBLE-214009-EVAL Connections to CY8CKIT-042-BLE

The CYBLE-214009-00 module contains 32 connections on the bottom side of the module. All of these connections are present on the CYBLE-214009-EVAL evaluation board.

Figure 141 shows the CYBLE-214009-EVAL and highlights the elements on the top side of the board. The port-pin connections shown below denote the EZ-BLE module connections on the evaluation board, not the CY8CKIT-042-BLE baseboard connections.

Figure 141. CYBLE-214009-EVAL Board Top Side



Note: Connections not called out on J1 and J2 connection headers are NC (No Connect), where no physical connection is present between the CYBLE-214009-00 EZ-BLE PSoC Module and the CYBLE-214009-EVAL board J1 and J2 headers.

Note: The EZ-BLE PSoC Module includes only 25 GPIOs. In order to maintain full capability of the CY8CKIT-042-BLE Pioneer Kit functionality, three of the Port-Pin connections do not completely match the CY8CKIT-042-BLE baseboard pin out. See Table 33 for the complete list of GPIOs available on the CYBLE-214009-EVAL and the corresponding Port-Pin connection to the CY8CKIT-042-EVAL baseboard.

The CYBLE-214009-EVAL includes the following elements:

- J3 and J5 Header: 2x two-pin headers that exposes VDD, VDDA and VDDR. These headers can be used to short the VDDA and VDDR power connections to VDD. These jumpers must be shorted when using the CYBLE-214009-EVAL with the MiniProg3 kit due to the fact that the MiniProg3 kit only supplies VDD to the evaluation board. When using the CYBLE-214009-EVAL in conjunction with the CY8CKIT-042-BLE Pioneer kit, these jumper connections do not matter, and they can be connected or disconnected.
- J4 Header: A 10-pin header is included on the CYBLE-214009-EVAL kit that exposes connections used for programming and debug with the MiniProg3 kit, as shown in Figure 142. The 10-pin ribbon cable included in the MiniProg3 kit must be used for this connection.

Figure 142. CYBLE-214009-EVAL Using CY8CKIT-002 MiniProg3 and 10-Pin Ribbon Cable

- J6 Header: A four-pin header is included on the CYBLE-214009-EVAL kit that exposes the P3[5] connection of the CYBLE-214009-00 module and the P3[5] and P2[7] connections of the CY8CKIT-042-BLE baseboard. Two jumpers are provided to short the connection as needed. Table 32 outlines the four connection options that are possible with the two jumpers provided.

Table 32. J6 Header and Jumper Connection Options

Header Position	1	2	3	4	Resulting Configuration
Header Name (Silkscreen)	"K042 3.5"	"BLE 3.5*"		"K042 2.7"	
Connection Option #1	Short Pin 1 to Pin 2	Short Pin 2 to Pin 1	Open	Open	Module connection P3.5 is routed to the CY8CKIT042-BLE Baseboard P3.5 output.
Connection Option #2	Open	Short Pin 2 to Pin 3	Short Pin 3 to Pin 2	Open	Module connection P3.5 is not routed out to any of the CY8CKIT042-BLE Baseboard outputs. This is not a useful configuration.
Connection Option #3	Open	Open	Short Pin 3 to Pin 4	Short Pin 4 to Pin 3	Module connection P3.5 is routed to the CY8CKIT042-BLE Baseboard P2.7 [SW2] output.
Connection Option #4	Short Pin 1 to Pin 2	Short Pin 2 to Pin 1	Short Pin 3 to Pin 4	Short Pin 4 to Pin 3	Module connection P3.5 is routed to the CY8CKIT042-BLE Baseboard P3.5 AND P2.7 [SW2] output.

For example, if SW2 on the CY8CKIT-042-BLE is desired to be connected to the EZ-BLE module, then configuration #3 in Table 32 should be used.

As mentioned previously, the port-pin connections of the CYBLE-214009-EVAL do not completely match the CY8CKIT-042-BLE baseboard pin out. Three such connections exist on the CYBLE-214009-EVAL that do not align with the CY8CKIT-042-BLE baseboard (highlighted in red in Table 33). Fortunately, PSoC BLE is configurable so that pin functions can be easily re-assigned. Note: P3[5] of the CYBLE-214009-00 module is routed to both the P3[5] and P2[7] CY8CKIT-042-BLE baseboard connections as stated in the J6 header description.

Table 33 details all connections on the CY8CKIT-042-BLE baseboard and provides the equivalent Port-Pin connection on the CYBLE-214009-EVAL board. The port-pin list order is according on the CY8CKIT-042-BLE baseboard physical connection pinout.

Table 33. CYBLE-214009-EVAL Port-Pin Connections to CY8CKIT-042-BLE Baseboard

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-214009-EVAL Connection Port-Pin
J11	P0[0]	NC
J11	P0[1][62]	NC
J11	P0[2]	NC
J11	P0[3]	NC
J11	P0[4]	P0[4]
J11	P0[5]	P0[5]
J11	VREF	VREF
J11	P1[0]	P1[0]
J11	P1[1]	P1[1]
J11	P1[2]	P1[2]
J11	P1[4]	P1[4]
J11	P0[6]	P0[6]
J11	P1[3]	P1[3]
J11	P0[7]	P0[7]
J11	P1[5]	P1[5]

[62] P0[1] is routed to the P2[0] connection on the CY8CKIT-042-BLE baseboard in order to allow for connection to the Proximity Sensor element on the baseboard (if desired).

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-214009-EVAL Connection Port-Pin
J11	XRES	XRES
J11	P1[7]	NC
J11	GND	GND
J11	P1[6]	NC
J11	VDD	VDD
J12	GND	GND
J10	VDD	VDD
J10	P3[6]	P3[6]
J10	P3[7]	P3[7]
J10	P3[4]	P3[4]
J10	P3[5][63]	P3[5][63] / NC
J10	P3[2]	P3[2]
J10	P3[3]	P3[3]
J10	P3[0]	P3[0]
J10	P3[1]	P3[1]
J10	P4[0][64]	NC[64]
J10	P5[1]	P5[1]
J10	P4[1][64]	NC[64]
J10	P5[0]	P5[0]
J10	P2[6]	P2[6]
J10	P2[7]	P3[5] / NC
J10	P2[4]	P2[4]
J10	P2[5]	P2[5]
J10	P2[2]	P2[2]
J10	P2[3]	P2[3]
J10	P2[0][62]	P0[1][62]
J10	P2[1]	P2[1]
J10	VDDR	VDDR
J10	GND	GND

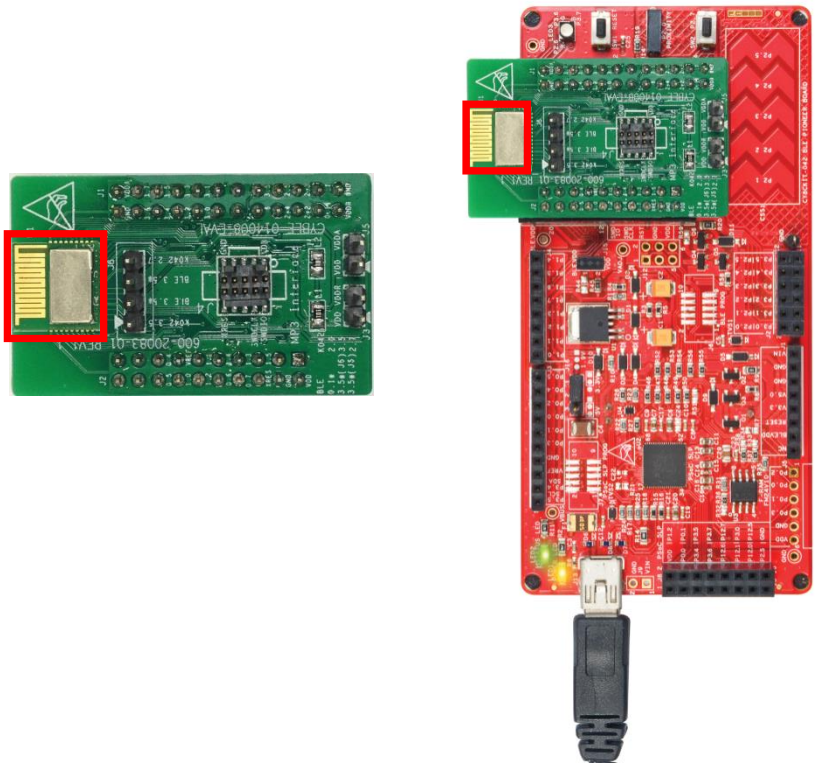
C.1.9 CYBLE-214015-EVAL

Figure 143 shows the CYBLE-214015-EVAL connected to the CY8CKIT-042-BLE Kit. The EZ-BLE Module (CYBLE-214015-01) is shown in the red box in Figure 143.

[63] P3[5] is routed to both P3[5] of the Pioneer kit as well as P2[7] of the pioneer kit. This is done in order to maintain the SW2 switch connection on the baseboard and still allow for DTM mode operation on P3[5]. The J6 header is used to select if P3[5] of the module is routed to P2[7] of the CY8CKIT-042-BLE or to P3[5] of the CY8CKIT-042-BLE

[64] P4[0] and P4[1] are connected on the PSoC4A BLE Module to an on-board 2.2nF and 10nF capacitor respectively, so they are not available on the module or the CYBLE-214009-EVAL board for connection.

Figure 143. CYBLE-214015-EVAL (Left) Connected to CY8CKIT-042-BLE (Right)

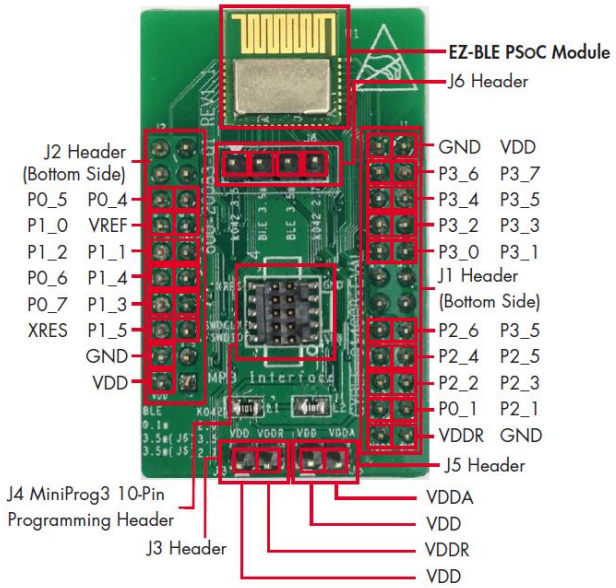


C.1.9.1 CYBLE-214015-EVAL Connections to CY8CKIT-042-BLE

The CYBLE-214015-01 module contains 32 connections on the bottom side of the module. All of these connections are present on the CYBLE-214015-EVAL evaluation board.

Figure 144 shows the CYBLE-214015-EVAL and highlights the elements on the top side of the board. The port-pin connections shown below denote the EZ-BLE module connections on the evaluation board, not the CY8CKIT-042-BLE baseboard connections.

Figure 144. CYBLE-214015-EVAL Board Top Side



Note: Connections not called out on J1 and J2 connection headers are NC (No Connect), where no physical connection is present between the CYBLE-214015-01 EZ-BLE PSoC Module and the CYBLE-214015-EVAL board J1 and J2 headers.

Note: The EZ-BLE PSoC Module includes only 25 GPIOs. In order to maintain full capability of the CY8CKIT-042-BLE Pioneer Kit functionality, three of the Port-Pin connections do not completely match the CY8CKIT-042-BLE baseboard pin out. See Table 35 for the complete list of GPIOs available on the CYBLE-214015-EVAL and the corresponding Port-Pin connection to the CY8CKIT-042-EVAL baseboard.

The CYBLE-214015-EVAL includes the following elements:

- J3 and J5 Header: 2x two-pin headers that exposes VDD, VDDA and VDDR. These headers can be used to short the VDDA and VDDR power connections to VDD. These jumpers must be shorted when using the CYBLE-214015-EVAL with the MiniProg3 kit due to the fact that the MiniProg3 kit only supplies VDD to the evaluation board. When using the CYBLE-214015-EVAL in conjunction with the CY8CKIT-042-BLE Pioneer kit, these jumper connections do not matter, and they can be connected or disconnected.
- J4 Header: A 10-pin header is included on the CYBLE-214015-EVAL kit that exposes connections used for programming and debug with the MiniProg3 kit, as shown in Figure 145. The 10-pin ribbon cable included in the MiniProg3 kit must be used for this connection.

Figure 145. CYBLE-214015-EVAL Using CY8CKIT-002 MiniProg3 and 10-Pin Ribbon Cable

- J6 Header: A four-pin header is included on the CYBLE-214015-EVAL kit that exposes the P3[5] connection of the CYBLE-214015-01 module and the P3[5] and P2[7] connections of the CY8CKIT-042-BLE baseboard. Two jumpers are provided to short the connection as needed. Table 34 outlines the four connection options that are possible with the two jumpers provided.

Table 34. J6 Header and Jumper Connection Options

Header Position	1	2	3	4	Resulting Configuration
Header Name (Silkscreen)	"K042 3.5"	"BLE 3.5*"		"K042 2.7"	
Connection Option #1	Short Pin 1 to Pin 2	Short Pin 2 to Pin 1	Open	Open	Module connection P3.5 is routed to the CY8CKIT042-BLE Baseboard P3.5 output.
Connection Option #2	Open	Short Pin 2 to Pin 3	Short Pin 3 to Pin 2	Open	Module connection P3.5 is not routed out to any of the CY8CKIT042-BLE Baseboard outputs. This is not a useful configuration.
Connection Option #3	Open	Open	Short Pin 3 to Pin 4	Short Pin 4 to Pin 3	Module connection P3.5 is routed to the CY8CKIT042-BLE Baseboard P2.7 [SW2] output.
Connection Option #4	Short Pin 1 to Pin 2	Short Pin 2 to Pin 1	Short Pin 3 to Pin 4	Short Pin 4 to Pin 3	Module connection P3.5 is routed to the CY8CKIT042-BLE Baseboard P3.5 AND P2.7 [SW2] output.

For example, if SW2 on the CY8CKIT-042-BLE is desired to be connected to the EZ-BLE module, then configuration #3 in Table 34 should be used.

As mentioned previously, the port-pin connections of the CYBLE-214015-EVAL do not completely match the CY8CKIT-042-BLE baseboard pin out. Three such connections exist on the CYBLE-214015-EVAL that do not align with the CY8CKIT-042-BLE baseboard (highlighted in red in Table 35). Fortunately, PSoC BLE is configurable so that pin functions can be easily re-assigned. Note: P3[5] of the CYBLE-214015-01 module is routed to both the P3[5] and P2[7] CY8CKIT-042-BLE baseboard connections as stated in the J6 header description.

Table 35 details all connections on the CY8CKIT-042-BLE baseboard and provides the equivalent Port-Pin connection on the CYBLE-214015-EVAL board. The port-pin list order is according on the CY8CKIT-042-BLE baseboard physical connection pinout.

Table 35. CYBLE-214015-EVAL Port-Pin Connections to CY8CKIT-042-BLE Baseboard

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-214015-EVAL Connection Port-Pin
J11	P0[0]	NC
J11	P0[1][65]	NC
J11	P0[2]	NC
J11	P0[3]	NC
J11	P0[4]	P0[4]
J11	P0[5]	P0[5]
J11	VREF	VREF
J11	P1[0]	P1[0]
J11	P1[1]	P1[1]
J11	P1[2]	P1[2]
J11	P1[4]	P1[4]
J11	P0[6]	P0[6]
J11	P1[3]	P1[3]
J11	P0[7]	P0[7]
J11	P1[5]	P1[5]

[65] P0[1] is routed to the P2[0] connection on the CY8CKIT-042-BLE baseboard in order to allow for connection to the Proximity Sensor element on the baseboard (if desired).

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-214015-EVAL Connection Port-Pin
J11	XRES	XRES
J11	P1[7]	NC
J11	GND	GND
J11	P1[6]	NC
J11	VDD	VDD
J12	GND	GND
J10	VDD	VDD
J10	P3[6]	P3[6]
J10	P3[7]	P3[7]
J10	P3[4]	P3[4]
J10	P3[5][66]	P3[5][63] / NC
J10	P3[2]	P3[2]
J10	P3[3]	P3[3]
J10	P3[0]	P3[0]
J10	P3[1]	P3[1]
J10	P4[0][67]	NC[64]
J10	P5[1]	P5[1]
J10	P4[1][64]	NC[64]
J10	P5[0]	P5[0]
J10	P2[6]	P2[6]
J10	P2[7]	P3[5] / NC
J10	P2[4]	P2[4]
J10	P2[5]	P2[5]
J10	P2[2]	P2[2]
J10	P2[3]	P2[3]
J10	P2[0][62]	P0[1][62]
J10	P2[1]	P2[1]
J10	VDDR	VDDR
J10	GND	GND

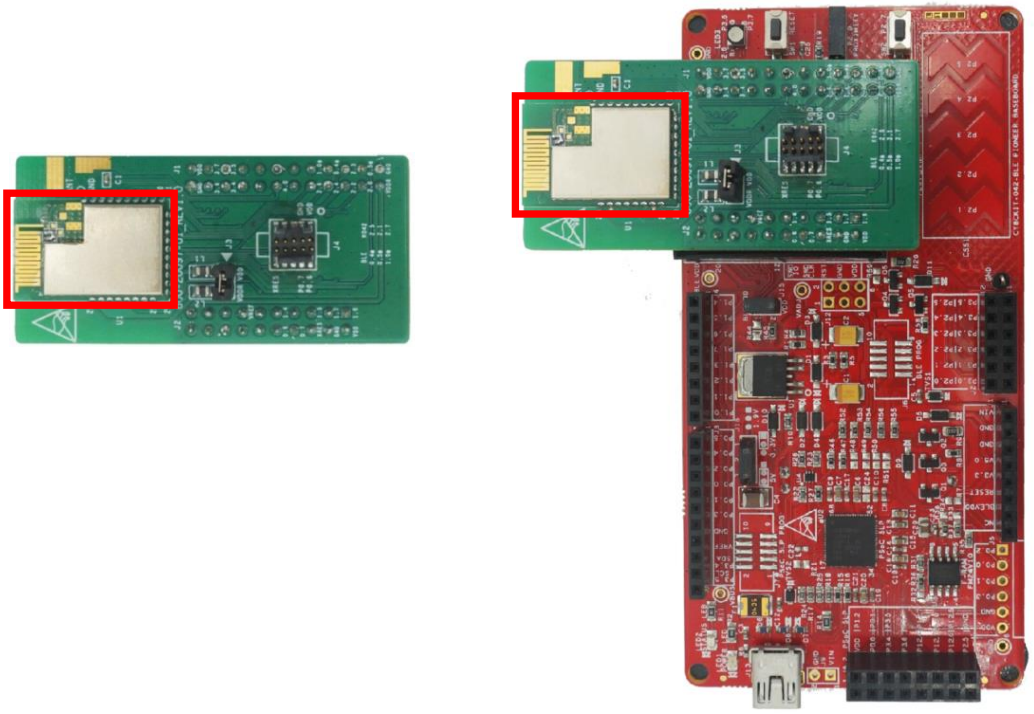
[66] P3[5] is routed to both P3[5] of the Pioneer kit as well as P2[7] of the pioneer kit. This is done in order to maintain the SW2 switch connection on the baseboard and still allow for DTM mode operation on P3[5]. The J6 header is used to select if P3[5] of the module is routed to P2[7] of the CY8CKIT-042-BLE or to P3[5] of the CY8CKIT-042-BLE

[67] P4[0] and P4[1] are connected on the PSoC4A BLE Module to an on-board 2.2nF and 10nF capacitor respectively, so they are not available on the module or the CYBLE-214009-EVAL board for connection.

C.1.10 CYBLE-2X20XX-EVAL

Figure 146 shows the CYBLE-212006-EVAL connected to the CY8CKIT-042-BLE Kit. The EZ-BLE Module (CYBLE-212006-01) is shown in the red box in Figure 146. The CYBLE-212006-EVAL (integrated antenna), CYBLE-202007-EVAL (u.FL antenna connector), and the CYBLE-202013-EVAL (antenna solder pad) all have the same form, however, the antenna implementation differs as stated in the specific evaluation board's quick start guide. All other information for these kits is the same as described in this section.

Figure 146. CYBLE-212006-EVAL (Left) Connected to CY8CKIT-042-BLE (Right)

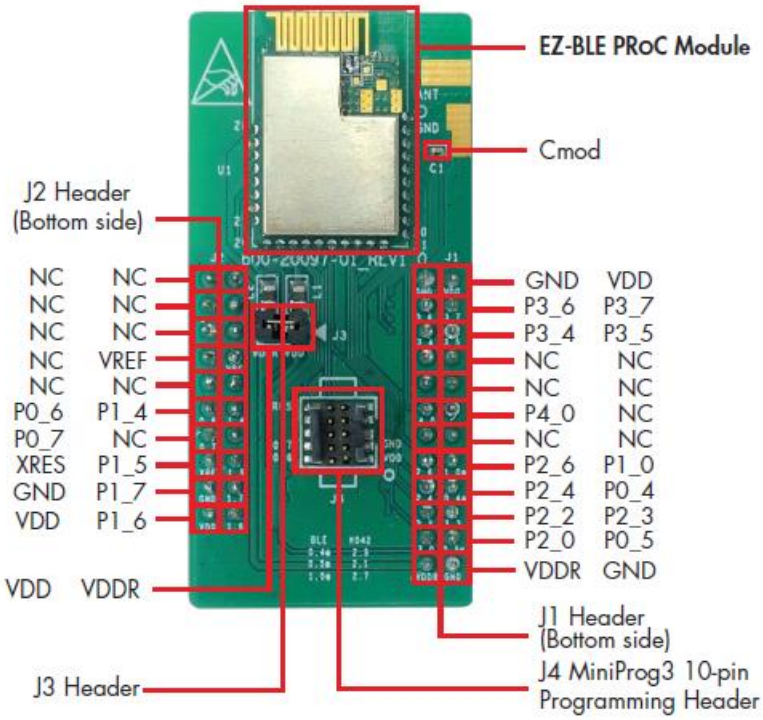


C.1.10.1 CYBLE-212006-EVAL Connections to CY8CKIT-042-BLE

The CYBLE-212006-01 module contains 30 connections on the bottom side of the module. All of these connections are present on the CYBLE-212006-EVAL evaluation board.

Figure 147 shows the CYBLE-212006-EVAL and highlights the elements on the top side of the board. The port-pin connections shown below denote the EZ-BLE module connections on the evaluation board, not the CY8CKIT-042-BLE baseboard connections.

Figure 147. CYBLE-212006-EVAL Board Top Side



Note: Connections called out on J1 and J2 connection headers as NC (No Connect) have no physical connection present between the CYBLE-212006-01 EZ-BLE Module and the CYBLE-212006-EVAL board J1 and J2 headers.

Note: The EZ-BLE Module includes only 19 GPIOs. In order to maintain full capability of the CY8CKIT-042-BLE Pioneer Kit functionality, four of the Port-Pin connections do not completely match the CY8CKIT-042-BLE baseboard pin out. See Table 36 for the complete list of GPIOs available on the CYBLE-212006-EVAL and the corresponding Port-Pin connection to the CY8CKIT-042-EVAL baseboard.

The CYBLE-212006-EVAL includes the following elements:

- J3 Header: A two-pin header that exposes VDD and VDDR. This header can be used to short the VDD and VDDR power connections. This jumper must be shorted when using the CYBLE-212006-EVAL with the MiniProg3 kit due to the fact that the MiniProg3 kit only supplies VDD to the evaluation board. When using the CYBLE-212006-EVAL in conjunction with the CY8CKIT-042-BLE Pioneer kit, this jumper connection does not matter, and can be connected or disconnected.
- J4 Header: A 10-pin header is included on the CYBLE-212006-EVAL kit that exposes connections used for programming and debug with the MiniProg3 kit, as shown in Figure 148. The 10-pin ribbon cable included in the MiniProg3 kit must be used for this connection.

Figure 148. CYBLE-212006-EVAL Using CY8CKIT-002 MiniProg3 and 10-Pin Ribbon Cable

As mentioned previously, the port-pin connections of the CYBLE-212006-EVAL do not completely match the CY8CKIT-042-BLE baseboard pin out. Four such connections exist on the CYBLE-212006-EVAL that do not align with the CY8CKIT-042-BLE baseboard (highlighted in red in Table 36). Fortunately, Cypress BLE silicon is configurable so that pin functions can be easily re-assigned. Note: P3[5] of the CYBLE-212006-01 module is routed to both the P3[5] and P2[7] CY8CKIT-042-BLE baseboard connections.

Table 36 details all connections on the CY8CKIT-042-BLE baseboard and provides the equivalent Port-Pin connection on the CYBLE-212006-EVAL board. The port-pin list order is according on the CY8CKIT-042-BLE baseboard physical connection pinout.

Table 36. CYBLE-212006-EVAL Port-Pin Connections to CY8CKIT-042-BLE Baseboard

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-212006-EVAL Connection Port-Pin
J11	P0[0]	NC
J11	P0[1]	NC
J11	P0[2]	NC
J11	P0[3]	NC
J11	P0[4]	NC
J11	P0[5]	NC
J11	VREF	VREF
J11	P1[0]	P1[0]
J11	P1[1]	NC
J11	P1[2]	NC
J11	P1[4]	P1[4]
J11	P0[6]	P0[6]
J11	P1[3]	NC
J11	P0[7]	P0[7]
J11	P1[5]	P1[5]
J11	XRES	XRES
J11	P1[7]	P1[7]
J11	GND	GND
J11	P1[6]	P1[6]
J11	VDD	VDD
J10	GND	GND
J10	VDD	VDD
J10	P3[6]	P3[6]
J10	P3[7]	P3[7]
J10	P3[4]	P3[4]
J10	P3[5][68]	P3[5][78]
J10	P3[2]	NC
J10	P3[3]	NC
J10	P3[0]	NC
J10	P3[1]	NC
J10	P4[0][69]	NC

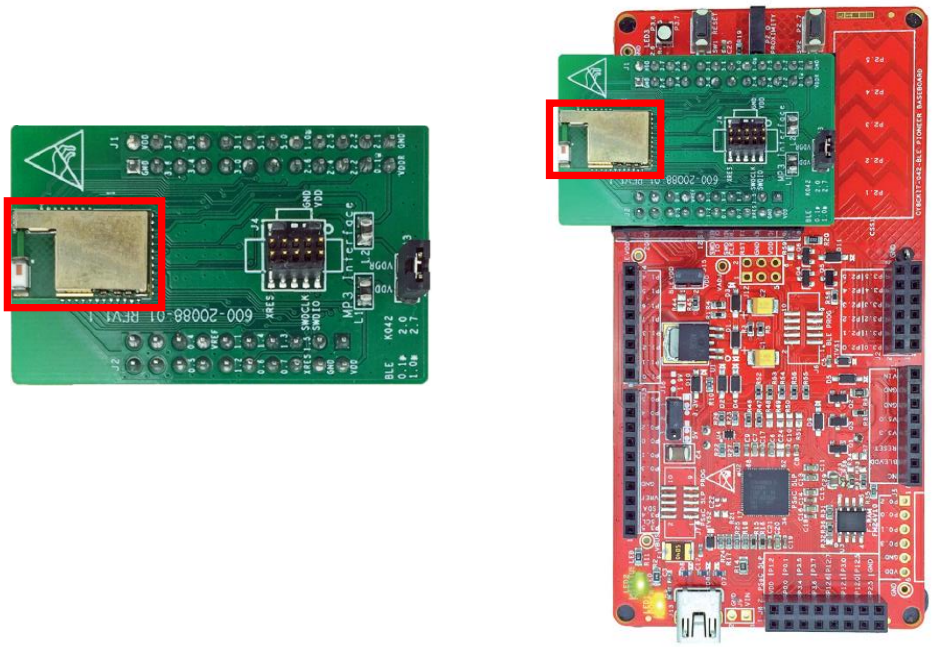
[68] P3[5] is routed to both P3[5] of the Pioneer kit as well as P2[7] of the pioneer kit. This is done in order to maintain the switch connection on the baseboard but still allow for DTM mode operation on P3[5].

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-212006-EVAL Connection Port-Pin
J10	P5[1]	NC
J10	P4[1]	NC
J10	P5[0]	NC
J10	P2[6]	P2[6]
J10	P2[7][70]	P1[0][80]
J10	P2[4]	P2[4]
J10	P2[5]	P0[4]
J10	P2[2]	P2[2]
J10	P2[3]	P2[3]
J10	P2[0]	P2[0]
J10	P2[1]	P0[5]
J10	VDDR	VDDR
J10	GND	GND

C.1.11 CYBLE-224110-EVAL

Figure 149 shows the CYBLE-224110-EVAL connected to the CY8CKIT-042-BLE Kit. The EZ-BLE PSoC Module (CYBLE-224110-00) is shown in the red box in Figure 149.

Figure 149. CYBLE-224110-EVAL (Left) Connected to CY8CKIT-042-BLE (Right)



[69] P4[0] and P4[1] are connected to a.2nF and 10nF capacitor on the CYBLE-212006-EVAL board, so they are not available on the module or the CYBLE-212006-EVAL board for connection.

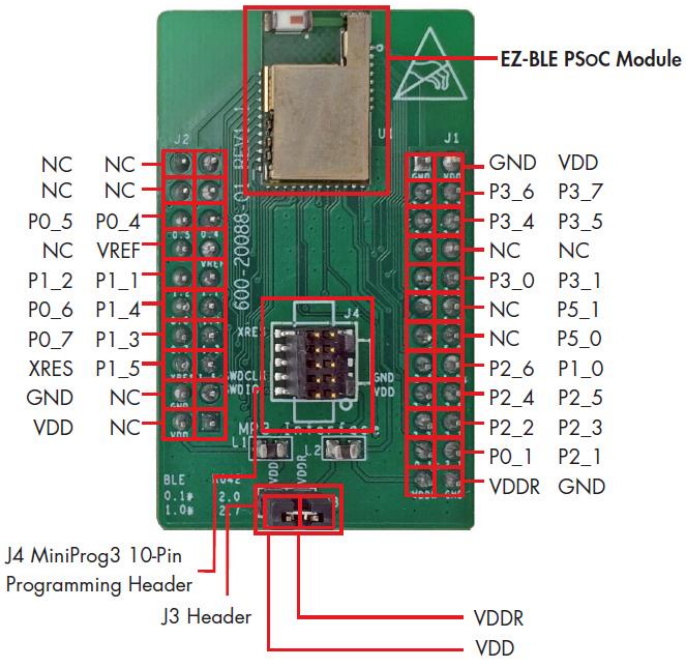
[70] P1[0] is routed to the P2[7] connection on the CY8CKIT-042-BLE baseboard in order to allow for connection to the Capacitive Sensing slider element on the baseboard (if desired).

C.1.11.1 CYBLE-224110-EVAL Connections to CY8CKIT-042-BLE

The CYBLE-224110-00 module contains 32 connections on the bottom side of the module. All of these connections are present on the CYBLE-224110-EVAL evaluation board.

Figure 150 shows the CYBLE-224110-EVAL and highlights the elements on the top side of the board. The port-pin connections shown below denote the EZ-BLE module connections on the evaluation board, not the CY8CKIT-042-BLE baseboard connections.

Figure 150. CYBLE-224110-EVAL Board Top Side



Note: Connections not called out on J1 and J2 connection headers are NC (No Connect), where no physical connection is present between the CYBLE-224110-00 EZ-BLE PSoC Module and the CYBLE-224110-EVAL board J1 and J2 headers.

Note: The EZ-BLE PSoC XT/XR Module includes only 25 GPIOs. In order to maintain full capability of the CY8CKIT-042-BLE Pioneer Kit functionality, three of the Port-Pin connections do not completely match the CY8CKIT-042-BLE baseboard pin out. See Table 37 for the complete list of GPIOs available on the CYBLE-224110-EVAL and the corresponding Port-Pin connection to the CY8CKIT-042-EVAL baseboard.

The CYBLE-224110-EVAL includes the following elements:

- J3 Header: A two-pin header that exposes VDD and VDDR. This header can be used to short the VDDA and VDDR power connections to VDD. This jumper must be shorted when using the CYBLE-224110-EVAL with the MiniProg3 kit due to the fact that the MiniProg3 kit only supplies VDD to the evaluation board. When using the CYBLE-224110-EVAL in conjunction with the CY8CKIT-042-BLE Pioneer kit, these jumper connections do not matter, and they can be connected or disconnected.
- J4 Header: A 10-pin header is included on the CYBLE-224110-EVAL kit that exposes connections used for programming and debug with the MiniProg3 kit, as shown in Figure 151. The 10-pin ribbon cable included in the MiniProg3 kit must be used for this connection.

Figure 151. CYBLE-224110-EVAL Using CY8CKIT-002 MiniProg3 and 10-Pin Ribbon Cable

As mentioned previously, the port-pin connections of the CYBLE-224110-EVAL do not completely match the CY8CKIT-042-BLE baseboard pin out. Two such connections exist on the CYBLE-224110-EVAL that do not align with the CY8CKIT-042-BLE baseboard (highlighted in red in Table 37). Fortunately, PSoC BLE is configurable so that pin functions can be easily re-assigned.

Table 37 details all connections on the CY8CKIT-042-BLE baseboard and provides the equivalent Port-Pin connection on the CYBLE-224110-EVAL board. The port-pin list order is according on the CY8CKIT-042-BLE baseboard physical connection pinout.

Table 37. CYBLE-224110-EVAL Port-Pin Connections to CY8CKIT-042-BLE Baseboard

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-224110-EVAL Connection Port-Pin
J11	P0[0]	NC
J11	P0[1][71]	NC
J11	P0[2]	NC
J11	P0[3]	NC
J11	P0[4]	P0[4]
J11	P0[5]	P0[5]
J11	VREF	VREF
J11	P1[0][39]	NC[39]
J11	P1[1]	P1[1]
J11	P1[2]	P1[2]
J11	P1[4]	P1[4]
J11	P0[6]	P0[6]
J11	P1[3]	P1[3]
J11	P0[7]	P0[7]
J11	P1[5]	P1[5]
J11	XRES	XRES
J11	P1[7]	NC
J11	GND	GND

[71] P0[1] is routed to the P2[0] connection on the CY8CKIT-042-BLE baseboard in order to allow for connection to the Proximity Sensor element on the baseboard (if desired).

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-224110-EVAL Connection Port-Pin
J11	P1[6]	NC
J11	VDD	VDD
J12	GND	GND
J10	VDD	VDD
J10	P3[6]	P3[6]
J10	P3[7]	P3[7]
J10	P3[4]	P3[4]
J10	P3[5]	P3[5]
J10	P3[2]	NC
J10	P3[3]	NC
J10	P3[0]	P3[0]
J10	P3[1]	P3[1]
J10	P4[0][72]	NC[72]
J10	P5[1]	P5[1]
J10	P4[1][72]	NC[72]
J10	P5[0]	P5[0]
J10	P2[6]	P2[6]
J10	P2[7][73]	P1[0][73]
J10	P2[4]	P2[4]
J10	P2[5]	P2[5]
J10	P2[2]	P2[2]
J10	P2[3]	P2[3]
J10	P2[0][71]	P0[1][71]
J10	P2[1]	P2[1]
J10	VDDR	VDDR
J10	GND	GND

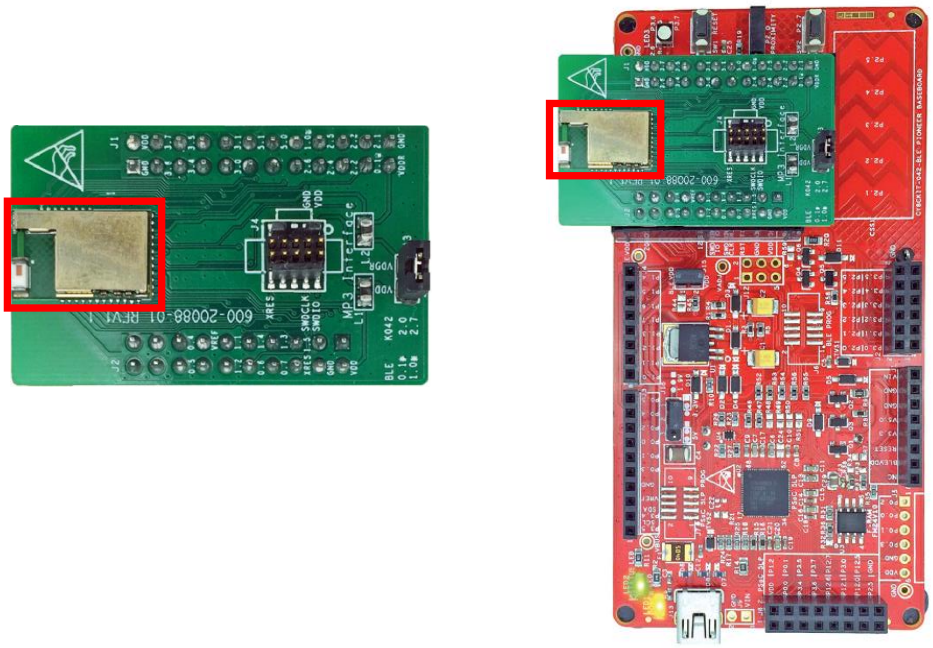
[72] P4[0] and P4[1] are connected on the CYBLE-224110-00 EZ-BLE XT/XR Module to an on-board 2.2nF and 10nF capacitor respectively, so they are not available on the module or the CYBLE-224110-EVAL board for connection

[73] P1[0] is routed to the P2[7] connection on the CY8CKIT-042-BLE baseboard in order to allow for connection to the Capacitive Sensing slider element on the baseboard (if desired).

C.1.12 CYBLE-224116-EVAL

Figure 152 shows the CYBLE-224116-EVAL connected to the CY8CKIT-042-BLE Kit. The EZ-BLE PSoC Module (CYBLE-224116-01) is shown in the red box in Figure 152.

Figure 152. CYBLE-224116-EVAL (Left) Connected to CY8CKIT-042-BLE (Right)

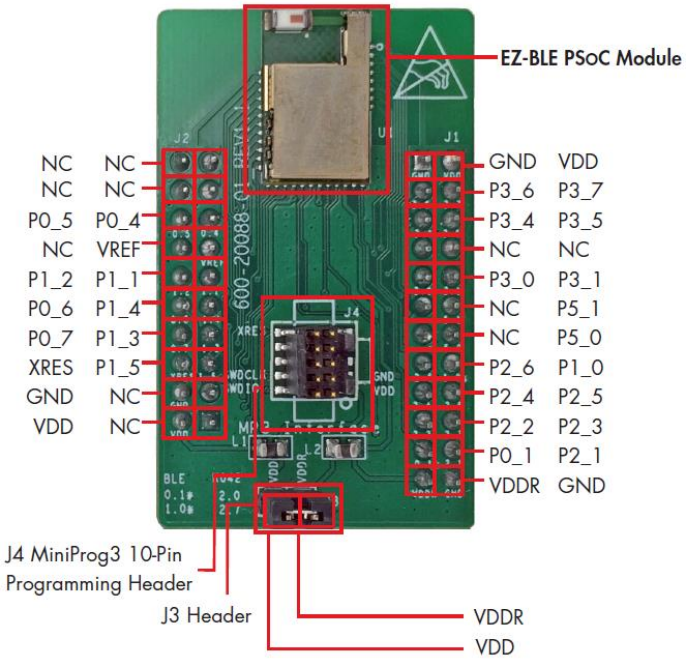


C.1.12.1 CYBLE-224116-EVAL Connections to CY8CKIT-042-BLE

The CYBLE-224116-01 module contains 32 connections on the bottom side of the module. All of these connections are present on the CYBLE-224116-EVAL evaluation board.

Figure 153 shows the CYBLE-224116-EVAL and highlights the elements on the top side of the board. The port-pin connections shown below denote the EZ-BLE module connections on the evaluation board, not the CY8CKIT-042-BLE baseboard connections.

Figure 153. CYBLE-224116-EVAL Board Top Side



Note: Connections not called out on J1 and J2 connection headers are NC (No Connect), where no physical connection is present between the CYBLE-224116-01 EZ-BLE PSoC Module and the CYBLE-224116-EVAL board J1 and J2 headers.

Note: The EZ-BLE PSoC XT/XR Module includes only 25 GPIOs. In order to maintain full capability of the CY8CKIT-042-BLE Pioneer Kit functionality, three of the Port-Pin connections do not completely match the CY8CKIT-042-BLE baseboard pin out. See Table 38 for the complete list of GPIOs available on the CYBLE-224116-EVAL and the corresponding Port-Pin connection to the CY8CKIT-042-EVAL baseboard.

The CYBLE-224116-EVAL includes the following elements:

- J3 Header: A two-pin header that exposes VDD and VDDR. This header can be used to short the VDDA and VDDR power connections to VDD. This jumper must be shorted when using the CYBLE-224116-EVAL with the MiniProg3 kit due to the fact that the MiniProg3 kit only supplies VDD to the evaluation board. When using the CYBLE-224116-EVAL in conjunction with the CY8CKIT-042-BLE Pioneer kit, these jumper connections do not matter, and they can be connected or disconnected.
- J4 Header: A 10-pin header is included on the CYBLE-224116-EVAL kit that exposes connections used for programming and debug with the MiniProg3 kit, as shown in Figure 154. The 10-pin ribbon cable included in the MiniProg3 kit must be used for this connection.

Figure 154. CYBLE-224116-EVAL Using CY8CKIT-002 MiniProg3 and 10-Pin Ribbon Cable

As mentioned previously, the port-pin connections of the CYBLE-224116-EVAL do not completely match the CY8CKIT-042-BLE baseboard pin out. Two such connections exist on the CYBLE-224116-EVAL that do not align with the CY8CKIT-042-BLE baseboard (highlighted in red in Table 38). Fortunately, PSoC BLE is configurable so that pin functions can be easily re-assigned.

Table 38 details all connections on the CY8CKIT-042-BLE baseboard and provides the equivalent Port-Pin connection on the CYBLE-224116-EVAL board. The port-pin list order is according on the CY8CKIT-042-BLE baseboard physical connection pinout.

Table 38. CYBLE-224116-EVAL Port-Pin Connections to CY8CKIT-042-BLE Baseboard

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-224116-EVAL Connection Port-Pin
J11	P0[0]	NC
J11	P0[1][74]	NC
J11	P0[2]	NC
J11	P0[3]	NC
J11	P0[4]	P0[4]
J11	P0[5]	P0[5]
J11	VREF	VREF
J11	P1[0][39]	NC[39]
J11	P1[1]	P1[1]
J11	P1[2]	P1[2]
J11	P1[4]	P1[4]
J11	P0[6]	P0[6]
J11	P1[3]	P1[3]
J11	P0[7]	P0[7]
J11	P1[5]	P1[5]
J11	XRES	XRES
J11	P1[7]	NC
J11	GND	GND

[74] P0[1] is routed to the P2[0] connection on the CY8CKIT-042-BLE baseboard in order to allow for connection to the Proximity Sensor element on the baseboard (if desired).

CY8CKIT-042-BLE Baseboard Connection Header	CY8CKIT-042-BLE Baseboard Connection Port-Pin	CYBLE-224116-EVAL Connection Port-Pin
J11	P1[6]	NC
J11	VDD	VDD
J12	GND	GND
J10	VDD	VDD
J10	P3[6]	P3[6]
J10	P3[7]	P3[7]
J10	P3[4]	P3[4]
J10	P3[5]	P3[5]
J10	P3[2]	NC
J10	P3[3]	NC
J10	P3[0]	P3[0]
J10	P3[1]	P3[1]
J10	P4[0][75]	NC[72]
J10	P5[1]	P5[1]
J10	P4[1][72]	NC[72]
J10	P5[0]	P5[0]
J10	P2[6]	P2[6]
J10	P2[7][76]	P1[0][73]
J10	P2[4]	P2[4]
J10	P2[5]	P2[5]
J10	P2[2]	P2[2]
J10	P2[3]	P2[3]
J10	P2[0][71]	P0[1][71]
J10	P2[1]	P2[1]
J10	VDDR	VDDR
J10	GND	GND

[75] P4[0] and P4[1] are connected on the CYBLE-224110-00 EZ-BLE XT/XR Module to an on-board 2.2nF and 10nF capacitor respectively, so they are not available on the module or the CYBLE-224110-EVAL board for connection

[76] P1[0] is routed to the P2[7] connection on the CY8CKIT-042-BLE baseboard in order to allow for connection to the Capacitive Sensing slider element on the baseboard (if desired).

Appendix D. Code Examples

PSoC Creator includes a large number of code example projects. These projects are available from the PSoC Creator Start Page, as Figure 155 shows.

Example projects can speed up your design process by starting you off with a complete design, instead of a blank page. The example projects also show how PSoC Creator Components can be used for various applications. Code examples and datasheets are included, as Figure 156 shows.

In the **Find Example Project** dialog shown in Figure 156, you have several options:

- Filter for examples based on architecture or device family. For EZ-BLE PRoC Module, use the PRoC BLE filter. Most of the PRoC BLE example projects can be reconfigured to work with the EZ-BLE PRoC Module by just changing the target device and the pin assignments.
- Select from the menu of examples offered based on the **Filter Options**. There are more than 20 BLE example projects for you to get started, as shown in Figure 156.
- Review the datasheet for the selection (on the **Documentation** tab)
- Review the code example for the selection. You can copy and paste code from this window to your project, which can help speed up code development.
- Or create a new project (and a new workspace if needed) based on the selection. This can speed up your design process by starting you off with a complete basic design. You can then adapt that design to your application.

Figure 155. Code Examples in PSoC Creator

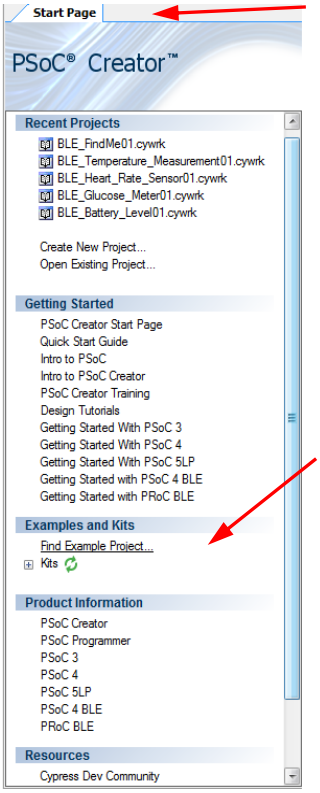
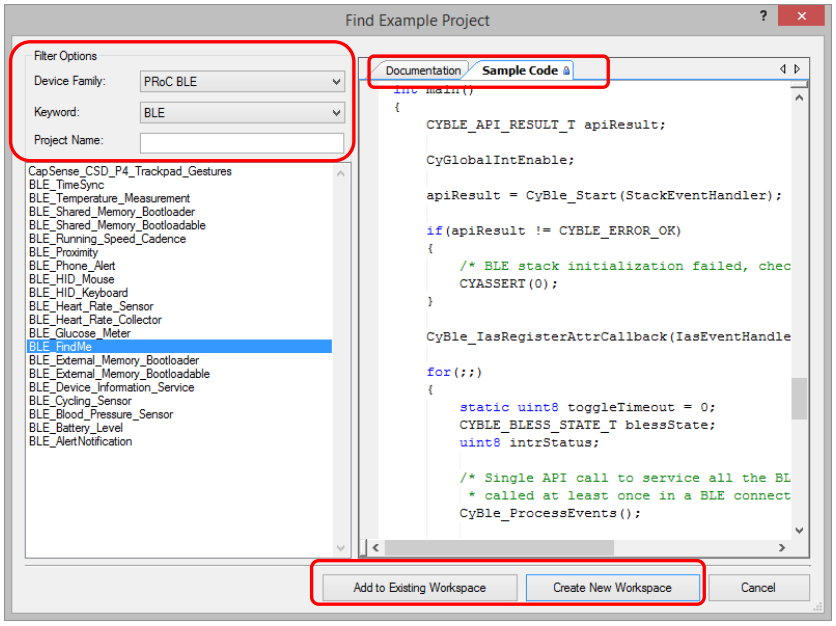


Figure 156. Code Example Projects with Sample Code



Appendix E. Example Project main.c

```
#include <Project.h>

#define LED_ON                  (0u)
#define LED_OFF                 (1u)

#define NO_ALERT                (0u)
#define MILD_ALERT              (1u)
#define HIGH_ALERT              (2u)

#define LED_TOGGLE_TIMEOUT      (100u)

#define CAPACITOR_TRIM_VALUE    0x00003FFA

uint8 alertLevel;


void IasEventHandler(uint32 event, void *eventParam)
{
    /* Alert Level Characteristic write event */
    if(event == CYBLE_EVT_IASS_WRITE_CHAR_CMD)
    {
        /* Read the updated Alert Level value from the GATT database */
        CyBle_IassGetCharacteristicValue(CYBLE_IAS_ALERT_LEVEL,
            sizeof(alertLevel), &alertLevel);
    }
}

void StackEventHandler(uint32 event, void *eventParam)
{

    CYBLE_BLESS_CLK_CFG_PARAMS_T clockConfig;

    switch(event)
    {
        /* Mandatory events to be handled by Find Me Target design */
        case CYBLE_EVT_STACK_ON:
            /* load capacitors on the ECO should be tuned and the tuned value
            * must be set in the CY_SYS_XTAL_BLERD_BB_XO_CAPTRIM_REG  */

            CY_SYS_XTAL_BLERD_BB_XO_CAPTRIM_REG = CAPACITOR_TRIM_VALUE;

            /* Get the configured clock parameters for BLE sub-system */

           CyBle_GetBleClockCfgParam(&clockConfig);

        case CYBLE_EVT_GAP_DEVICE_DISCONNECTED:
            /* Start BLE advertisement for 30 seconds and update link
             * status on LEDs */
            CyBle_GappStartAdvertisement(CYBLE_ADVERTISING_FAST);
            Advertising_LED_Write(LED_ON);
            alertLevel = NO_ALERT;
        break;
```

```
        case CYBLE_EVT_GAP_DEVICE_CONNECTED:
            /* BLE link is established */
            Advertising_LED_Write(LED_OFF);
            Disconnect_LED_Write(LED_OFF);
        break;

        case CYBLE_EVT_GAPP_ADVERTISEMENT_START_STOP:
            if(CyBle_GetState() == CYBLE_STATE_DISCONNECTED)
            {
                /* Advertisement event timed out, go to low power
                 * mode (Stop mode) and wait for device reset
                 * event to wake up the device again */
                Advertising_LED_Write(LED_OFF);
                Disconnect_LED_Write(LED_ON);
                CySysPmSetWakeupPolarity(CY_PM_STOP_WAKEUP_ACTIVE_HIGH);
                CySysPmStop();

                /* Code execution will not reach here */
            }
        break;

        default:
        break;
    }
}

int main()
{
  CYBLE_API_RESULT_T apiResult;

  CyGlobalIntEnable;

  apiResult = CyBle_Start(StackEventHandler);

  if(apiResult != CYBLE_ERROR_OK)
  {
    /* BLE stack initialization failed, check your configuration */
    CYASSERT(0);
  }

  CyBle_IasRegisterAttrCallback(IasEventHandler);

for(;;)
{
    static uint8 toggleTimeout = 0;
    CYBLE_BLESS_STATE_T blessState;
    uint8 intrStatus;

    /* Single API call to service all the BLE stack events. Must be
     * called at least once in a BLE connection interval */
        CyBle_ProcessEvents();
    /* Update Alert Level value on the blue LED */
    switch(alertLevel)
    {
```

```
        case NO_ALERT:
        Alert_LED_Write(LED_OFF);
        break;

        case MILD_ALERT:
        toggleTimeout++;
        if(toggleTimeout == LED_TOGGLE_TIMEOUT)
        {
            /* Toggle alert LED after timeout */
            Alert_LED_Write(Alert_LED_Read() ^ 0x01);
            toggleTimeout = 0;
        }
        break;

        case HIGH_ALERT:
        Alert_LED_Write(LED_ON);
        break;
    }

    /* Configure BLESS in Deep-Sleep mode */
    CyBle_EnterLPM(CYBLE_BLESS_DEEPSLEEP);

    /* Prevent interrupts while entering system low power modes */
    intrStatus = CyEnterCriticalSection();

    /* Get the current state of BLESS block */
    blessState = CyBle_GetBleSsState();

    /* If BLESS is in Deep-Sleep mode or the XTAL oscillator is turning on,
     * then PRoC BLE can enter Deep-Sleep mode (1.3uA current consumption) */
    if(blessState == CYBLE_BLESS_STATE_ECO_ON ||
        blessState == CYBLE_BLESS_STATE_DEEPSLEEP)
    {
        CySysPmDeepSleep();
    }
    else if(blessState != CYBLE_BLESS_STATE_EVENT_CLOSE)
    {
        /* If BLESS is active, then configure PRoC BLE system in
         * Sleep mode (~1.6mA current consumption) */
        CySysPmSleep();
    }
    else
    {
        /* Keep trying to enter either Sleep or Deep-Sleep mode */
    }
    CyExitCriticalSection(intrStatus);

    /* BLE link layer timing interrupt will wake up the system from Sleep
     * and Deep-Sleep modes */
}
      }
```

Appendix F. Regulatory Information

Please refer to your specific EZ-BLE module datasheet for module specific compliance declarations.

FCC:

FCC NOTICE:

Cypress EZ-BLE Modules, including integrated antennas, comply with Part 15 of the FCC Rules. When stated in the module datasheet, the modules meet the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407.transmitter Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

CAUTION

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Cypress Semiconductor may void the user's authority to operate the equipment.

Any certified modules provided by Cypress have been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

LABELING REQUIREMENTS

The Original Equipment Manufacturer (OEM) must ensure that FCC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor FCC identifier for this product as well as the FCC Notice above. The FCC identifier for each module is listed in the module datasheet, and is of the form “**FCC ID: WAPxxxx”**, where “xxxx” denotes the module-specific FCC identifier.

In any case, the end product using a certified Cypress module must be labeled on the exterior with "Contains FCC ID: WAPxxxx", where “xxxx” is the module-specific FCC identifier.

ANTENNA WARNING

Please refer to the module datasheet for details on the specific antenna used for the module design. Each Cypress certified module may have a different Antenna design. When integrated in the OEMs product, these antennas require installation preventing end-users from replacing them with non-approved antennas. Any antenna not listed in the module datasheet must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

RF EXPOSURE

To comply with FCC RF Exposure requirements, the Original Equipment Manufacturer (OEM) must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antennas listed in the module datasheet, to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of Cypress certified modules with antenna mounted is far below the FCC radio frequency exposure limits. Nevertheless, use Cypress modules in such a manner that minimizes the potential for human contact during normal operation.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

Innovation, Science and Economic Development (ISED) Canada Certification

When indicated in the module datasheet, Cypress EZ-BLE modules are licensed to meet the regulatory requirements of Innovation, Science and Economic Development (ISED) Canada. Refer to the module datasheet for details on the specific IC identifier. The IC identifier will be of the form:

License: IC: 7922A-xxxx, where “xxxx” is the ID for a specific module.

Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from www.ic.gc.ca.

Cypress EZ-BLE modules have been designed to operate with the antennas listed in the module datasheet. Antennas not included in the module datasheet or having a gain greater than what is specified in the module datasheet are strictly prohibited for use with this device. The required antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

ISED NOTICE

Cypress EZ-BLE modules, including the built-in antenna complies with Canada RSS-GEN Rules. Cypress EZ-BLE modules meet the requirements for modular transmitter approval as detailed in RSS-GEN. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

Les modules Cypress EZ-BLE, y compris l'antenne intégrée, sont conformes aux Règles RSS-GEN de Canada. Les modules Cypress EZ-BLE répondent aux exigences d'approbation de l'émetteur modulaire, tel que décrit dans RSS-GEN. L'opération est soumise aux deux conditions suivantes: (1) Cet appareil ne doit pas causer d'interférences nuisibles, et (2) Cet appareil doit accepter toute interférence reçue, y compris les interférences susceptibles de provoquer un fonctionnement indésirable.

ISED INTERFERENCE STATEMENT FOR CANADA

Cypress EZ-BLE modules comply with Innovation, Science and Economic Development (ISED) Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Les modules Cypress EZ-BLE sont conformes aux normes RSS, exemptées de licences et exemptées de licence de l'Innovation, des Sciences et du Développement (ISED). Le fonctionnement est soumis aux deux conditions suivantes: (1) cet appareil ne doit pas provoquer d'interférence, et (2) cet appareil doit accepter toute interférence, y compris les interférences susceptibles de provoquer un fonctionnement indésirable de l'appareil.

ISED RADIATION EXPOSURE STATEMENT FOR CANADA

Cypress EZ-BLE modules comply with ISED radiation exposure limits set forth for an uncontrolled environment. Please refer to the module datasheet for any details on integration requirements for radiation exposure.

Les modules Cypress EZ-BLE sont conformes aux limites d'exposition au rayonnement ISED prévues pour un environnement incontrôlé. Veuillez vous référer à la fiche technique du module pour tout détail sur les exigences d'intégration pour l'exposition au rayonnement.

LABELING REQUIREMENTS

The Original Equipment Manufacturer (OEM) must ensure that IC labelling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Cypress Semiconductor IC identifier for this product as well as the IC Notice above. The IC identifier is **7922A-xxxx**, where “xxxx” is the specific IC ID for a given module. In any case, the end product must be labeled in its exterior with "Contains **IC: 7922A-xxxx**", where “xxxx” is the module specific ID as indicated in the module datasheet.

Le fabricant d'équipement d'origine (OEM) doit s'assurer que les exigences d'étiquetage IC sont respectées. Cela comprend une étiquette clairement visible à l'extérieur de l'enceinte OEM spécifiant l'identifiant Cypress Semiconductor approprié pour ce produit ainsi que l'avis IC ci-dessus. L'identifiant IC est 7922A-xxxx, où "xxxx" est l'ID CI spécifique pour un module donné. En tout cas, le produit final doit être étiqueté dans son extérieur avec "Contient IC: 7922A-xxxx", où "xxxx" est l'ID spécifique du module comme indiqué dans la fiche technique du module.

EUROPEAN DECLARATION OF CONFORMITY

Hereby, Cypress Semiconductor declares that the EZ-BLE Bluetooth modules, when indicated on the module datasheet, comply with the essential requirements and other relevant provisions of Directive 2014. As a result of the conformity assessment procedure described in Annex III of the Directive 2014, the end-customer equipment should be labeled as follows:

CE

When indicated in the module datasheet, the module used in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

MIC JAPAN

When indicated, Cypress EZ-BLE modules are certified as a module with a specific type certification number detailed in the module datasheet. End products that integrate modules that are certified for Japan do not need additional MIC Japan certification for the end product.

End product can display the certification label of the embedded module as display in the specific module datasheet.

KC Korea

When indicated in the module datasheet, Cypress EZ-BLE modules are certified for use in Korea with specific certificate numbers specified in the module datasheet.

F.1 Module Regulatory Reports and Certificates

Table 39 details the knowledge base articles that contain the test reports and certificates for each EZ-BLE module. These knowledge base article can be found by visiting www.cypress.com and searching for the KBA number below, or by clicking on the hyperlinks in the below table.

Table 39. Regulatory Test Report and Certificate KBA Reference

EZ-BLE Module Part Number	Knowledge Base Article Containing Regulatory Reports and Certificates
CYBLE-022001-00	KBA97094
CYBLE-222005-00	KBA210559
CYBLE-222014-01	
CYBLE-012011-00	KBA210638
CYBLE-212019-00	
CYBLE-212020-01	
CYBLE-012012-10	N/A – Not certified
CYBLE-212023-10	N/A – Not certified
CYBLE-014008-00	KBA210574
CYBLE-214009-00	
CYBLE-214015-01	
CYBLE-212006-01	KBA216380
CYBLE-202007-01	
CYBLE-202013-11	N/A – Not certified
CYBLE-224110-00	KBA213260
CYBLE-224116-01	

Document History

Document Title: AN96841 – Getting Started with EZ-BLE™ Creator Modules

Document Number: 001-96841

Rev.	ECN	Orig. of Change	Submission Date	Description of Change
**	4715534	DSO	04/08/2015	New application note
*A	4763637	DSO	05/12/2015	Added associated project to this application note Separated Development Tools and Development Kits in More Information on Page 2 as well as in content of document Updated Table 3 to remove functions that are not functional with the module (i.e. EXTPA_EN, EXT_CLK) Added footnote definitions for TCPWM, ECO_OUT, and GPIO in Table 3 Added footnote definitions for IMO, WDT, ILO, and SCB on Page 7 Specified “Typical” for Power Consumption shown in Figure 4 Added Figure 6 to Page 8 Updated BLE Overview content throughout Pages 9~18 Updated Figure 26 to remove P1[3] as a connected GPIO on the CYBLE-022001-EVAL board Updated Table 3 to highlight the seven connections in red text on the CYBLE-022001-00 that do not match those of the CY8CKIT-042-BLE Baseboard Updated flow and text in “My First EZ-BLE PRoC Module Design” section. All sections updated (Part 1, Part 2, Part 3, and Part 4) Updated all links throughout to final web links Added Appendix D for additional information on BLE Protocol Added Appendix E with entire main.c code example Added Appendix F detailing Regulatory Information
*B	4803518	DSO	06/19/2015	Updated the following figures with the latest screen captures: Figure 6, Figure 7, Figure 37, Figure 38, Figure 39, Figure 40, Figure 41, Figure 42, Figure 43, Figure 44, Figure 45, Figure 46, Figure 59 Updated PSoC Creator section Updated Figure 12, and Figure 13 with final Evaluation Board Images Added Figure 27, Figure 28, and Figure 29 for instructions on how to update components with the Component Update Tool Updated Regulatory Information to add MIC (Japan) and KC (Korea) certification information
*C	4860212	DSO	07/27/2015	Added support link to page footers
*D	4925758	DSO	09/25/2015	Change Title of Application Note from “Getting Started With EZ-BLE™ PRoC™ Module” to “Getting Started With EZ-BLE™ Module” Update Associated Part Family to “CYBLE-XXXXXX-XX” to represent all EZ-BLE Modules Update supported PSoC Creator Version to V3.2 and higher General update throughout Application Note body making it general to the EZ-BLE family and not specific to the EZ-BLE PRoC Module Updated Figure 32 with the latest screen capture Added Appendix B: EZ-BLE Module Product Details, detailing specific information on each EZ-BLE Module part number Added Appendix C: EZ-BLE Evaluation Board Details, detailing specific information on each EZ-BLE Evaluation board Update EZ-BLE Module Overview to split into four sub-sections: 3.1. EZ-BLE Module Family Features; 3.2. EZ-BLE Module Low Power Modes; 3.3. Device Security; and 3.4. EZ-BLE Module Marketing Part Number Overview Removed Bluetooth Low Energy (BLE) Overview (previous section 3) and added reference to this content in AN91267 - Getting Started with PSoC® 4 BLE in the More Information section

Rev.	ECN	Orig. of Change	Submission Date	Description of Change
				Updated EZ-BLE Evaluation Boards section to provide general information on EZ-BLE Evaluation boards and refer to Appendix C: EZ-BLE Evaluation Board Details for additional information for specific evaluation board part numbers Added Section 7, Module Placement and Orientation Considerations in a Host System to this Application Note Added Section 8, Manufacturing with EZ-BLE Modules to this Application Note
*E	5037763	DSO	12/14/2015	Updated Creator Software references from version 3.2 to version 3.3 SP1 or newer. Added reference to PRoC BLE and PSoC 4 BLE 256KB Flash silicon devices. Updated Table 2 to add new module part numbers: CYBLE-012011-00, CYBLE-012012-10, CYBLE-214009-00, and CYBLE-212019-00. Updated Table 3 to add new module evaluation board part numbers: CYBLE-012011-EVAL, CYBLE-214009-EVAL, and CYBLE-212019-EVAL. Updated PSoC Creator Figures throughout based on latest version 3.3 SP1 release. Updated Component Update Process in Figure 24, Figure 25, Figure 26, Figure 27, Figure 28, and Figure 29 based on Creator 3.3 SP1 process. Updated EZ-BLE Module Product Details to include new module marketing part numbers added. Organize modules in EZ-BLE Module Product Details based on PRoC BLE processor and PSoC BLE processor. . Updated mechanical drawings and tables throughout Appendix B to latest format. Updated EZ-BLE Evaluation Board Details to include new module evaluation board marketing part numbers added. Organize modules in EZ-BLE Evaluation Board Details based on PRoC BLE processor and PSoC BLE processor. Updated Component Library in associated example project for compatibility to PSoC Creator 3.3 SP1.
*F	5281609	DSO	06/02/2016	Updated EZ-BLE Module Overview Updated template Updated Table 2 to include new module part numbers CYBLE-222014-01, CYBLE-212023-10, and CYBLE-224110-00 Updated Table 3 to include new module evaluation board CYBLE-222014-EVAL and CYBLE-224110-EVAL Updated Figure 12 and Figure 13 Updated Figure 66, Figure 72, Figure 78, Figure 84, Figure 90, Figure 96, and Figure 102 Updated Section B.1.4 CYBLE-2120XX- to include CYBLE-212023-10 module part number. Added Section B.1.5 CYBLE-222014-01 Added Section B.2.3 CYBLE-224110-00 XT/XR (Extended Temperature/Extended Range), including code example detailing the Process for Enabling and Activating Power Amplifier/Low-Noise Amplifier
*G	5768555	AESATP12	06/13/2017	Updated logo and copyright.
*H	5801110	DSO	07/23/2017	Update Creator version to 4.1 Add new Modules to the document (224116, 212006, 202007, 202013, 214015). Reorder the Module Appendix B to combine certain modules that only have a functional difference but have the exact same pinout. Add the evaluation boards for the new added modules. General clean up of typos/grammar as needed.
*I	6151936	DSO	04/24/2018	Updated to new template. Completing Sunset Review.

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