AN96592

Migrating from Everspin's 4-Mbit SPI MRAM (MR2xH40) to Cypress's 4-Mbit SPI F-RAM (CY15B104Q)

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Associated Part Family: CY15B104Q
Software Version: None
Related Application Notes: AN304, AN87352

AN96592 provides an overview of advantages and potential differences to be considered when migrating from Everspin's 4-Mbit SPI MRAM (MR2xH40) to Cypress's high-reliability and energy-efficient 4-Mbit SPI F-RAM (CY15B104Q).

1 Introduction

Cypress's SPI F-RAM is a serial, nonvolatile memory employing an advanced ferroelectric process that offers the world's most energy-efficient, high-performance, and high-reliability nonvolatile RAM solution. F-RAM eliminates the complexities, overheads, and system-level reliability problems caused by other serial nonvolatile memories such as serial EEPROM, flash, and MRAM. F-RAM performs write operations at bus speed without incurring any write delays (NoDelay™), unlike serial EEPROM and flash memories. Data is directly written into the F-RAM array and the next bus cycle can start immediately without the need for data polling to verify the device readiness before the next write access.

Cypress's F-RAM products offer virtually unlimited endurance of 10^{14} cycles, orders of magnitude higher than typical serial nonvolatile memories such as EEPROM and flash. Also, F-RAM exhibits a lower power consumption than serial EEPROM, flash, and MRAM memories. In addition, the data stored in the F-RAM array does not get corrupted in magnetic field environments, thereby making F-RAM the best choice of the nonvolatile memory for critical data logging for the majority of the industrial applications operating in magnetic field environments. The closest alternative solution, the SPI MRAM, uses magnetic storage elements (ferromagnetic plates) to store information, which makes it highly susceptible to any magnetic field causing data corruption.

This application note highlights differences between the 4-Mbit SPI MRAM (MR2xH40) and the 4-Mbit SPI F-RAM (CY15B104Q). These differences need to be considered when migrating from MR2xH40 to CY15B104Q.

For more details on SPI F-RAM designs, refer to the application note AN304 - SPI Guide for F-RAM™.

For more details on benefits of F-RAM over a serial nonvolatile memory (EEPROM), refer to the application note AN87352 – F-RAM™ for Smart E-Meters.

2 Migrating from 4-Mbit SPI MRAM to 4-Mbit SPI F-RAM

The following sections highlight all key differences between the 4-Mbit SPI MRAM and the 4-Mbit SPI F-RAM and discuss their compatibilities when migrating from the SPI MRAM to the SPI F-RAM.

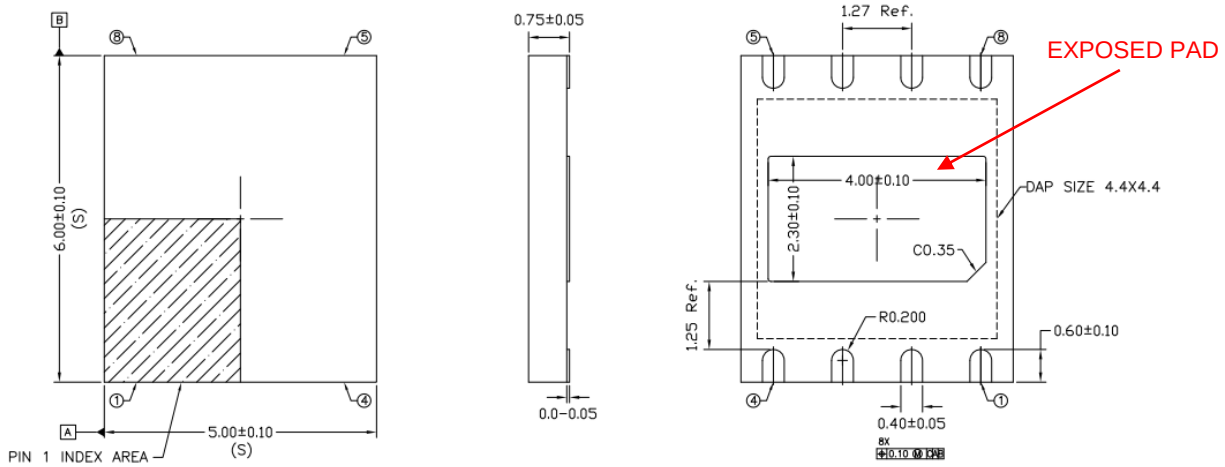
2.1 Pin and Package Compatibility

Cypress's 4-Mbit SPI F-RAM is available in two industry-standard packages: 8-pin SOIC and 8-pin DFN. These standard, versatile package options make Cypress's SPI F-RAM a drop-in replacement for all existing MRAM sockets without compromising the system's performance. In addition, Cypress's F-RAM solution provides additional advantages in the form of energy-efficiency and magnetic tolerance to make systems more reliable. Table 1 discusses key differences and their compatibilities.

Table 1. Pin and Package Comparison

Feature/Function	SPI MRAM (MR2xH40)	SPI F-RAM (CY15B104Q)	Comments
8-pin DFN EXPOSED PAD	Do not connect anything except V_{SS}	No connect	The EXPOSED PAD of the F-RAM 8-pin DFN package is an NC (No Connect) pad; therefore, it can be either floating or connected to V_{SS}/ V_{DD}. Cypress does not recommend soldering the F-RAM DFN EXPOSED PAD on the PCB.
8-pin packages	8-pin DFN, 8-pin DFN (Small Flag)	8-pin DFN, 8-pin SOIC	Both the 8-pin DFN packages of MRAM as shown in Figure 2 and Figure 3 are compatible with the 8-pin DFN package of F-RAM as shown in Figure 1. The SPI F-RAM also supports 8-pin SOIC package.

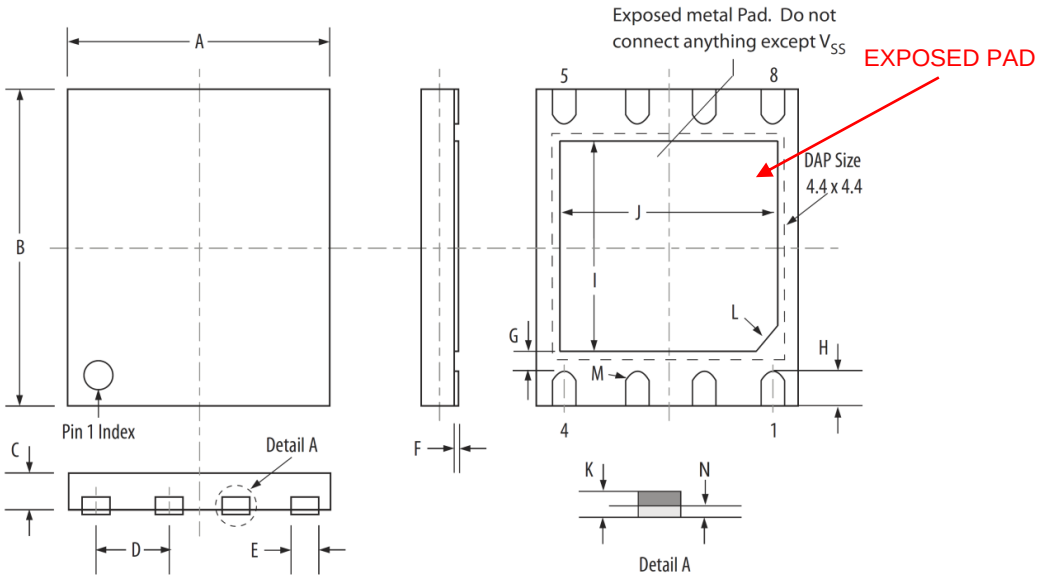
Figure 1. 4-Mbit SPI F-RAM 8-pin DFN (5 mm × 6 mm × 0.75 mm) Package Outline



The SPI F-RAM EXPOSED PAD is not connected to the die hence should be left floating. Ensure that the EXPOSED PAD of the SPI F-RAM DFN package is not soldered on the PCB when migrating to SPI F-RAM from SPI MRAM. Doing so will cause the SPI F-RAM die to be exposed to excessive heat, which can result in bit failures and margin loss.

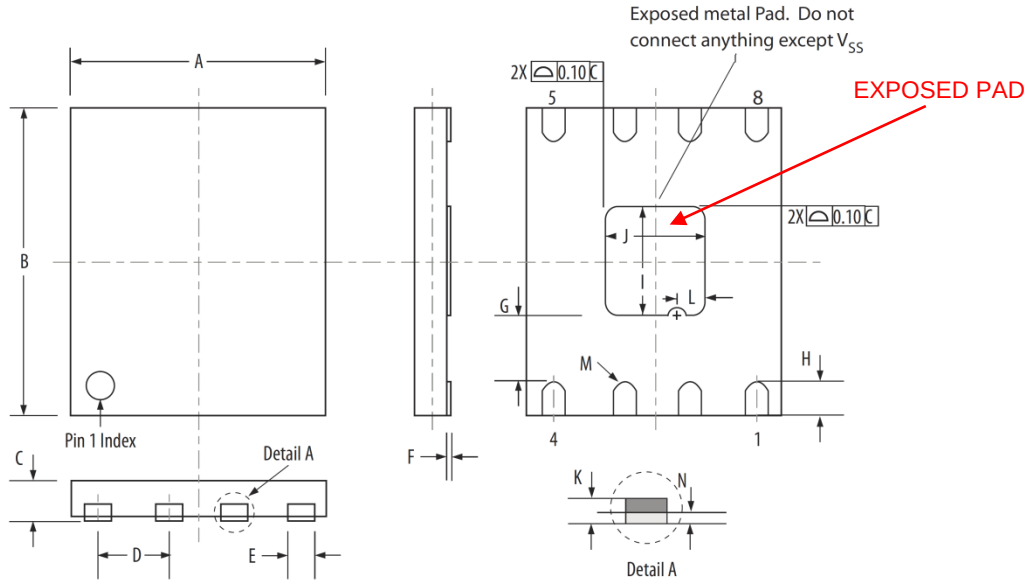
Figure 2 and Figure 3 show the Everspin 4-Mbit SPI MRAM package outlines for 8-pin DFN and 8-pin DFN (Small Flag) packages. The 4-Mbit SPI F-RAM 8-pin DFN package can be soldered directly on the footprints of these two packages.

Figure 2. 4-Mbit SPI MRAM 8-pin DFN Package Outline



Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M	N
Max.	5.10	6.10	1.00	1.27 BSC	0.45	0.05	0.35 Ref.	0.70	4.20	4.20	0.261	C0.35	R0.20	0.05
Min.	4.90	5.90	0.90		0.35	0.00		0.50	4.00	4.00	0.195			0.00

Figure 3. 4-Mbit SPI MRAM 8-pin DFN (Small Flag) Package Outline



Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M	N
Max.	5.10	6.10	0.90	1.27 BSC	0.45	0.05	1.60	0.70	2.10	2.10	.210	C0.45	R0.20	0.05
Min.	4.90	5.90	0.80		0.35	0.00	1.20	0.50	1.90	1.90	.196			0.00

Note: *The 4-Mbit SPI F-RAM DFN package height is 0.2 mm lower than the 4-Mbit SPI MRAM package DFN package height. This is an advantage with the SPI F-RAM in systems with the component height restrictions.*

2.2 Command (OPCODE) Compatibility

Table 2 shows the 4-Mbit SPI MRAM and SPI F-RAM access commands (OPCODEs) and their compatibilities.

Table 2. OPCODE Comparison

Command OPCODE (Hex)	Command Description	SPI MRAM (MR2xH40)	SPI F-RAM (CY15B104Q)	Comments
WREN (06h)	Set write enable latch	√	√	Identical functionality.
WRDI (04h)	Reset write enable latch	√	√	
RDSR (05h)	Read Status Register	√	√	
WRSR (01h)	Write Status Register	√	√	
READ (03h)	Read memory data	√	√	
FSTRD (0Bh)	Fast read memory data	X	√	The 4-Mbit SPI MRAM doesn't support this command.
WRITE (02h)	Write memory data	√	√	Identical functionality.
SLEEP (B9h)	Enter sleep mode	√	√	The 4-Mbit SPI MRAM takes t_{DP} (3 µs) to enter sleep.
WAKE (ABh)	Exit sleep mode	√	X	The 4-Mbit SPI F-RAM does not support this command. Migrating from MRAM to F-RAM does not require any software update because the SPI F-RAM wakes up when $\overline{CS}$ toggles HIGH to LOW and ignores the subsequent WAKE instruction sent on its input.
RDID (9Fh)	Read device ID	X	√	The 4-Mbit SPI MRAM does not support this feature.

2.3 Status Register Compatibility

The Status Register access in the case of the 4-Mbit SPI MRAM and the SPI F-RAM are identical. However, the value returned by the Status Register read can differ between the two parts for some bit locations. For example, the "Don't Care" bits in the SPI MRAM Status Register are writeable and they can return either '0' or '1', while the "Don't Care" bits in the SPI F-RAM Status Register are read-only bits and always return '0'. Table 3 shows the Status Register bits definition for the two parts and their compatibilities.

Table 3. Status Register Comparison

Status Register	SPI MRAM (MR2xH40)	SPI F-RAM (CY15B104Q)	Comments
Bit0	Don't Care	Don't Care (0)	This bit is non-writeable in the SPI F-RAM and always returns '0' upon read. This bit can be modified in the SPI MRAM.
Bit1	WEL	WEL	Identical behavior.
Bit2	BP0	BP0	Identical behavior.
Bit3	BP1	BP1	Identical behavior.
Bit4	Don't Care	Don't Care (0)	These bits are read-only in the SPI F-RAM and always return '0' upon read. These bits can be modified in the SPI MRAM.
Bit5	Don't Care	Don't Care (0)	
Bit6	Don't Care	Don't Care (1)	This bit is the read-only bit in the SPI F-RAM and always returns '1' upon read. This bit can be modified in the SPI MRAM.
Bit7	SRWD	WPEN	Identical behavior.

2.4 Device Spec Compatibility

This section lists all spec differences between the two parts in Table 4. Most of these differences can be considered to improve the signal-integrity, energy efficiency, and reliability by adjusting the system parameters when migrating from the 4-Mbit SPI MRAM to the 4-Mbit SPI F-RAM. However, there are a few parameters that warrant some system-level analysis before replacing the SPI MRAM with the SPI F-RAM. These include output load, start-up time, and the power ramp (power-up and power-down).

Table 4. Device Spec Comparison

Parameter	Description	SPI MRAM (MR2xH40)	SPI F-RAM (CY15B104Q)	Comments
DC Parameters				
V_{DD}	Power supply voltage	3.0 V to 3.6 V	2.0 V to 3.6 V	The SPI F-RAM operating range is wider.
V_{IH}	Input high voltage	2.2 V to V_{DD} + 0.3 V	0.7 x V_{DD} to V_{DD} + 0.3 V	V_{IH} (min) for the SPI F-RAM is 2.1 V at 3.0-V V_{DD}, which is an advantage.
V_{IL}	Input low voltage	-0.5 V to 0.8 V	-0.3 V to 0.3 x V_{DD}	V_{IL} (max) for the SPI F-RAM is 0.9 V at 3.0-V V_{DD}, which is an advantage. V_{IL} (min) = - 0.3 V is tighter for the SPI F-RAM. Systems must ensure that signal swings on the F-RAM input pins do not go below - 0.3 V.
V_{OH}	Output high voltage	2.4 V (min), I_{OH} = -4 mA; V_{DD}-0.2 V (min), I_{OH} = -100 µA	2.4 V (min), I_{OH} = -1 mA; V_{DD} - 0.2 V (min), I_{OH} = -100 µA	No change is required when migrating from the 4-Mbit SPI MRAM to the 4-Mbit SPI F-RAM in a typical system configuration. However, a heavily loaded system bus must ensure that V_{OH} remains within the logic levels for inputs.
V_{OL}	Output low voltage	0.4 V (max), I_{OL} = +4 mA; 0.2 V (max), I_{OL} = +100 µA	0.4 V (max), I_{OL} = +2 mA; 0.2 V (max), I_{OL} = +150 µA	No change is required when migrating from the 4-Mbit SPI MRAM to the 4-Mbit SPI F-RAM in a typical system configuration. However, a heavily loaded system bus must ensure that V_{OL} remains within the logic levels for inputs.
I_{DDR}	Active read current	17 mA, 40 MHz	3 mA, 40 MHz	The SPI F-RAM consumes 82% less current during read operation.
I_{DDW}	Active write current	42 mA, 40 MHz	3 mA, 40 MHz	The SPI F-RAM consumes 93% less current during write operation.
I_{SB}	Standby current	180 µA	250 µA	The SPI F-RAM consumes 39% more current when in standby mode.
I_{ZZ}	Sleep mode current	40 µA	8 µA	The SPI F-RAM consumes 80% less current when in sleep mode.
H_{max_write}	Maximum magnetic field during write	12000 A/m	Not applicable	The SPI F-RAM is not susceptible to magnetic field; therefore, F-RAM data does not get corrupted in a magnetic field of any intensity.
H_{max_read}	Maximum magnetic field during read or standby	12000 A/m	Not applicable	

Parameter	Description	SPI MRAM (MR2xH40)	SPI F-RAM (CY15B104Q)	Comments
I_{OUT}	DC output current per pin	±20 mA	±15 mA	This is the absolute maximum rating for the device. This parameter does not influence any device operation across its operating range.
Timing Parameters				
t_{DP}	Sleep mode entry time	3 µs	Not applicable	The SPI F-RAM enters sleep as soon as $\overline{CS}$ toggles LOW to HIGH after the SLEEP command is entered.
t_{PU}	Start-up (V_{DD} min to first access)	400 µs	1000 µs	Typically, the host controllers take longer than 1000 µs to boot up. Systems must review the impact of longer t_{PU} time in the SPI F-RAM and adjust their timing accordingly.
t_{REC} (t_{RDP})	Recovery time from sleep	t_{RDP} = 400 µs	t_{REC} = 450 µs	Systems must review the impact of longer wake-up time of the SPI F-RAM and adjust their timing accordingly.
t_{OD}	Output disable time	t_{DIS} = 12 ns (min)	t_{OD} = 12 ns (max)	The SPI F-RAM defines this as max spec while the SPI MRAM defines this as min spec. The max spec ensures that the device will release the output within 12 ns. The min spec ensures that the device will release the output only after 12 ns. Providing the max spec is better for a system to determine when the bus will be available for access.
Power Parameters				
V_{WI}	Write inhibit voltage	2.2 V	Not applicable	As soon as V_{DD} falls below V_{DD} min limit, the SPI F-RAM access is inhibited.
t_{VR}	V_{DD} power-up ramp rate	Not specified	50 µs/V	Systems must ensure that V_{DD} power-up ramp rate is within the datasheet spec.
t_{VF}	V_{DD} power-down ramp rate	Not specified	100 µs/V	Systems must ensure that V_{DD} power-down ramp rate is within the datasheet spec.
t_{PD}	Last access ($\overline{CS}$ HIGH) to power down V_{DD} (min)	Not specified	0 µs	Not specified for the SPI MRAM. The SPI F-RAM power can turn off immediately after the last bit access.

Note 2: *All other AC/DC parameters not listed in this table are equivalent.*

Figure 4. 4-Mbit SPI F-RAM Power Cycle Timing

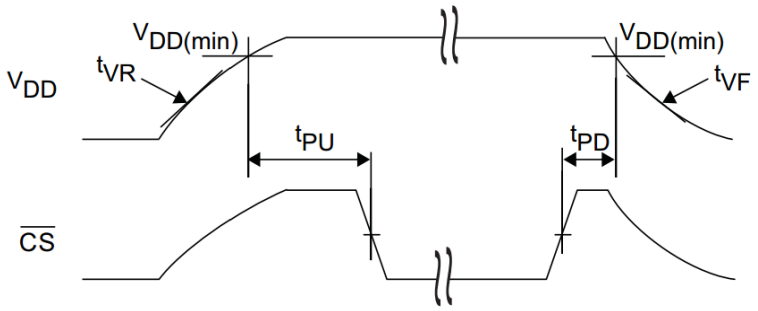
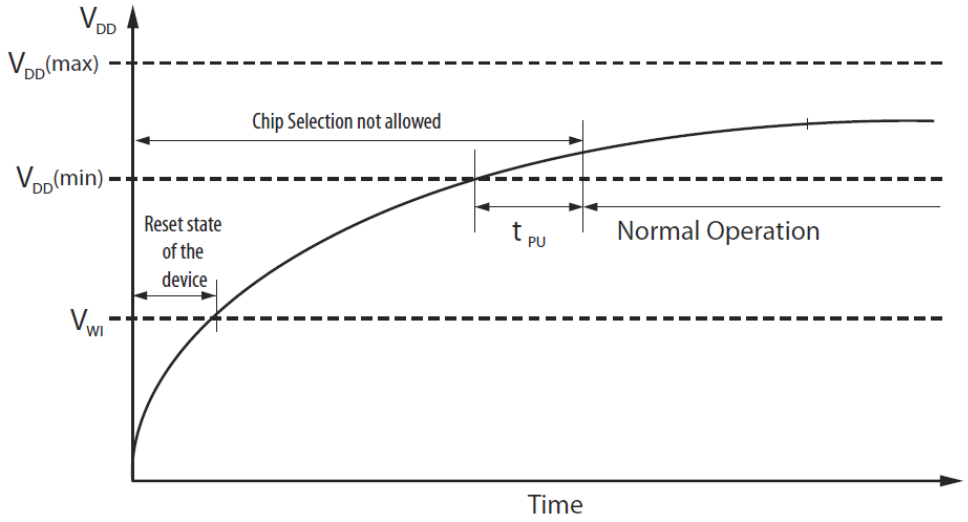


Figure 5. 4-Mbit SPI MRAM Power Cycle Timing



3 Summary

Migrating from Everspin's 4-Mbit SPI MRAM (MR2xH40) to Cypress's 4-Mbit SPI F-RAM (CY15B104Q) will improve the reliability and energy efficiency of the system. Cypress's 4-Mbit SPI F-RAM standard pin and package configuration, SPI instruction set (OPCODE), and electrical compatibility simplifies the migration. Differences between two devices are highlighted through this application note. These differences need to be considered but will typically not be gating for migration in most applications.

4 Related Documents

4.1 Application Notes

- AN304 - SPI Guide for F-RAM™
- AN87352 - F-RAM™ for Smart E-Meters

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*A	4852641	ZSK	07/22/2015	Updated Migrating from 4-Mbit SPI MRAM to 4-Mbit SPI F-RAM: Updated Device Spec Compatibility: Updated Table 4 (Fixed typo in description of V_{OH} parameter).
*B	5848881	HARA	08/18/2017	Updated logo and copyright.

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