AN95089

PSoC/PRoC BLE Crystal Oscillator Selection and Tuning Techniques

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Associated Part Family: CY8C6XXX-BL, CY8C4XXX-BL, CYBL1XX7X

AN95089 provides insights into the selection and tuning of the external crystal oscillator (ECO) and watch crystal oscillator (WCO) for PSoC®/PRoC™ BLE devices to achieve a good RF performance. This application note introduces basics of crystals and clock accuracy measurements. Cypress-recommended crystals and tuning techniques for optimum performance is also discussed.

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1 Introduction

This application note helps you select the ECO crystal and the WCO crystal for PSoC/PRoC BLE devices and tune them for optimum performance.

Bluetooth Low Energy (BLE) is a timing-sensitive technology in which an inaccurate ECO clock can degrade the physical layer RF performance; similarly, an inaccurate WCO clock can lead to increased power consumption in a peripheral.

The on-chip ECO circuit with an external crystal is used to synthesize a reference clock to run the BLE subsystem. For PSoC 4/PRoC BLE devices, the frequency of this external crystal must be 24 MHz. PSoC 6 MCU with Bluetooth Low Energy (BLE) Connectivity devices (referred to as *PSoC 6 BLE* in this document) offer an option to choose between 16-MHz and 32-MHz external crystals. The ECO clock sets the protocol timing for link-layer operations and derives the carrier frequency for physical-layer RF circuits. This application note discusses ECO, which is part of the BLE sub-system (BLESS). PSoC 6 BLE devices also support an additional ECO through the system resources sub-system (SRSS). See AN218241 - PSoC 6 MCU Hardware Design Considerations for information on using the SRSS ECO.

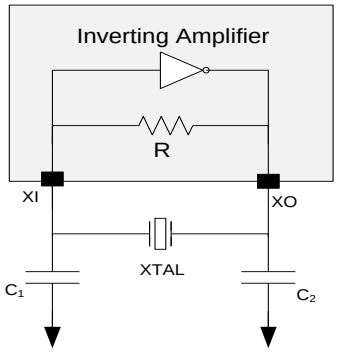
An external WCO crystal is used to derive the 32.768-kHz clock that maintains link-layer timing synchronization when the BLE subsystem is in a low-power mode.

2 Crystal Oscillator Basics

2.1 Crystal Oscillator Circuitry

A typical crystal oscillator circuit is shown in Figure 1. The oscillator circuit has one inverting amplifier, one feedback resistor (R), two capacitors (C_1 and C_2), and a quartz crystal (XTAL)

Figure 1. Basic Crystal Oscillator Circuit



During normal operation, the crystal and the capacitors form a π-network band-pass filter that provides a 180-degree phase shift and a voltage gain from the output to input at approximately the resonant frequency of the crystal.

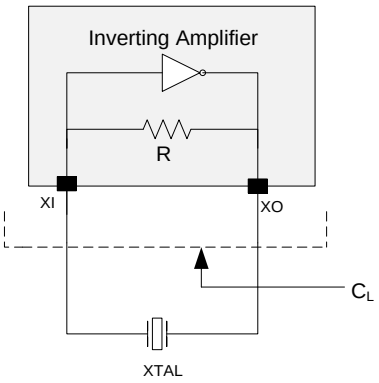
The resistor R acts as a feedback resistance, biasing the inverter in its linear region of operation and effectively causing it to function as a high-gain inverting amplifier.

The combination of the 180-degree phase shift from the π- network and the negative gain from the inverter results in a positive loop-gain (positive feedback), making the bias point set by the feedback resistor unstable and leading to oscillation.

2.2 Load Cap Value (C_L)

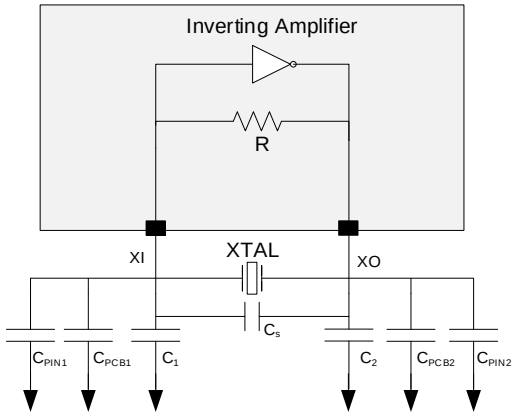
The load capacitance is the total capacitance seen by the crystal looking into the rest of the circuit (see Figure 2).

Figure 2. Load Capacitance



The correct operation of a crystal oscillator circuit depends on the value of the total load capacitance value C_L that is composed of not only the two capacitors C_1 and C_2, but also the parasitic capacitances and pin capacitances.

Figure 3. Total Load Capacitance Including Parasitic Capacitance and Pin Capacitance



$C_{T1} = C_1 + C_{PCB1} + C_{PIN1}$

$C_{T2} = C_2 + C_{PCB2} + C_{PIN2}$

$$C_L = \frac{C_{T1} * C_{T2}}{C_{T1} + C_{T2}} + C_S$$ Equation 1

Where,

C_1, C_2 = Node Capacitance at XI and XO

C_{T1}, C_{T2} = Total node capacitance (including pin capacitance and parasitic capacitance)

C_{PCB1}, C_{PCB2} = Parasitic Capacitance between PCB pads of the crystal

C_{PIN1}, C_{PIN2} = Input capacitance of the oscillator pins

C_S = PCB stray capacitance

C_L = Total load capacitance seen by the crystal

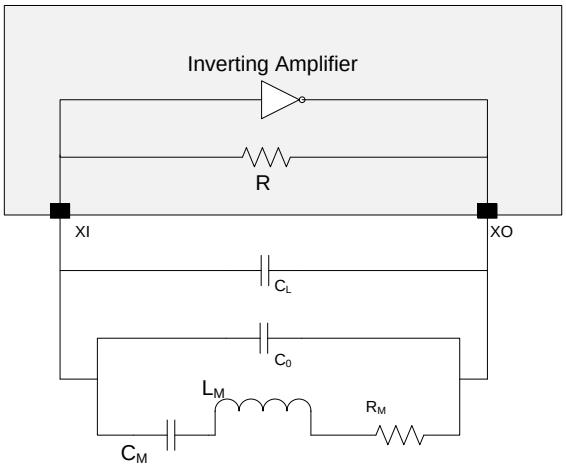
The load capacitance required to generate an accurate crystal frequency is specified in the crystal datasheet. Capacitors C_1 and C_2 in Figure 1 should be chosen such that the value of C_L from Equation 2 matches the datasheet value.

The crystal will not oscillate at the frequency specified in the crystal datasheet if the passive crystal load circuitry does not provide the load capacitance (C_L) that is required for the crystal. Too low a capacitive load will result in a crystal oscillator frequency higher than the specified value, while too high a capacitive load will result in a lower oscillation frequency. This frequency offset will be directly translated to an offset in the RF carrier frequency and symbol timing accuracy of the device.

2.3 Equivalent RLC Circuit of the Crystal

Figure 4 shows the equivalent RLC circuit of the crystal.

Figure 4. Equivalent RLC Circuit of the Crystal



Where,

R_M = Motional resistance of the crystal

C_0 = Shunt capacitance

C_L = Load capacitance

C_M = Motional capacitance

L_M = Motional inductance

This circuit represents the parallel resonant mode. The frequency of oscillation is derived from Equation 2.

$$f_p = f_s * (1 + \frac{C_M}{2C_L}) \quad \text{Equation 2}$$

Where, $f_s = \frac{1}{2\pi\sqrt{L_M C_M}}$ is the series resonant frequency of the oscillator and f_p is the frequency of oscillation.

2.3.1 Equivalent Series Resistance (ESR)

This resistance represents the resistive element of the quartz crystal equivalent circuit. It is the equivalent impedance of the crystal at its natural resonant frequency (series resonance). The gain of the oscillator amplifier directly depends on the ESR: the higher the ESR value, the higher will be the gain required by the oscillator amplifier to oscillate at the desired frequency.

Internal oscillator circuits in every chip are designed to work with a maximum specified value of ESR such that the biasing point of the amplifier becomes unstable, resulting in oscillations.

Equation 3 gives the ESR for a crystal

$$ESR = R_M * (1 + \frac{C_0}{C_L})^2 \quad \text{Equation 3}$$

See the crystal datasheet for the ESR value. Its value depends on the crystal frequency and usually varies from 20 Ω to 100 Ω.

2.4 Drive Level

This is a measure of the amount of power dissipated (in µW) across the crystal. The maximum drive level is the maximum power a crystal can dissipate while still maintaining the specified performance. High drive-level causes problems such as instability and aging. The drive level should be considered in your design to avoid premature aging and damage to the crystal. You should choose a crystal whose drive level specification meets your design drive level requirement.

2.5 PPM Error

The crystal clock accuracy is usually defined in parts per million (ppm), which means the inaccuracy in the number of clock cycles measured per 10^6 (1 million) clock cycles.

$$ppm = \frac{(measured\ freq - Expected\ freq)(in\ Hz)}{Expected\ freq\ (in\ MHz)}$$

Equation 4

For example, if a 24-MHz crystal oscillator provides a clock of 23.999928 MHz, then the clock accuracy is -72/24 = -3 ppm

There are many reasons for ppm variation. Some of these reasons include:

- **Initial Tolerance (ppm):** The offset from the nominal crystal frequency for different devices under identical conditions (temperature, PCB layout, voltage, etc). This is a datasheet parameter.
- **Temperature Drift (ppm):** The offset from the nominal crystal frequency over temperature.
- **Aging (ppm/year):** The cumulative change in the frequency of oscillation experienced by a crystal over a year. The variation due to aging may be different in different years. This may be +/- 1 ppm for the first year and +/- 20 ppm after 15 years.
- **Pullability**: This is the change in crystal oscillator frequency due to a change in load capacitance. It is typically 20 ppm/pF. The parasitic load capacitance varies between 2.5 pF to 3.5 pF, which can cause the ppm to shift outside the BLE specification limit of +/-50 ppm. Therefore, the board parasitic capacitance should also be considered while choosing the load capacitor value for the crystal.
- **Parasitic Capacitance:** Stray capacitances from the PCB and pin input add to the overall parasitic capacitance seen by the crystal. This parasitic capacitance changes the load capacitance value.

3 Effects of Inaccurate ECO Crystal Frequency on RF Performance

The data transmitted over BLE can have a symbol rate of 1 mega-symbol per second (symbol timing of 1 µs) or 2 mega-symbols per second (symbol timing of 0.5 µs). Here, a symbol refers to one bit of baseband signal that modulates the carrier. For best RF performance, the symbol timing accuracy should be better than ± 50 ppm. In addition, the offset in the RF center frequency during a packet transmission should not exceed ± 150 kHz (See Frequency Error (Transmit Center Frequency Tolerance)).

Symbol timing and centre frequency are both derived from the crystal oscillator onboard PSoC /PRoC BLE devices. The crystal oscillator onboard PSoC 4/PRoC BLE devices should be used with a 24-MHz crystal, while that onboard PSoC 6 BLE devices supports both 16-MHz as well as 32-MHz crystals. You should use a crystal that meets the BLE specification because the offset in the crystal oscillator clock directly impacts the RF performance

A higher RF center-frequency offset of the transmitter increases transmission leakages in adjacent channels. This leakage has the following undesirable effects:

- Higher interference for receivers in adjacent channels
- Possibility of not meeting the radio specifications
- Increase in the spurious spillover in the adjacent channel that could result in failures in a band-edge test

A higher frequency offset of the receiver with respect to the transmitter could cause a part of the received energy to fall outside the bandwidth of the baseband filter. This causes valid signal energy to be lost in the filter and results in a reduced sensitivity (and hence a reduced range).

For GFSK receivers, the frequency offset also causes a DC shift in the demodulated output and could result in the decoded symbols to be erroneous. This results in a higher packet error rate (PER) and reduced sensitivity.

Apart from these, a higher frequency offset of the receiver makes the receiver move closer to the adjacent channel. Consequently, signals in adjacent channels impact the reception, thus reducing the selectivity.

The most important measure of RF performance is the receiver sensitivity. For BLE, receiver sensitivity is the lowest power-level up to which the receiver can receive packets with a maximum of 30.8 percent packet error rate (PER). Internal receiver characterization has shown that the receiver sensitivity can degrade by as much as 1 dBm if the ECO clock drifts beyond ± 20 ppm.

Another important RF performance parameter is the Carrier-to-Interference (C/I) ratio expressed in dB. This ratio indicates how strong or weak can the interferer signal be as compared to the carrier signal such that PER is ≤ 30.8 percent. A more negative C/I ratio is better as it means that even if the carrier power level is much weaker than the interference power level (i.e., strong interference), the receiver can still receive packets with a maximum of 30.8 percent PER. The C/I ratio can degrade by as much as 5 to 8 dBm if the ECO clock is inaccurate by -20 ppm.

While the chosen crystal may have a good accuracy, the ppm may vary due to the reasons mentioned in Crystal Oscillator Basics. This requires the ability to tune the ppm to ensure a good RF performance.

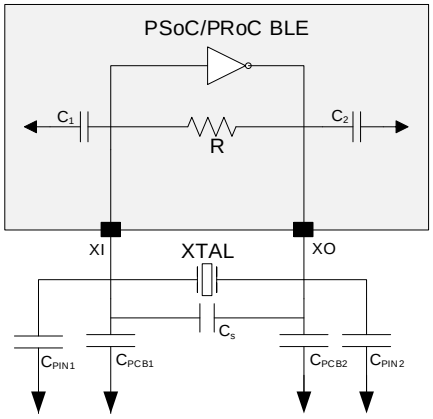
4 Crystal Tuning Technique for ECO

Tuning is the method of correcting any inaccuracy in the crystal clock that may occur in the system. Tuning aims at improving the accuracy of the generated frequency by adjusting the load capacitance value seen by the crystal oscillator circuit.

Typically, tuning is done by directly adjusting the externally mounted load capacitance values or by having an external variable capacitor that can offset the mounted load capacitance value. However, external capacitors add additional system cost.

PSoC/PRoC BLE devices have internal programmable trim capacitances (instead of an externally mounted load capacitance) on pins XI and XO (shown in Figure 5) as a part of the oscillator circuit. These load capacitances are tuned by firmware to correct the load capacitance offset, and therefore the frequency.

Figure 5. Internal Programmable Trim Capacitors in PSoC/PRoC BLE Devices



For tuning, the ECO clock is routed out of the chip to a GPIO to measure the clock accuracy. The clock accuracy is measured with a high-precision frequency measurement instrument like a universal time interval counter (Model SR620 from Stanford Research Systems). Equation 4 can then be used to determine the inaccuracy in the clock.

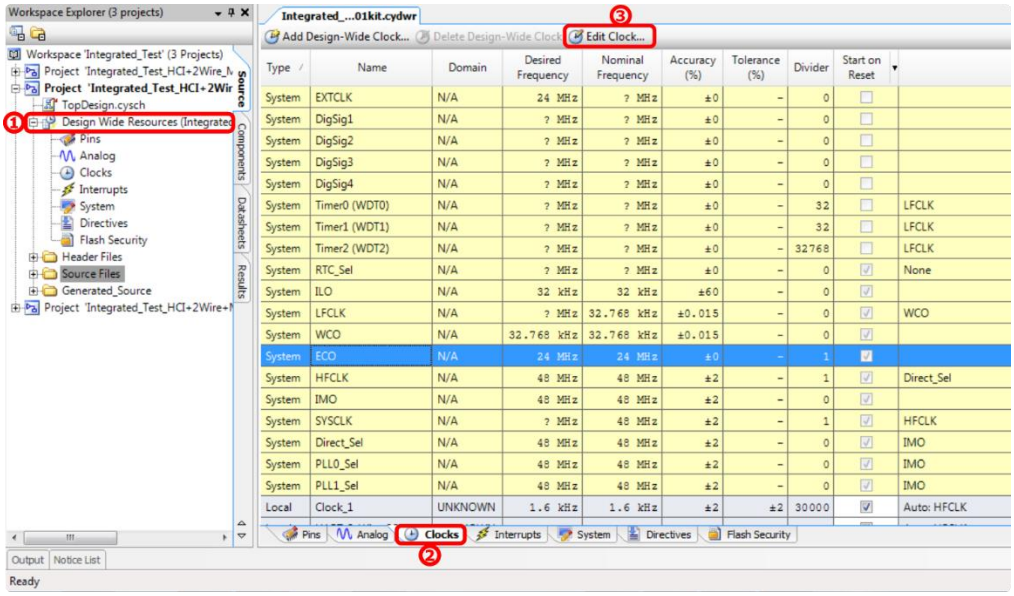
Next, it takes a simple three-step procedure to correct the clock inaccuracy by changing the value of the internal programmable capacitances C_1 and C_2. However, the procedure is different for PSoC 4/PRoC BLE and PSoC 6 BLE devices. Skip to the section applicable for your design.

4.1 Crystal Tuning Procedure for Designs with PSoC 4/PRoC BLE Devices

4.1.1 Designs with BLE Component V3.2 or Later

As mentioned earlier, the ECO clock frequency must be adjusted with ± 20 ppm accuracy to achieve the best RF performance. Use the following procedure to adjust the internal trimmer capacitors onboard PSoC 4/PRoC BLE devices and in-turn tune the ECO:

Figure 6. Step 1: Open the Configure System Clocks Window



Step 1: As shown in Figure 6, from the **Workspace Explorer** window, double-click on the **Design Wide Resources** tab in the active project. This opens the *<Project Name>.cydwr* file corresponding to your active project in a PSoC Creator™ window. Next, click on the **Clocks** tab in the Design Wide resources and click on the **Edit Clock...** button to open the **Configure System Clocks** pop-up window.

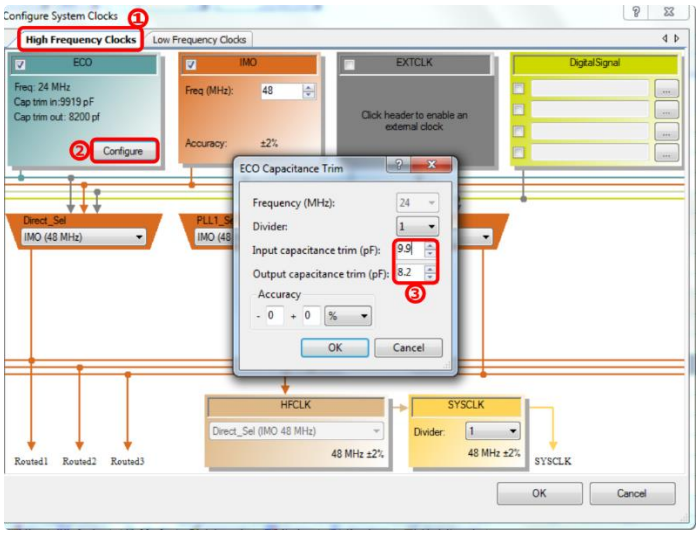
Step 2: In the **Configure System Clocks** pop-up window, select the **High Frequency Clocks** tab to open the clock settings for high-frequency clocks. From the window (Figure 7), click on the **Configure** button under **ECO** to open the **ECO Capacitance Trim** dialog box. Adjust the values of Input and output capacitance trim to reduce clock inaccuracy. Changes in C_1 and C_2 result in a change in C_L. Therefore, both values should be changed to tune the crystal properly. Even though there is no one-to-one look-up table to relate a change in capacitance value to a change in the ppm accuracy, a general practice is mentioned below:

- If the ppm is negative (i.e., the measured frequency is less than the crystal frequency), decrease the capacitance trim value on XI and XO because a smaller C_L value results in an increase in f_p according to Equation 2.
- If the ppm is positive (i.e., the measured frequency is more than the crystal frequency), increase the trim capacitance value because a larger C_L value results in a decrease in f_p according to Equation 2.
- For optimal phase noise, the total capacitance on the XI pin should be 0.8 times the total capacitance on the XO pin.

Step 3: Measure the clock inaccuracy and repeat Step 2 until the desired clock accuracy is achieved.

CAUTION: Ensure that you have installed the latest version of PSoC Creator before you start this procedure. This is important to ensure that your design employs the BLE Component Version 3.2 or later.

Figure 7. Step 2: Adjust C1 and C2 to Reduce the Clock Inaccuracy (PSoC 4/PRoC BLE Devices Only)



4.1.2 Designs with BLE Component V3.1 or Earlier

For PSoC 4/ PRoC BLE designs which are based on a BLE Component V3.1 or earlier, the clock inaccuracy can be corrected by changing the value of the internal programmable capacitances C_1 and C_2 using writes to the ECO trim register CYREG_BLE_BLERD_BB_XO_CAPTRIM. Details for this register are available in PSoC 4/PRoC BLE Registers Technical Reference Manuals (TRMs): PSoC 4 BLE Registers TRM and PRoC BLE Registers TRM. Following is the procedure along with a functional code (Code 1), for tuning the external crystal:

Step 1. Enable radio.

Step 2. Enable WCO.

Step 3. Enable ECO.

Step 4. Bring the ECO clock on a GPIO and observe the clock accuracy (Example - clock on Port 2 Pin 7).

Step 5. Trim the internal capacitance to achieve 0 ppm.

Code 1. Code to Trim the Crystal Load Capacitance

```
void trim_capacitance()
{

    /* Step1:Enable Radio */
    *(uint32*) CYREG_BLE_BLESS_RF_CONFIG = 0x01;

    /* Step2:Enable WCO */
    *(uint32*) CYREG_BLE_BLESS_WCO_CONFIG |= 0x80000000;

    /* Step3:Enable ECO */
    *(uint32*) CYREG_BLE_BLERD_DBUS = 0xC992;
    /* Step4:Configure pin 2[7] as ECO crystal Output */
    *(uint32*) CYREG_GPIO_PRT2_PC = 0xDB6DB6;
    *(uint32*) CYREG_HSIOM_PORT_SEL2 |= 0xA0000000;

    /* Step5:Trim Load Capacitance */
    *(uint32*) CYREG_BLE_BLERD_BB_XO_CAPTRIM = <Load Cap value >;
        }
```

Setting the Load Cap Value

Bits 15 and 7 of the CYREG_BLE_BLERD_BB_XO_CAPTRIM register are used for coarse control (adds 8.1 pF) of capacitance at nodes XI and XO respectively. The first seven bits of this register provide fine control (0.1011 pF/step) of the value of capacitance at node XI, whereas the last seven bits provide fine control (0.1011 pF/step) of the value of capacitance at node XO. Table 1 lists the values of capacitances at nodes XI (C_1) and XO (C_2) corresponding to different settings of this register.

Table 1. C_1 and C_2 Values Corresponding to CYREG_BLE_BLERD_BB_XO_CAPTRIM Register Setting

Decimal Value of Bits 14-8	C_1	Decimal Value of Bits 6-0	C_2
0	3.6900 pF	0	3.6900 pF
1	3.7911 pF	1	3.7911 pF
2	3.8922 pF	2	3.8922 pF
.....	.....	.....	.....
127	16.428 pF	127	16.428 pF

It is important to note that if you are using BLE Component V3.1 (or earlier) in your application, the ECO trim register is written with a default value as part of the BLE stack initialization. Therefore, the trim value should be written to the ECO trim register after the BLE stack initialization in the application so that the register holds the updated trim value. This sequence is shown in the code snippet Code 2.

Code 2. For BLE Component V3.1 (or earlier) Set CAP TRIM VALUE After BLE Stack Initialization

```
int main()
{

/* Stack Initialization */
CyBle_Start(EventCallback);

/* Write trim value */
*(uint32*) CYREG_BLE_BLERD_BB_XO_CAPTRIM = <CAP TRIM VALUE >;

for(;;)
    {

    CyBle_ProcessEvents();

     }
}
```

4.2 Crystal Tuning Procedure for Designs with PSoC 6 BLE Devices

As mentioned earlier, the ECO clock frequency must be adjusted to be accurate within ± 20 ppm to achieve the best RF performance. Use the procedure mentioned below to adjust the internal trimmer capacitors onboard PSoC 6 BLE devices and in-turn tune the ECO:

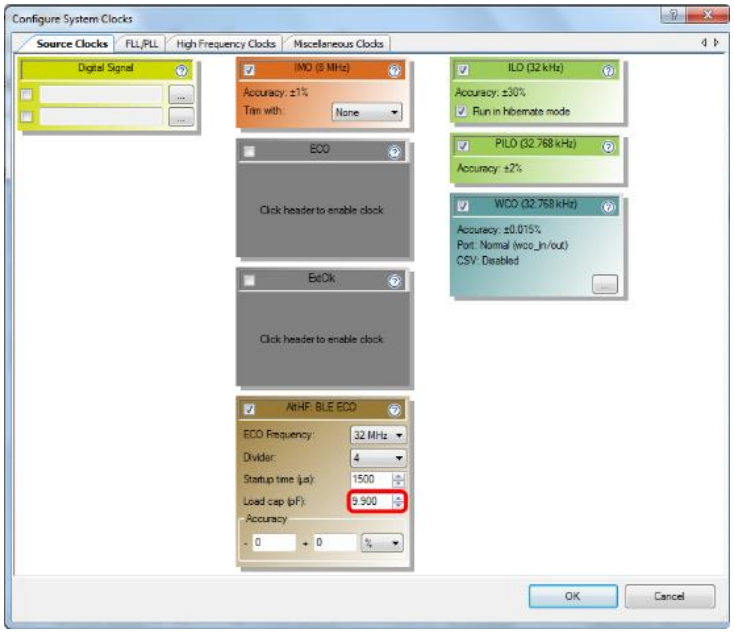
Step 1: As shown in Figure 6, from the **Workspace Explorer** window, double-click on the **Design Wide Resources** tab in the active project. This opens the *<Project Name>.cydwr* file corresponding to your active project in a PSoC Creator window. Next, click on the **Clocks** tab in the Design Wide resources and click on the **Edit Clock...** button to open the **Configure System Clocks** pop-up window.

Step 2: In the **Configure System Clocks** pop-up window, select the **Source Clocks** tab to open the clock settings for various source clocks. From the **Source Clocks** window (Figure 8), under **BLE ECO** box, set the value of **Load cap** to reduce the clock inaccuracy. Even though there is no one-to-one look-up table to relate a change in capacitance value to a change in the ppm accuracy, a general practice is mentioned below:

- If the ppm is negative (i.e., the measured frequency is less than the crystal frequency), decrease the **Load cap** value because a smaller C_L value results in an increase in f_p according to Equation 2.
- If the ppm is positive (i.e., the measured frequency is more than the crystal frequency), increase the **Load cap** value because a larger C_L value results in a decrease in f_p according to Equation 2.

Step 3: Measure the clock inaccuracy and repeat Step 2 until the desired clock accuracy is achieved.

Figure 8. Step 2: Adjust C_L to Reduce Clock Inaccuracy (PSoC 6 BLE Devices Only)



As can be observed from Figure 8, for PSoC 6 BLE devices, you can configure two parameters in the **BLE ECO** box: Startup time and Accuracy

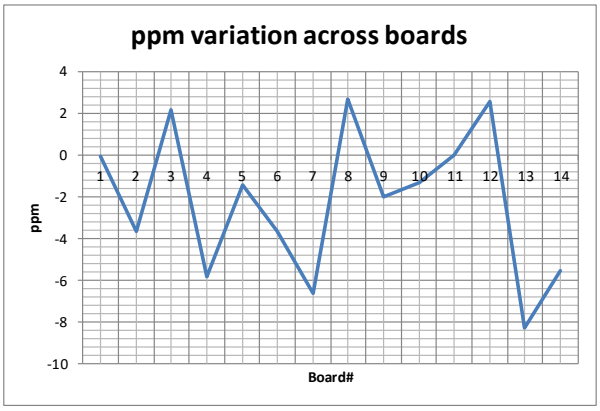
Startup Time
The “Startup time” is the time delay (in µs) from the instant when the firmware sets the BLE ECO ON, to the instant after which BLE ECO clock is enabled to the link layer. In this period, the BLE ECO clock is assumed to be unstable, and so the controller does not turn ON the clock to internal link layer (LL) logic until this period is over. Therefore, this parameter must be set to a value greater than the time required for the BLE ECO to stabilize after it is turned ON. The default value (Cypress-recommended value) of this parameter is set using the data from the internal characterization.

Accuracy
The accuracy must be set to the frequency stability of the external crystal used in your design. PSoC Creator uses this parameter to set the maximum achievable accuracy for the clocks which are sourced from the BLE ECO clock.

5 Is Tuning Required for Each Board?

Figure 9 shows the ppm variation measured for the same load cap value on 14 boards with the same PCB layout after tuning the C_L for one board. From this data, it is evident that the variation in crystal accuracy across boards is in the range of ± 7-8 ppm. This range of variation is permissible for optimum RF performance. Therefore, you don’t need to tune each board. You can tune a board once and use the same capacitance trim value for boards with the same PCB layout. After the trim value is determined for a device, the trim value should be written in the ECO Clock configuration in the *cydwr* file corresponding to the active project, as detailed in Crystal Tuning Technique for ECO.

Figure 9. ppm Variation Across Boards for the Same C_L

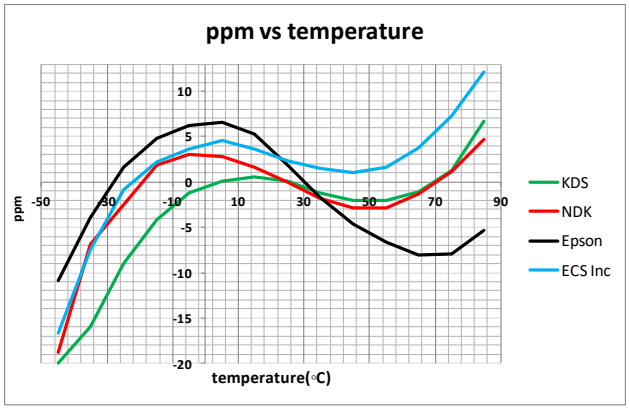


6 Crystal Analysis for ECO

6.1 Frequency Variation with Temperature

Figure 10 shows the frequency variation that was measured for different crystals with temperature.

Figure 10. ppm Variation with Temperature



This graph shows that the ppm variation for the four crystals across the temperature range of the device meets BLE specification of ± 50 ppm. However, other factors like aging, pullability, and stray capacitances can also change the crystal ppm. Therefore, the cumulative effect of all these factors on ppm should be within ± 50 ppm.

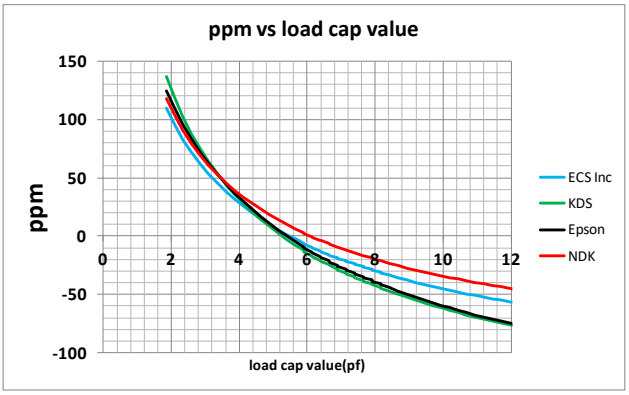
6.2 Frequency Variation with Load Cap Value

Figure 11 shows the frequency variation for crystals that were measured with the load capacitance value.

This graph shows that the frequency can be changed exponentially from positive offset (positive ppm) to negative offset (negative ppm) by changing the load capacitance value. This load capacitor is internal to the PSoC/PRoC BLE device.

However, it is important to note that the ppm variation with the load capacitance value depends heavily on the PCB layout of the device. A PCB layout with a lot of stray capacitances may leave the frequency insensitive to changes in internal trim capacitances; therefore, tuning may become difficult. Some general guidelines to reduce parasitic capacitance on the board are discussed in the Layout Considerations for PCB section.

Figure 11. ppm Variation with Load Cap Value



7 Cypress Recommendations for External Crystal Oscillator (ECO)

7.1 ECO for PSoC 4/PRoC BLE Devices

Cypress recommends a crystal based on the following five parameters:

1. **Equivalent series resistance (ESR):** The maximum ESR requirement for the 24-MHz crystal to be used with PSoC 4/PRoC BLE devices is **60 Ω** at 24-MHz. Therefore, the crystal ESR should be ≤ 60 Ω.
2. **Drive level:** The drive-level specification for PSoC 4/PRoC BLE devices is maximum **100 µW,** so the chosen crystal should be able to support a drive level of up to 100 µW. Therefore, a crystal whose maximum drive-level specification is ≥ 100 µW (meaning that it can sustain at least 100 µW) would suffice.
3. **Load Capacitance:** The oscillator of PSoC 4/PRoC BLE devices is designed to work with an 8-pF load capacitance, which requires that the chosen crystal have an 8-pF load capacitance.
4. **Pullability:** Pullability should be low. If not, parasitic capacitances will cause a large variation in the crystal frequency.
5. **ppm variation across temperature range of the device:** Temperature range for PSoC 4/ PRoC BLE devices is -40 to 85 ºC. The chosen crystal ppm should meet the BLE requirement (within ± 50ppm) across the chip-supported temperature range. To meet the BLE requirement, Cypress recommends using crystals with frequency tolerance within ± 20 ppm.

Table 2 summarizes the crystals that were used for internal characterization for use with PSoC 4/PRoC BLE devices.

Table 2. Drive Level and ESR Values for Different Crystals for Use with PSoC 4/PRoC BLE Devices

Crystal Part Number	Crystal Vendor	Drive Level (Max in µW)	ESR (Max in Ω)
ECS-240-8-36CKM	ECS, Inc.	100	60
TSX 3225	Epson	200	40
NX2520SA	NDK	200	60
DSX321SH	KDS	200	60

7.2 ECO for PSoC 6 BLE Devices

Cypress recommends a crystal based on the following five parameters:

1. **Equivalent series resistance (ESR):** PSoC 6 BLE devices offer the user a choice between 16-MHz and 32-MHz crystals. The maximum ESR requirement for a 16-MHz crystal to be used with PSoC 6 BLE devices is 250 Ω, while that for the 32-MHz crystal is 100 Ω.
2. **Drive level:** The drive-level specification for PSoC 6 BLE devices is maximum **100 µW.** The chosen crystal should be able to support a drive level of up to 100 µW. Therefore, a crystal whose maximum drive-level specification is ≥ 100 µW (meaning that it can sustain at least 100 µW) would suffice.
3. **Load Capacitance:** The oscillator of PSoC 6 BLE devices the chosen crystal can have a load capacitance ranging from 8 pF to 12 pF.
4. **Pullability:** Pullability should be low. If not, parasitic capacitances will cause a large variation in the crystal frequency.
5. **ppm variation across temperature range of the device:** Temperature range for PSoC 6 BLE devices is –40 to 85 ºC. The chosen crystal ppm should meet the BLE requirement (within ± 50ppm) across the chip-supported temperature range. To meet the BLE requirement, Cypress recommends using crystals with frequency tolerance within ± 20 ppm.

Table 3 summarizes the crystals that were used for internal characterization for use with PSoC 6 BLE devices.

Table 3. Drive Level and ESR Values for Different Crystals for Use with PSoC 6 BLE Devices

Crystal Part Number	Crystal Vendor	Crystal Frequency	Drive Level (Max in µW)	ESR (Max in Ω)
NX2520SA-16MHZ-STD-CSW-5	NDK	16 MHz	200	80
CX3225GB16000D0HPQCC	AVX Corp	16 MHz	100	80
ECS-160-10-36-JGN-TR	ECS Inc.	16 MHz	100	80
CX3225SB32000D0FPLCC	AVX Corp	32 MHz	100	50
FA-20H 32.0000MF20X-K3	EPSON	32 MHz	200	50
NX3225SA-32MHZ-EXS00A-CS02368	NDK	32 MHz	100	50

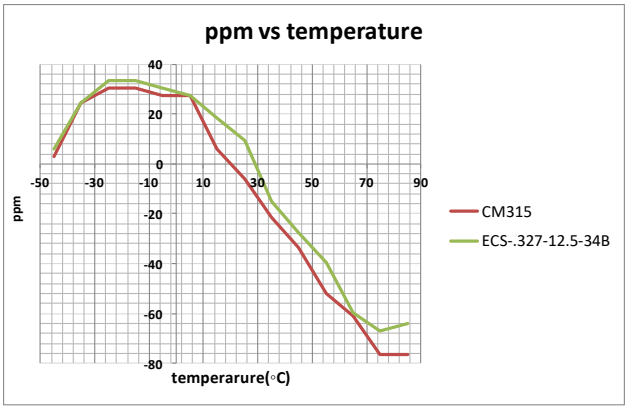
In a nutshell, it is recommended to use those crystals that have their ppm specification meeting the BLE requirements across the chip-supported temperature range. The crystal must also meet the ESR and drive-level requirements for PSoC4 /PRoC BLE and PSoC 6 BLE devices. After the crystal is chosen, the crystal tuning method suggested earlier must be used to tune the crystal to be accurate within ± 10 ppm to achieve the best RF performance.

8 Crystal Analysis for WCO

8.1 Frequency Variation with Temperature

The BLE specification for low-frequency crystal is ± 500 ppm. Figure 12 illustrates the accuracy in ppm over temperature for a typical external WCO crystal.

Figure 12. ppm Variation with Temperature



The less the variation, the better it is for low-power operations. This is because a larger drift in the low-frequency clock requires the device in the Peripheral role to listen for a master anchor point over a larger listening time window at the link layer, thus consuming extra power.

8.2 Start-Up Time and ESR

The startup time indicates how long it takes for the WCO to provide a stable 32.768-kHz clock from the time the block is enabled.

There are three distinct operating power modes for the WCO:

1. Power-down mode (PDM)

2. High-power mode (HPM)

3. Low-power mode (LPM)

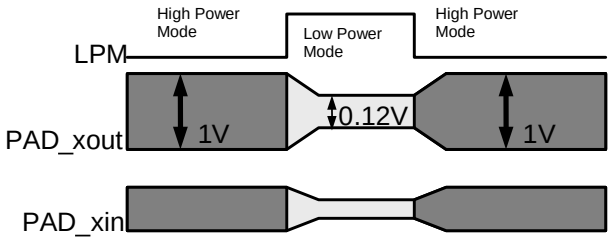
The WCO is started in HPM. After it is stable, it is switched to LPM to conserve power. The startup time with HPM is 500 ms.

After the WCO has switched to LPM, no additional switching of modes is required for the block while the chip is in active mode or when the chip is switching between active and deep-sleep modes. However, if the chip switches to the hibernate mode or stop mode, then the entire WCO startup sequence is initiated again because the chip is reset.

Crystal amplitude in HPM is limited to approximately 1-V pp while in LPM it is limited to approximately 0.12 V pp.

The explained WCO start up sequence is taken care of as a part of the PSoC Creator initialization code; you do not have to do this in the application code.

Figure 13. PAD Voltages in Power Modes for WCO

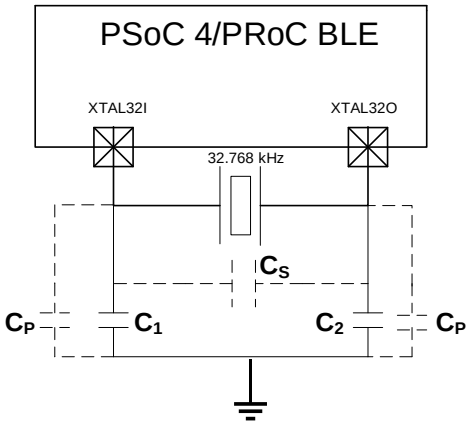


The start-up time is directly related to the ESR of the external crystal. The larger the ESR of the crystal, the longer the time it takes to start up because the amplification of oscillations during startup takes longer with a larger resistance in series with the external load capacitors. Because the ESR of the crystal represents this series resistance, longer start-up times are evident. Crystal ESR characterization shows that the WCO design covers all crystal manufacturers' ESR ranges from 35 to 70 kΩ.

8.3 Load Capacitance Value for Designs with PSoC 4/PRoC BLE Devices

Figure 14 shows the external application view of a PSoC 4/PRoC BLE device. Note that no parallel or series resistors are required externally (they are present on the chip). The only external requirements are a 32.768-kHz watch crystal and two load capacitors, C_1 and C_2, such that the total effective load capacitance C_L is 6 pF to 12.5 pF depending on the crystal chosen.

Figure 14. External Application View of PSoC 4/PRoC BLE Devices



$$C_L = \frac{(C_1 + C_P) \times (C_2 + C_P)}{(C_1 + C_2 + 2C_P)} + C_S$$

C_L – From crystal datasheet
C_1, C_2 – External capacitors
C_P – Package pin to ground capacitance
C_S – PCB stray capacitance

A higher C_1/C_2 ratio results in a higher current consumption but improved duty cycle.

Based on extensive characterization, a ratio of 2:1 ($C_1 = 2 \times C_2$) for the external capacitors is found to be optimal with respect to the performance and power consumption. The tradeoff for using a 2:1 ratio is slightly higher I_{CC} (Integrated Chip Current) of up to 100 nA. For a 2:1 ratio, the recommended external capacitor values are:

C_1 = 37.5 pF, C_2 = 18.75 pF (for C_L = 12.5 pF)

C_1 = 18 pF, C_2 = 9 pF (for C_L = 6 pF)

Note that the C_P and C_S values are assumed be zero for the above calculations.

8.3.1 CL and Clock Accuracy

The parasitic capacitance due to trace lines and pads can vary depending on the board layout. You should take into account the parasitic capacitance of each leg while calculating the load capacitance.

The load capacitance may be further tuned to achieve a better clock accuracy. This can be done as follows:

- If the average ppm is negative (i.e., the measured frequency is less than 32.768 kHz), decrease both C_1 and C_2 capacitance values while keeping the ratio of C_1 to C_2 to within 10 percent of the recommended 2:1 ratio (a ratio of 1.8 to 2.2 is acceptable if exact capacitance values are not available). However, if the negative ppm change is very small, then only C2 can be changed.
- If the average ppm is positive (i.e., the measured frequency is more than 32.768 kHz), increase both C_1 and C_2 capacitance values while keeping the ratio of C_1 to C_2 to within 10 percent of the recommended 2:1 ratio (a ratio of 1.8 to 2.2 is acceptable if exact capacitance values are not available). However, if the positive ppm change is very small, then only C_2 can be changed.

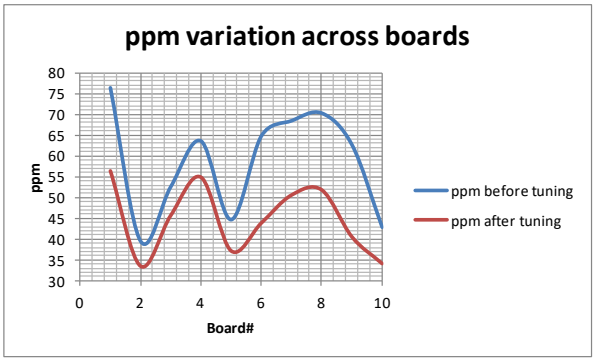
8.3.2 Frequency Variation across Boards

Table 4 and Figure 15 show the frequency offset (ppm) for a WCO measured across different boards having the same load capacitance values (in the ratio of 2:1). The table also shows how tuning the load capacitance within the recommended 10 percent variation range further reduces the ppm. Tuning is done only for one board; the same tuned capacitor values are used for all the boards.

Table 4. ppm Across Boards for 2:1 Cap Ratio

Board	ppm Before Tuning	ppm After Tuning
1	76.29	56.45
2	39.36	33.56
3	52.49	45.77
4	63.47	54.93
5	44.55	37.23
6	64.69	43.94
7	68.35	50.65
8	70.19	51.87
9	62.56	40.58
10	42.72	34.17

Figure 15. ppm Variation Across Boards for Same Load Capacitances

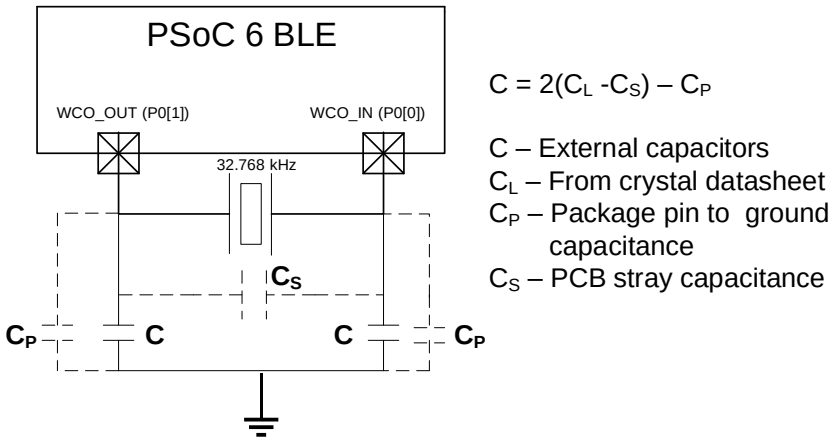


The ppm variation across boards with the same load capacitor value is approximately 20 ppm. This is acceptable for BLE, and therefore, you do not need to tune every board. You can use this approach for mass production, where you tune 4-5 boards to find out the optimum load capacitance values and then use the same capacitance value for all the boards during production.

8.4 Load Capacitance Value for Designs with PSoC 6 BLE Devices

Figure 14 shows the external application view of a PSoC 6 BLE device. Note that no parallel or series resistors are required externally (they are present on the chip). The only external requirements are a 32.768-kHz watch crystal and two load capacitors of equal value (C), such that the total effective load capacitance C_L matches the load capacitance value specified in the datasheet of the crystal.

Figure 16. External Application View of PSoC 6 BLE Devices



The external load capacitors for the WCO are calculated as:

$$C = 2(C_L - C_S) - C_P$$

Where,

C – External capacitors

C_L – Crystal load capacitor as per the crystal datasheet

C_S – PCB stray capacitance. A well-designed PCB to minimize the stray capacitance includes a grounded copper wire between the crystal input and output wires.

C_P – Package pin to ground parasitic capacitance (typical value of 3 pF. See the device datasheet for more details on pin parasitic capacitance).

The recommended external capacitor value is, C = 22 pF (for C_L = 12.5 pF, C_P = 3 pF, C_S = 0 pF).

9 Using an External Clock Source for WCO

9.1 Designs with PSoC 4/PRoC BLE Devices

It is possible to externally drive the main oscillator through external crystal pins. Make the following settings in the hardware:

1. Connect the external clock source to the XTAL32O pin.
2. Leave the XTAL32I pad floating. If floating is not desirable, ensure to have an impedance of at least 500 kΩ between the XTAL32I pad and ground.
3. Provide an external clock source that toggles from 0 V to a minimum of 1.0 V, or 0 V to a maximum of 1.6 V.
4. Ensure that the duty cycle of the external clock is between 20 and 80 percent.

To use an external clock in firmware, do the following:

1. Disable the WCO and select ILO for LFCLK in the **Low Frequency Clocks** tab of the **Configure System Clock** window in the *.cydwr* file.
2. Set the EXT_INPUT_EN (bit 2) bit to '1' in the BLE_BLESS_WCO_CONFIG register in firmware before enabling the WCO.
3. Start the WCO by calling the `CySysClkWcoStart();` function.
4. Select the WCO as the LFCLK source by calling the `CySysClkSetLfclkSource(CY_SYS_CLK_LFCLK_SRC_WCO);` function.
5. Stop the ILO by calling the `CySysClkIloStop();` function.

Code 3 shows a sample code for using the external clock source for the WCO:

Code 3. Code for Using External Clock Source for WCO

```
int main()
{
    /*Enable External Clock*/
    CY_SYS_CLK_WCO_CONFIG_REG |= CY_SYS_CLK_WCO_EXT_INPUT_EN;

    /*Start WCO */
    CySysClkWcoStart();

    /*Select WCO as the clock source*/
    CySysClkSetLfclkSource(CY_SYS_CLK_LFCLK_SRC_WCO);

    /*Stop ILO*/
    CySysClkIloStop();

    CyGlobalIntEnable;
    /* Stack Initialization */
    CyBle_Start(EventCallback);

    for(;;)
    {
        CyBle_ProcessEvents();
    }
}
```

9.2 Designs with PSoC 6 BLE Devices

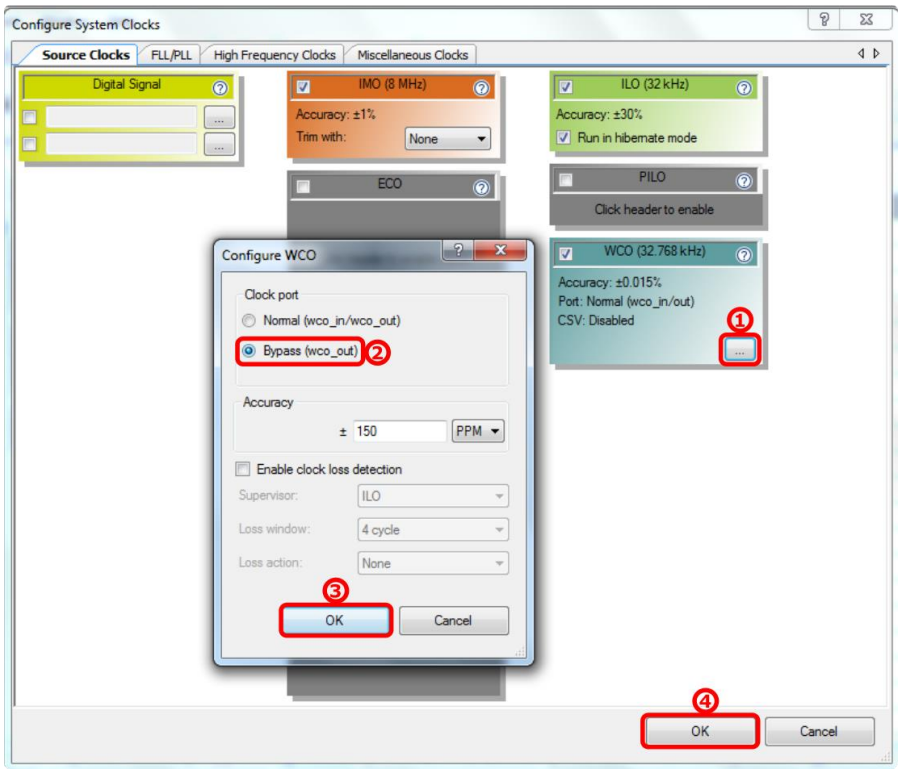
Make the following settings in the hardware:

1. Connect the external clock source to the XOSC_O pin.
2. Ground the XOSC_I pad.
3. Provide an external clock source that toggles from 0 V to V_{DDD} supply levels.
4. Ensure that the duty cycle of the external clock is between 20 and 80 percent.

Next, make the following changes in firmware:

1. As shown in Figure 6, open the **Configure Clock System** window from the active project's cydwr file.
2. In the **Configure Clock System** window (Figure 17), under the WCO box, select the button labeled **…** to open the **Configure WCO** window.
3. Select the **Bypass (wco_out)** button in the **Configure WCO** window and click **OK**.

Figure 17. Configure an External Clock Source as WCO



10 Recommendations for WCO

The following factors should be considered while choosing the WCO crystal:

1. **ESR:** It should be a maximum of 70 kΩ for the correct operation of the crystal circuitry. A higher ESR means a longer start-up time.
2. **Drive Level:** The maximum drive level of the crystal should be ≥ 1 µW.
3. **ppm variation across the device temperature range:** The less the ppm variation, the better it is for power consumption. Choose a crystal that doesn't have more than ± 50 ppm variation in frequency at room temperature after meeting the 2:1 ratio recommendation for load capacitance values.
4. **Size:** The size of the crystal should be chosen such that it is as small as possible, while meeting the three requirements listed earlier. The ESR of the crystal varies inversely with the crystal size.

Table 5. ESR and Size for WCO Crystals

Part Number	Mfr	Drive Level	Max ESR	Size (mm) L × W × H
ECS-.327-12.5-34B	ECS	1 µW	70 kΩ	3.2 × 1.5 × 0.9
CM315	Citizen	1 µW	70 kΩ	3.2 ×1.5 × 0.55
ECS-.327-12.5-32-TR	ECS	1 µW	50 kΩ	3.2 × 1.2 × 1

11 Layout Considerations for PCB

The crystal frequency is sensitive to parasitic capacitances, board noise, and electromagnetic interference. Keep the following points in mind while designing a PCB layout:

1. Position the crystal close to the chip to minimize the parasitic capacitance due to longer trace length and wider trace width, which would consequently alter the load cap value resulting in clock inaccuracy.
2. Minimize the pin-to-pin stray capacitance by having a ground shield trace between pin-connected traces.
3. Place the crystal on the same side of the PCB as the PSoC /PRoC BLE chip so that it provides a common ground plane without unnecessary vias on the crystal input/output traces.
4. Avoid floating pads of conductor near the crystal because this may introduce a stray capacitance.
5. Surround crystal components by a ground fill to avoid electromagnetic interference.
6. Keep fast-switching and high-current traces and pins such as LEDs away from the crystal circuitry.
7. Route PCB traces symmetrically to have the same parasitic capacitance on both crystal pins.

Figure 18 illustrates these points more clearly. Some of the layout considerations are highlighted in this figure. Figure 19 provides examples of some commonly made mistakes.

Figure 18. PCB Layout with Crystals

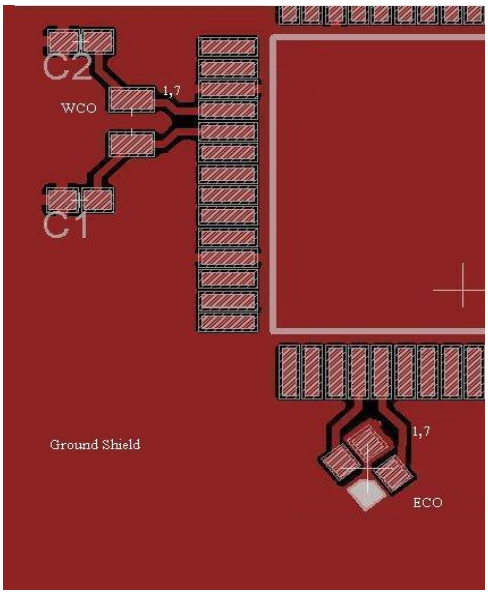
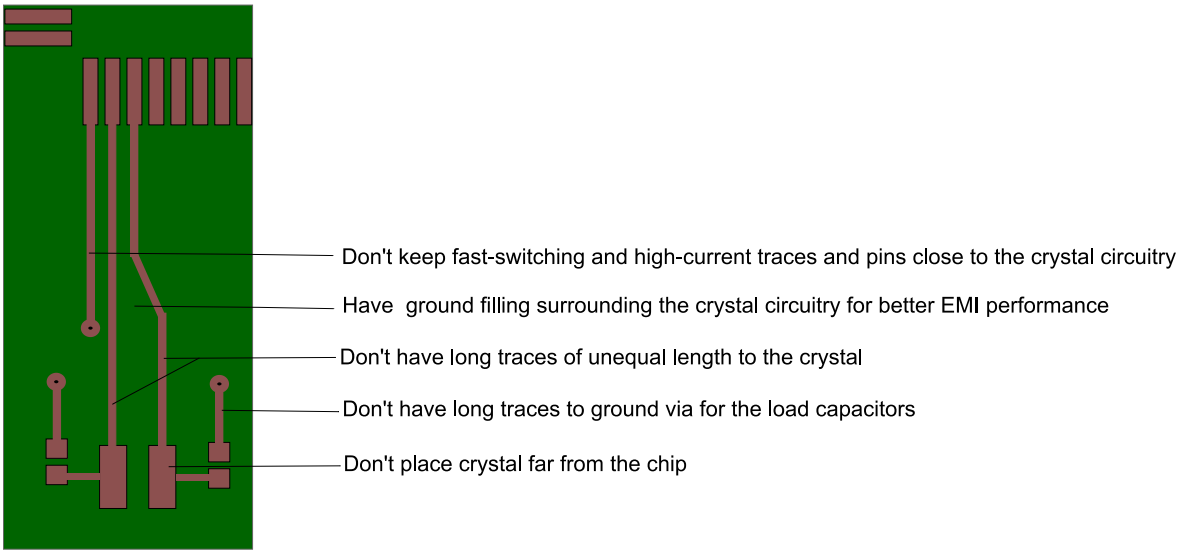


Figure 19. Example of Non-Recommended Layout Practices



12 Summary

- The BLE protocol requires that the ECO crystal clock accuracy is within ± 50 ppm.
- An inaccurate ECO crystal frequency results in poor RF performance.
- An inaccurate WCO crystal frequency results in high current consumption.
- The ECO crystal frequency inaccuracy can be corrected by following the procedure discussed here.
- Tuning is not required for every board; it is needed to be done only once during development.
- PSoC 4/PRoC BLE devices require 2:1 ratio for the two external capacitors for the WCO crystal for optimal power consumption and performance whereas the PSoC 6 BLE devices require balanced load capacitors (two capacitors of equal value).
- Temperature, aging, and parasitic capacitance cause variations in the crystal clock accuracy.
- The crystal should be positioned close to the chip to minimize parasitic capacitances.

13 References

Oscillator Concepts

- http://www.abracon.com/Support/facn_abracon_jul2011.pdf
- http://www.electronics-tutorials.ws/oscillator/crystal.html
- http://kunz-pc.sce.carleton.ca/thesis/CrystalOscillators.pdf
- http://www.am1.us/Local_Papers/U11625%20VIG-TUTORIAL.pdf

ECO Crystal Datasheets

- ECS-240-8-36CKM from ECS Inc.
- TSX-3225 from EPSON
- NX2520SA from NDK
- DSX321SH from KDS
- NX2520SA-16MHZ-STD-CSW-5 from NDK
- CX3225GB16000D0HPQCC from AVX Corp.
- ECS-160-10-36-JGN-TR from ECS Inc.
- CX3225SB32000D0FPLCC from AVX Corp.
- FA-20H 32.000MF20X-K3 from EPSON
- NX3225SA-32MHZ-EXS00A-CS02368 from NDK

WCO Crystal Datasheets

- ECS-.327-12.5-34B from ECS
- CM315 from Citizen
- ECS-.327-12.5-32-TR from ECS

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Appendix A. Frequency Error (Transmit Center Frequency Tolerance)

In BLE, the offset of the RF center frequency during the packet transmission should not exceed ±150 kHz for the whole packet. For example, when a radio transmits at the center frequency of 2480 MHz, it could be 2479.850 MHz, or 2480.150 MHz. This is the tolerance in the center frequency when transmitting a packet.

The center frequency is derived from the ECO and therefore any inaccuracies in the crystal frequency would be multiplied up to the center frequency.

The clock accuracy requirement after taking into account all the factors that affect clock accuracy is $\frac{150\ \text{KHz}}{2480\ \text{MHz}} = 60.5 \times 10^{-6} = 60.5\ \text{PPM}$

Document History

Document Title: AN95089 – PSoC /PRoC BLE Crystal Oscillator Selection and Tuning Techniques

Document Number: 001-95089

Revision	ECN	Submission Date	Description of Change
**	4643683	01/29/2015	New Application Note.
*A	4764564	05/15/2015	Updated template Updated associated part families
*B	5054825	12/17/2015	Updated MPNs to include PSoC4 BLE 256K and PRoC BLE 256K parts Added a section on using external clock for WCO Added layout examples of non-recommended layout practices
*C	5643907	03/27/2017	Updated App note to include ECO and WCO tuning techniques for PSoC6 BLE parts. Updated template
*D	5860171	09/22/2017	Updated for PSoC 6 Reorganized for improved readability
*E	6896441	06/10/2020	Updated the oscillator circuits to include stray capacitance (C_S) across the two crystal pins Updated the WCO section to recommend balanced load cap values for PSoC 6 BLE devices

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