AN94077

Advantages of 65-nm Technology Over 90-nm for Sync/NoBL® SRAMs

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AN94077 provides a detailed overview of the advantages of the 65-nm technology over 90-nm for Cypress's Sync/NoBL® (No Bus Latency™) family of SRAMs.

Contents

1 Introduction

The Cypress 65-nm Sync/NoBL® (No Bus Latency™) product family is a 100 percent backward-compatible die shrink of the 90-nm Sync/NoBL product family, with the option of including embedded error correcting code (ECC) for improved soft-error immunity and higher field quality.

The robustness of SRAM devices is often challenged when exposed to radiation. To reduce the maximum SER observed on the SRAM device, Cypress offers 65-nm Sync/NoBL SRAM devices with an ECC option. These devices have a maximum SER of 0.01 FIT/Mb compared with 216 FIT/Mb for the 65-nm SRAMs without ECC and 394 FIT/Mb for the 90-nm SRAM devices.

This application note provides a detailed overview of the key differences between 65-nm and 90-nm Sync/NoBL SRAMs and highlights the advantages of the 65-nm technology.

2 Comparison of 65-nm and 90-nm Sync/NoBL SRAM Devices

Table 1 summarizes the differences between 65-nm and 90-nm Sync/NoBL SRAM devices with respect to the active current (I_{DD}), standby current (I_{SB}), sleep-mode current (I_{ZZ}), switching current (I_{DDQ}), input/output capacitance, ECC, soft-error rate (SER), core voltage (V_{DD}) and I/O voltage (V_{DDQ}), power consumption, density, organization, and packaging.

Compared with 90-nm devices, you can see a significant improvement in terms of active current (I_{DD}) values, as they are reduced to almost half, while the standby current (I_{SB}) is reduced by a significant factor in 65-nm Sync/NoBL devices. With current values decreasing in 65-nm devices, the total power consumption evaluated for 65-nm SRAM devices as opposed to 90-nm SRAM devices is almost half. The input/output capacitance values are reduced in the new 65-nm SRAM devices.

Table 1. Features of 65-nm and 90-nm Sync/NoBL Devices

65 nm / 90 nm / 65 nm and 90 nm			Standard Sync SRAMs		NoBL SRAMs	
			Pipeline SRAMs	Flow-Through SRAMs	Pipeline SRAMs	Flow-Through SRAMs
Max Frequency [1]	36M & 18M	65 nm	250 MHz	133 MHz	250 MHz	133 MHz
		90 nm	250 MHz	133 MHz	250 MHz	133 MHz
I_{DD} – Active Current (Max) [2]	36M	65 nm	240 mA	170 mA	240 mA	170 mA
		90 nm	475 mA	310 mA	475 mA	310 mA
	18M	65 nm	200 mA	149 mA	200 mA	149 mA
		90 nm	350 mA	210 mA	350 mA	210 mA
I_{SB1} – Standby Current [3]	36M	65 nm	90 mA	90 mA	90 mA	90 mA
		90 nm	225 mA	180 mA	225 mA	180 mA
	18M	65 nm	80 mA`	80 mA	80 mA`	80 mA
		90 nm	160 mA	140 mA	160 mA	140 mA
I_{SB2} – Standby Current [3]	36M	65 nm	80 mA	80 mA	80 mA	80 mA
		90 nm	120 mA	120 mA	120 mA	120 mA
	18M	65 nm	70 mA	70 mA	70 mA	70 mA
		90 nm	70 mA	70 mA	70 mA	70 mA
I_{SB3} – Standby Current [3]	36M	65 nm	90 mA	90 mA	90 mA	90 mA
		90 nm	200 mA	180 mA	200 mA	180 mA
	18M	65 nm	80 mA	80 mA	80 mA	80 mA
		90 nm	135 mA	130 mA	135 mA	130 mA
I_{SB4} – Standby Current [3]	36M	65 nm	80 mA	80 mA	80 mA	80 mA
		90 nm	135 mA	135 mA	135 mA	135 mA
	18M	65 nm	70 mA	70 mA	70 mA	70 mA
		90 nm	80 mA	80 mA	80 mA	80 mA
I_{DDZZ} – Sleep Mode Standby Current [3]	36M	65 nm	75 mA	75 mA	75 mA	75 mA
		90 nm	100 mA	100 mA	100 mA	100 mA
	18M	65 nm	65 mA	65 mA	65 mA	65 mA
		90 nm	80 mA	80 mA	80 mA	80 mA
V_{DD} – Core Voltage	36M & 18M	65 nm	3.3 V or 2.5 V			
		90 nm				
V_{DDQ} – I/O Voltage	36M & 18M	65 nm	3.3 V/2.5 V (for 3.3-V V_{DD}) or 2.5 V (for 2.5-V V_{DD})			
		90 nm				

[1] Cypress also supports pipelined SRAMs with 200-MHz, 167-MHz, and 133-MHz frequency and flow-through SRAMs with 100-MHz frequency.

[2] The active currents specified for comparison are the values for x36 bus width SRAMs. Refer to the respective product datasheets for the active current (I_{DD}) for other density SRAMs at www.cypress.com/?id=95.

[3] Please refer to the device datasheet for the respective standby current test condition.

65 nm	90 nm	65 nm and 90 nm			Standard Sync SRAMs		NoBL SRAMs	
					Pipeline SRAMs	Flow-Through SRAMs	Pipeline SRAMs	Flow-Through SRAMs
Max Core Power Consumption [4]			36M	65 nm	792 mW	561 mW	792 mW	561 mW
				90 nm	1568 mW	1023 mW	1568 mW	1023 mW
			18M	65 nm	660 mW	492 mW	660 mW	492 mW
				90 nm	1155 mW	693 mW	1155 mW	693 mW
Total Power Consumption [5]			36M	65 nm	1037 mW	691 mW	1037 mW	691 mW
				90 nm	1813 mW	1153 mW	1813 mW	1153 mW
			18M	65 nm	905 mW	622 mW	905 mW	622 mW
				90 nm	1425 mW	1179 mW	1425 mW	1179 mW
$C_{I/O}$ – Input/Output Capacitance (TQFP/FBGA)			36M	65 nm	5 pF / 5 pF			
				90 nm	5.5 pF / 6 pF			
			18M	65 nm	5 pF / 5 pF			
				90 nm	5 pF / 9 pF			
Organization (Bus Width)			36M & 18M	65 nm	x18, x32, x36, x72	x18, x32, x36	x18, x32, x36, x72	x18, x32, x36
				90 nm	x18, x32, x36, x72	x18, x32, x36	x18, x32, x36, x72	x18, x32, x36
ECC [6]			36M & 18M	65 nm	Yes – single-bit error correction (SEC)			
				90 nm	No			
Max SER (FIT/Mb) [7]			36M & 18M	Logical single -bit upset (LSBU) – 65 nm (with ECC)	0.01			
				LSBU – 65 nm (without ECC)	216			
				LSBU – 90 nm	394			
Package			36M	65 nm	100-pin TQFP and 165-ball FBGA			
				90 nm	100-pin TQFP, 119-ball BGA, and 165-ball FBGA			
			18M	65 nm	100-pin TQFP, 119-ball BGA, and 165-ball FBGA			
				90 nm	100-pin TQFP, 119-ball BGA, and 165-ball FBGA			
JTAG [8]			36M & 18M	65 nm	Yes			
				90 nm				
32-Bit JTAG ID Code			36M & 18M	65 nm	90-nm and 65-nm devices share the same JTAG ID code			
				90 nm				

[4] Core Power = V_{DD} x I_{DD}

[5] Total Power = (Core Power) + (Switching Power) = (V_{DD} x I_{DD}) + (α x f x C_L x V_{DDQ}^2 x N)

[6] Cypress supports 65-nm devices with and without ECC features.

[7] For more details, see the application note AN54908 – Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates.

[8] JTAG option not offered in 100-pin TQFP packages.

2.1 Power Consumption and Junction Temperature Calculation

2.1.1 Power Dissipation (P_d)

Calculate the power dissipation based on the following equations:

P_d = Core Power + I/O Switching Power

$P_d = V_{DD} I_{DD} + \alpha f C_L V_{DDQ}^2 N$

Where:

V_{DD} = Core voltage

I_{DD} = Active current

α = Activity factor, or the ratio of frequency at which outputs toggle to clock frequency

f = Operating frequency

C_L= External load capacitance

V_{DDQ} = I/O voltage

N = Number of I/Os that are switching

Table 2 shows that 65-nm parts have better power ratings than 90-nm parts.

Table 2. Comparison of Power Dissipation between 65-nm and 90-nm Sync/NoBL Devices

65-nm Sync SRAM (36 Mb) ***CY7C1440KV33-250AXC***	**90-nm Sync SRAM (36 Mb)** ***CY7C1440AV33-250AXC***
V_{DD} = 3.3 V	V_{DD} = 3.3 V
I_{DD} = 240 mA	I_{DD} = 475 mA
α = 0.5	α = 0.5
f = 250 MHz	f = 250 MHz
C_L= 5 pF (100-pin TQFP package)	C_L= 5 pF (100-pin TQFP package)
V_{DDQ} = 3.3 V	V_{DDQ} = 3.3 V
N = 36	N = 36
Therefore: $P_d = V_{DD} I_{DD} + \alpha f C_L V_{DDQ}^2 N$ P_d = 3.3 V x 240 mA + 0.5 x 250 MHz x 5 pF x $(3.3\ V)^2$ x 36	Therefore: $P_d = V_{DD} I_{DD} + \alpha f C_L V_{DDQ}^2 N$ P_d = 3.3 V x 475 mA + 0.5 x 250 MHz x 5 pF x $(3.3\ V)^2$ x 36
Total Power Dissipation = 1037 mW	**Total Power Dissipation = 1813 mW**

65-nm Sync SRAM (18 Mb) *CY7C1370KV33-250AXC*	90-nm Sync SRAM (18 Mb) *CY7C1370D-250AXC*
V_{DD} = 3.3 V	V_{DD} = 3.3 V
I_{DD} = 200 mA	I_{DD} = 350 mA
α = 0.5	α = 0.5
f = 250 MHz	f = 250 MHz
C_L= 5 pF (100-pin TQFP package)	C_L= 5 pF (100-pin TQFP package)
V_{DDQ} = 3.3 V	V_{DDQ} = 3.3 V
N = 36	N = 36
Therefore: $P_d = V_{DD} I_{DD} + \alpha f C_L V_{DDQ}^2 N$ P_d = 3.3 V x 200 mA + 0.5 x 250 MHz x 5 pF x (3.3 V) ^{2} x 36	Therefore: $P_d = V_{DD} I_{DD} + \alpha f C_L V_{DDQ}^2 N$ P_d = 3.3 V x 350 mA + 0.5 x 250 MHz x 5 pF x (3.3 V)^2 x 36
Total Power Dissipation = 905 mW	**Total Power Dissipation = 1400 mW**

2.1.2 Junction Temperature (T_J)

Calculate the junction temperature based on the following equation:

$T_J = P_d \theta_{JA} + T_A$

Where:

θ_{JA} = Junction-to-ambient thermal resistance

T_A = Ambient temperature

P_d = Power dissipation

Table 3 shows that 65-nm parts have lower junction temperature ratings than 90-nm parts.

Table 3. Comparison of Junction Temperature (T_J) Between 65-nm and 90-nm Sync/NoBL Devices

65-nm Sync SRAM (36 MB) *CY7C1440KV33-250AXC (100-pin TQFP)*	90-nm Sync SRAM (36 MB) *CY7C1440AV33-250AXC (100-pin TQFP)*
θ_{JA} = 35.36 °C/W	θ_{JA} = 25.21 °C/W
T_A = 30 °C	T_A = 30 °C
P_d = 1037 mW	P_d = 1813 mW
Therefore: $T_J = P_d \theta_{JA} + T_A$ T_J = (1037m x 35.36) + 30 **Junction Temperature = 66.67 °C**	Therefore: $T_J = P_d \theta_{JA} + T_A$ T_J = (1813m x 25.21) + 30 **Junction Temperature = 75.7 °C**

65-nm Sync SRAM (18 MB) *CY7C1370KV33-250AXC (100-pin TQFP)*	90-nm Sync SRAM (18 MB) *CY7C1370D-250AXC (100-pin TQFP)*
θ_{JA} = 37.95 °C/W	θ_{JA} = 28.66 °C/W
T_A = 30 °C	T_A = 30 °C
P_d = 905 mW	P_d = 1425 mW
Therefore: $T_J = P_d\ \theta_{JA} + T_A$ T_J = (905m x 37.95) + 30 **Junction Temperature = 64.34 °C**	Therefore: $T_J = P_d\ \theta_{JA} + T_A$ T_J = (1425m x 28.66) + 30 **Junction Temperature = 70.84 °C**

3 Implementation of ECC in 65-nm Sync/NoBL SRAMs

The memory core is architected such that there is a very low probability of having a multi-bit error in a single data word. Bit interleaving, also called “column multiplexing,” is the conventional approach used to protect memory arrays from spatial multi-bit errors. Based on the principle of this architecture, the SEC type of ECC based on hamming code has been selected. The ECC consists of four additional “syndrome bits” for every nine data bits. The syndrome bits cannot be accessed from the external host, and there is no change to the package or pinout.

As shown in Figure 1, when new data is being written, the ECC logic will compute the four syndrome bits and store them into the memory core along with the data bits. In this example, the 36 bits from the data-in buffer are regrouped into four 9-bit words, which in turn are passed to an ECC encoder block. Similarly, for the x18 and x72 data-width architecture, input bits are regrouped into two and eight 9-bit words respectively. The four syndrome bits generated by the encoder block are stored with the data bits. Upon reading any data-word location, syndrome/parity bits will be analyzed in the ECC decoder block to determine if any failures occurred. Syndrome bits identify the location of the failing bit in the data word, and the data word is corrected by flipping the bad bit.

Figure 1. ECC Parity Bit Generation

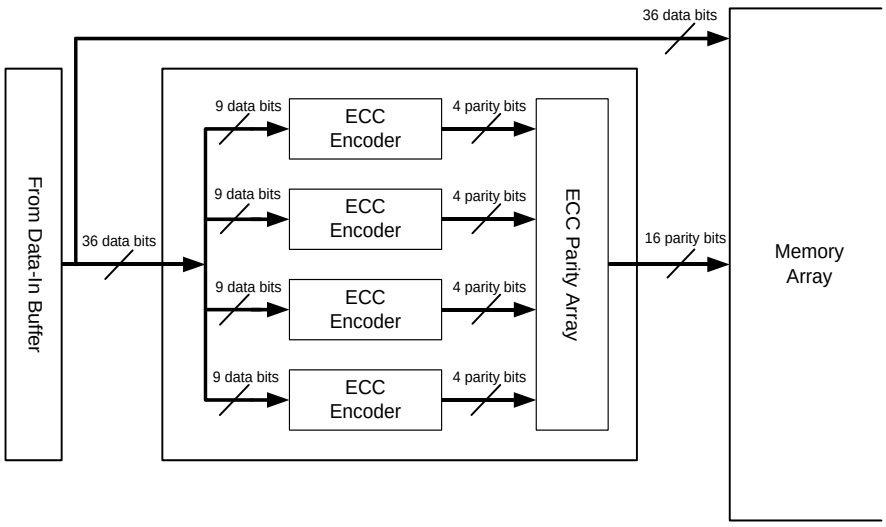
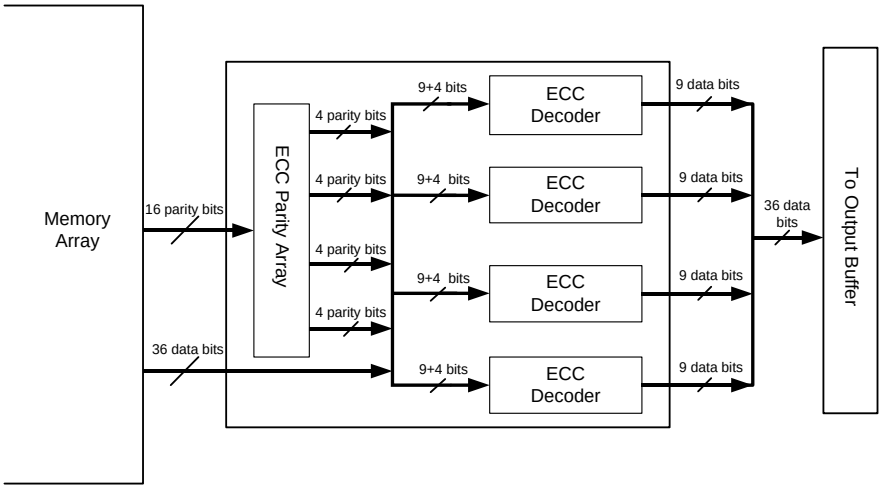


Figure 2 illustrates the process of single-bit error correction when a data word is read out of the SRAM. The ECC can correct a single-bit error in any or all data words. If the data in SRAM is retained for a long time without being rewritten, there is a remote chance that error will accumulate on multiple bits. If this occurs, the ECC will not be able to correct the multi-bit error, and the corrupted data will be output. Cypress recommends occasional data scrubbing to eliminate the occurrence of multi-bit errors.

Figure 2. Data Bit Correction

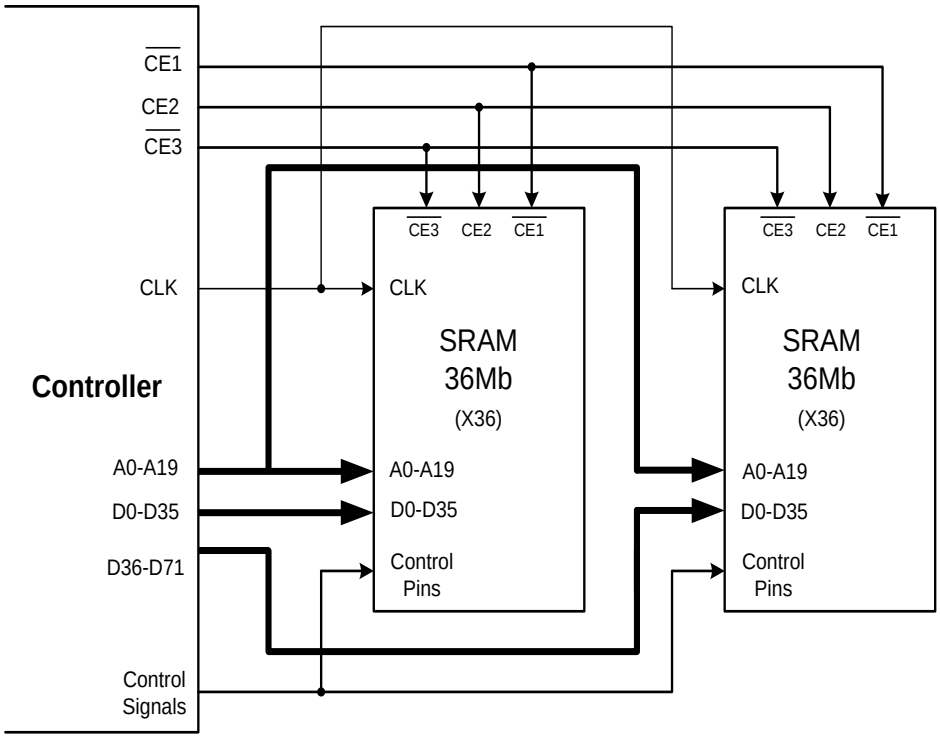


4 Width and Depth Expansion of 65-nm Sync/NoBL SRAMs

This section describes the recommended methods to expand the width and depth of 65-nm SRAMs, similar to the procedures in 90-nm Sync/NoBL SRAMs. In the process of expansion, multiple SRAMs are used to increase the memory density in the system.

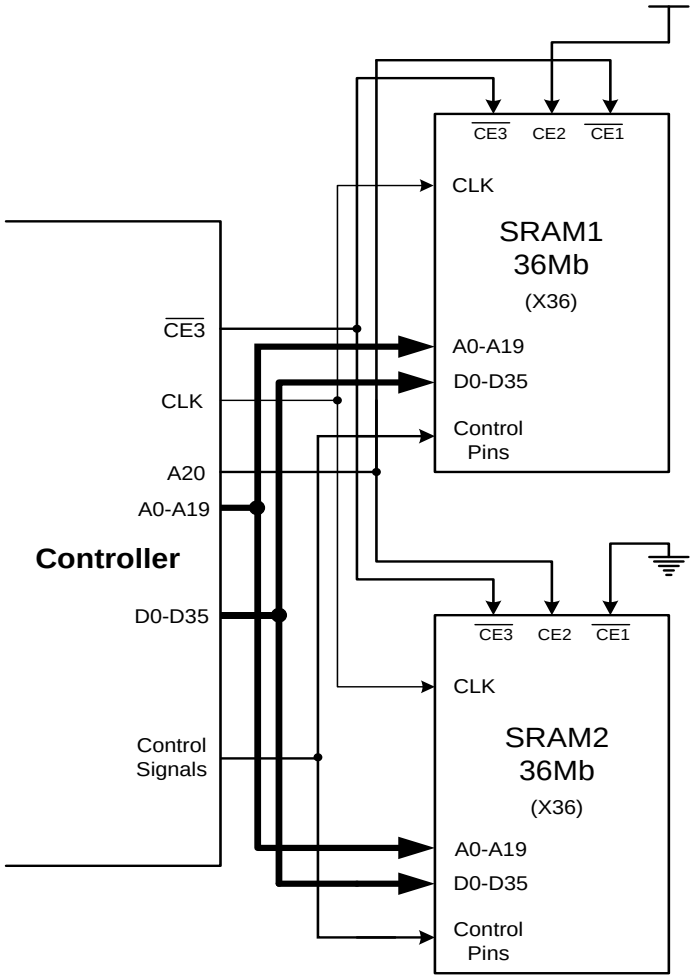
- **Width expansion:** This combines the data bus of each chip and use it as a single chip with a greater width. Both the chips are enabled, and the address line remains common. As shown in Figure 3, you use two 36-Mb SRAMs with an I/O width of 36 bits to expand the width up to 72 bits and increase the memory density to 72 Mb. The two SRAMs are combined such that the address lines (A0–A19), control lines ($\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$, $\overline{OE}$, $\overline{BWE}$, $\overline{GW}$), and chip enable lines ($\overline{CE1}$, $CE2$, and $\overline{CE3}$) remain common. Data lines D0–D35 are connected to the first SRAM, and data lines D36–D71 are connected to the second SRAM. During a read/write operation, the control lines enable both the SRAMs. Since the row address remains the same for both the SRAMs, you can concurrently access all 72 memory bit positions during any normal memory operation.

Figure 3. Width Expansion



- **Depth expansion:** In depth expansion, the number of rows that can be accessed by the processor/FPGA increases, but the I/O width remains the same. An extra address line from the controller side is used to activate the appropriate row from either of the SRAM chips. Chip Enable (CE) pins are driven selectively to access the desired SRAM. The common address (A0–A19), control ($\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$, $\overline{OE}$, $\overline{BWE}$, $\overline{GW}$), and data (D0–D35) lines are connected to each chip, as shown in Figure 4. The $\overline{CE3}$ pins of both SRAMs are driven by a common signal $\overline{CE3}$ from the controller. The $CE2$ pin of SRAM1 is connected HIGH, and the $\overline{CE1}$ pin of SRAM2 is grounded. The $\overline{CE1}$ pin of SRAM1 and the $CE2$ pin of SRAM2 are connected to address line A20. To access a row in SRAM1, the A20 pin is kept LOW, enabling the SRAM1 chip. To enable SRAM2, address line A20 is driven HIGH, which disables SRAM1 concurrently. Using two memories in this way doubles the total depth of the Sync/NoBL SRAM. Figure 4 illustrates the controller to memory pin connections for depth expansion.

Figure 4. Depth Expansion



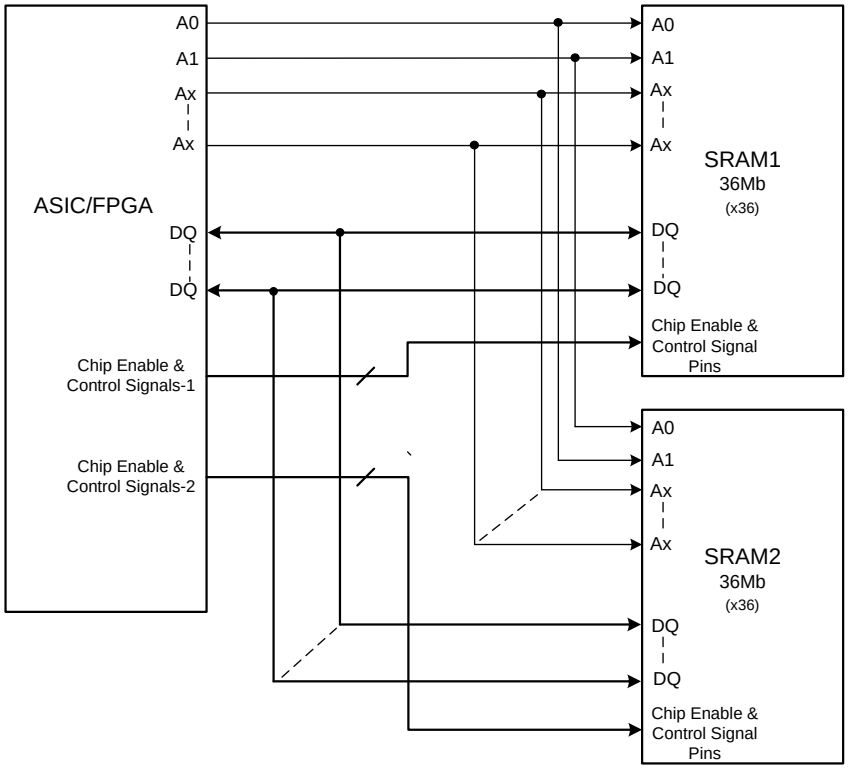
During width and depth expansion, ensure that an equal trace length for shared signal lines is maintained. They should also be impedance-matched through proper termination resistors.

5 Address Pin Assignments

When the address pins are assigned a particular bit location, read and write operations take place from the same location in memory. Each SRAM has a group of pins defined as addresses, another group as I/Os, and so forth.[9] Therefore, the exact address (A) pin numbers are not provided except for the A0 and A1 pins. In synchronous and NoBL SRAMs, the addresses A0 and A1 must be in order, as these bits load into a burst counter.

Consider an example where two identical SRAMs are connected to a single ASIC/FPGA. Assume that SRAM2 is being used to replicate the data that will be stored in SRAM1 and will be read later. The connection to the SRAM2 A0 and A1 pins is scrambled, as shown in Figure 5. The ASIC/FPGA writes to both the SRAMs and reads an individual SRAM by asserting corresponding chip enable and control signals.

Figure 5. ASIC/FPGA Connected to Two Identical 36-Mb Sync/NoBL SRAMs



If the ASIC/FPGA initiates a write sequence at the address location A0=0 A1=1 A2=0 …. Ax=1, then SRAM1 will write to internal address 1…..010, and SRAM2 will write to internal address 1…..001. If the ASIC/FPGA performs a read from the same address, A0=0 A1=1 A2=0 …. Ax=1, SRAM1 will read it from 1…..010, and SRAM2 will read it from 1…..001. Thus, the ASIC/FPGA will always receive the anticipated data for a given address regardless of the address labeling. So, you can connect the address pins on their side to any address pins on the SRAM. The only exception is that the A0 and A1 addresses must be in place for all the SRAMs, as these bits load into a burst counter.

The ASIC/FPGA will load the SRAM with the read/write address, and then the SRAM will use the internal 2-bit burst counter to generate the next three addresses. The location of A0 and A1 matters because during the read cycle, the ASIC/FPGA expects a certain sequence of data based on the addresses it assumes were generated by the internal burst counters of the SRAM during the write sequence. If A0 and A1 are jumbled, then the expected data may not be returned.

[9] Cypress follows the JEDEC SRAM pinout standards. The JEDEC standard does not stipulate that a particular pin should be assigned to a certain address in a setting where address differentiation does not make any functional difference.

For example, if the ASIC/FPGA starts a linear burst write with a start address of A0=1 and A1=0, and data of 100, 101, 102, and 103, then SRAM1 will start at address 01 and generate internal addresses in the order of 10, 11, and 00. On the other hand, SRAM2 will have a start address of 10 and generate internal addresses of 11, 00, and 01. When the ASIC/FPGA does a burst read starting at 11, the expected data will be 102, 103, 100, and 101. SRAM1 will start at the internal address ending in 11 and produce data of 102, 103, 100, and then 101. SRAM2 will also start at 11 but will produce data of 101, 102, 103, and finally 100. This may result in erroneous data being read by the ASIC/FPGA when it is accessing SRAM2. Therefore, during a synchronous burst, the A0 and A1 pin connections must match between devices, but the remaining address pins need not necessarily match.

6 Summary

The 65-nm Sync/NoBL family of SRAMs provides the ability to achieve improved soft-error immunity with the introduction of ECC. Compared with the 90-nm technology, it features less power consumption, lower input and output capacitances, and lower junction temperature ratings. Furthermore, the 65-nm devices are form-, fit-, and function-compatible with the 90-nm technology parts.

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*B	4794123	DEVM	06/17/2015	Updated Comparison of 65-nm and 90-nm Sync/NoBL SRAM Devices: Updated Table 1 (Updated with 18M Sync/NoBL SRAM values). Updated Power Consumption and Junction Temperature Calculation: Updated Power Dissipation (P_d): Updated Table 2 (Updated with 18M Sync/NoBL SRAM values). Updated Junction Temperature (T_J): Updated Table 3 (Updated with 18M Sync/NoBL SRAM values).
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