AN94074

Design Best Practices with CY27410 Four-PLL Spread-Spectrum Clock Generator

Author: Amitava Banerjee, Hiromu Takehara and Pawan Kumar

Associated Part Family: CY27410

Related Application Notes: AN94024, AN93892

AN94074 provides basic design guidelines of the CY27410 four-PLL Spread-Spectrum Clock Generator for the best performance in end systems. You should use this best practices guidance in conjunction with all other design, manufacturing, and software guidelines applicable to CY27410.

1 Introduction

CY27410 is a four-PLL spread-spectrum clock generator that generates eight differential and four single ended clock outputs up to 700 MHz with sub-picosecond jitter. This document outlines the architecture of CY27410 and provides design guidelines for best performance in end systems. This document also contains a case study that illustrates how CY27410 can be used to meet a sample clocking requirement. To create your configuration, use the Cypress proprietary tool (ClockWizard 2.1) and to evaluate the configuration use CY3679 Evaluation Kit.

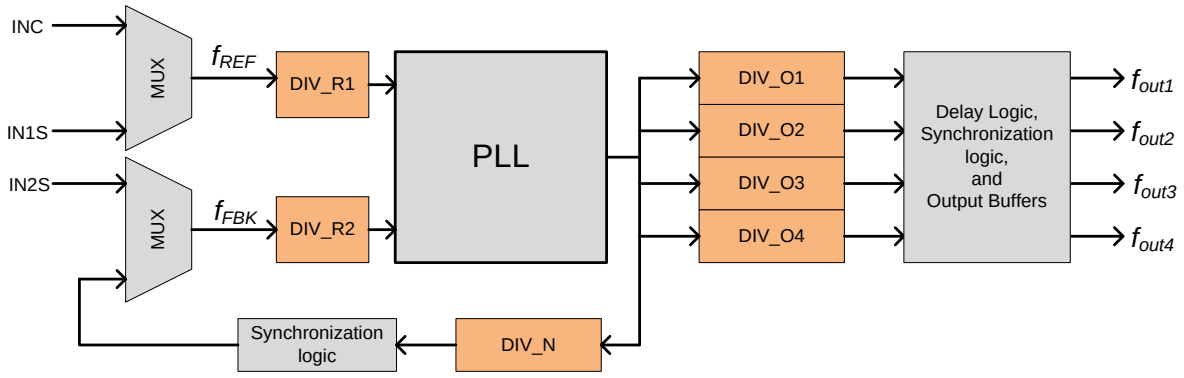
1.1 General Rule for Configuration

The basic architecture of CY27410 PLL is shown in Figure 1. This device provides clock synthesis for PLL output ports using a scaling factor. The basic formula for determining the final output frequency is:

$$f_{OUT} = f_{REF} \times \frac{(DIV\_N)}{(DIV\_R) \times (DIV\_O)}$$

- f_{REF} is the input reference frequency,
- *DIV_R* (*DIV_R1* and *DIV_R2*) is the division factor of the input frequency reference. These dividers are called pre-scale dividers.
- *DIV_N* is the fractional N division factor.
- *DIV_O* (*DIV-O1, DIV-O2, DIV-O3,* and *DIV-O4*) is the post division factor before outputs.

Figure 1. CY27410 PLL Simplified Architecture Block Diagram



The frequency range of operation of the PLL is 2.4 GHz to 3 GHz. The input clock (f_{REF}) is divided by a prescale counter (*DIV_R1* or *DIV_R2*) to produce the input reference clock to the PLL. The count value of *DIV_R* counter ranges from 1 to 28. The post-division factor *DIV_O* is an even number and its values range from 4 to 1020. The control loop drives the PLL to match the required f_{OUT} as per the previous equation.

2 Design Guidelines

2.1 VCO Spacing in Frequency

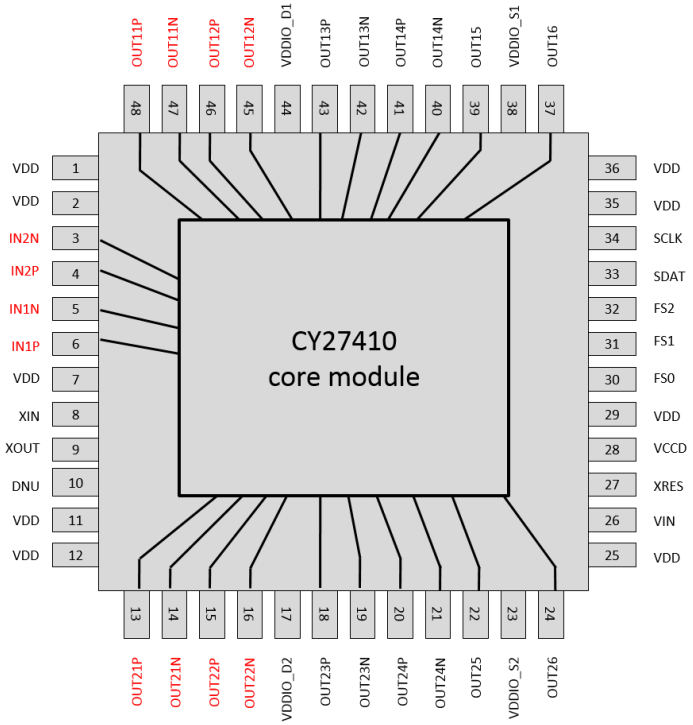
In an advanced design, when more than one PLL is active, frequency planning must provide a minimum frequency spacing between any two VCOs to avoid jitter. These VCO frequencies should have a difference of at least 50 MHz between each other. Otherwise, crosstalk may be induced due the interference between PLL blocks running at the same VCO frequencies. ClockWizard 2.1 does not take values of VCO frequencies that violate this guideline.[1].

2.2 Clock Signal Routing

Near to the input reference signal path (signal routing of IN2N, IN2P, IN1N, and IN1P pins), all outputs should be assigned as differential standards like LVPECL, LVDS, CML, or HCSL. If they are assigned as LVCMOS standard, the large voltage swing will induce more cross-talk into the input frequency reference. The induced crosstalk would affect the performance of PLL, and output clocks may become noisy.

Therefore, the outputs OUT11, OUT12, OUT21, and OUT22 (signal pins marked in orange in Figure 2) are recommended to be assigned as differential output standards as they are closer to the input signal lines (IN2N, IN2P, IN1N, and IN1P). If any of these lines is configured as single-ended CMOS standard, and having 0-V to 3.3-V swing, there is a possibility of jitter on the adjacent differential lines as well. LVCMOS standard outputs are recommended to be located far from these input reference clock lines.

Figure 2. Pinout Diagram of CY27410 Showing High-Frequency Input and Output Signal Lines



[1] Contact Cypress Tech Support if your design requirements need VCOs with frequency spacing less than 50 MHz.

CY27410 has four I/O supply domains, VDDIO_D1 (OUT11 to OUT14), VDDIO_S1 (OUT15, OUT16), VDDIO_D2 (-OUT21 to OUT24) and VDDIO_S2 (OUT25, OUT26). To have reduced crosstalk and better jitter performance, it is recommended to derive all the outputs of a particular VDDIO domain from one PLL only. For example, derive OUT11 to OUT 14 outputs from PLL1; OUT15, OUT 16 outputs from PLL2; OUT21 to OUT 24 from PLL3; and OUT25, OUT 26 from PLL4.

Figure 2 shows the pinout diagram of CY27410 and its high-frequency input and output lines. Crosstalk between input and output lines is a major contributor to the PLL jitter. This crosstalk may arise from the routing inside the IC and cannot be changed. In the system level, the PCB layout requires special attention of shielding between input and output lines.

2.3 Supply Decoupling

Because the clock IC's I/O-supply port (VDDIO) may introduce high-frequency noise into the overall power supply network. you should add an inductor (a ferrite bead) besides decoupling capacitor as shown in the Figure 3. A typical value for decoupling capacitors may be C1 =1 µF, C2 = 1 µF and C3 = 0.1 µF. C3 should be placed as close to the IC I/O supply as possible and C2 as the next closest component. C1 is placed as the decoupling capacitor for power supply net. See Table 1 for typical values and part numbers.

Figure 3. Supply Decoupling Circuit

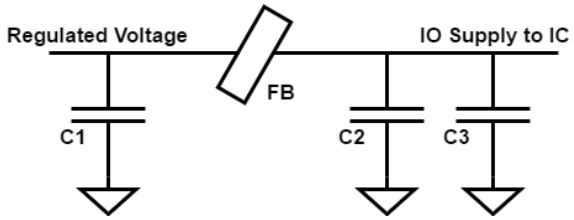


Table 1. Typical Values for components

Device	Value	Typical MPN
FB	FERRITE CHIP 220 OHM 450MA 0603	BLM18BB221SN1D
C1, C2	CAP CER 1UF 25V 10% X5R 0603	TMK107BJ105KA-T
C3	CAP CER 0.1UF 50V 10% X7R 1206	C1206C104K5RAC7867

These components have been used in Cypress **EVK CY3679,** which is Cypress's evaluation platform for CY27410. Other than this, all power pins must be decoupled with capacitors and individual ferrite beads placed as close to the power pins as possible on the PCB.

2.4 Example: Designing Cypress Clocks for Multiple Output Frequencies

The following example shows a case study that illustrates how CY27410 can be used to meet a sample clocking requirement such as the following:.

1. Three PCIe Gen 2.0 spread-spectrum (SS) clock (Each 100-MHz frequency, phase-aligned and 0.5% down spread)
2. Five dedicated LVCMOS clocks for four different applications:
   - One 33.33-MHz (0.5% down-spread) clock for ASIC
   - One 25.00-MHz clock for Ethernet
   - One 24.576-MHz clock for modem
   - One 20.00-MHz clock for CPU
   - One 64.00-MHz (0.5% Center Spread) clock for ASIC

The first step in designing this system with CY27410 is frequency planning. This frequency planning for the four PLLs can be done in the following way:

3. The 33.33-MHz SS and 100.00-MHz SS are related but the 64-MHz SS is UNRELATED; therefore, two PLLs are required to generate 33.33-MHz, 64-MHz, and 100-MHz clocks.

   Note: As the range of PLL frequency is 2400 MHz to 3000 MHz, and LCM of 64 and 100 is 1600, there is no solution to set the frequency of one particular PLL that can generate both the clock outputs. Therefore, 64-MHz and 100-MHz clocks are called UNRELATED.

4. As 24.576 MHz is UNRELATED to other clocks, either you can choose the 24.576-MHz clock as a reference input, or it is required to be generated from one PLL.
5. 20.00-MHz and 25.00-MHz clocks can be generated from one PLL.
6. One 64.00-MHz (0.5% center-spread) clock for ASIC.

Therefore, the PLL assignment would be as follows:

1. Use 24.576 MHz as the reference clock.
2. Four spread-spectrum clocks (three 100-MHz PCIe clocks and one 33.33-MHz ASIC clock) can be derived from PLL1.
3. One 25-MHz Ethernet clock and one 20-MHz CPU clock can be generated from PLL2.
4. The 24.576-MHz modem clock can be generated from PLL3.
5. The 64.00-MHz (0.5% center-spread) clock can be generated from PLL4.

3 Conclusion

This document presents design recommendations for CY27410 to obtain its best performance. Guidelines presented in this document will assist system designers to plan for proper PLL frequency and output settings. However, it is not always possible to configure all the internal and output parameters as per the typical programming guidelines. Rather, it depends on how complex the system design is, how many interfacing devices are clocked by CY27410, the frequencies of operation, output buffer standards, voltage requirements, jitter specifications etc.

In summary, designers must be aware of the best possible design configuration of CY27410. With this basic knowledge, designers can approach for designing more critical systems where tradeoff between different applications specifications is possible.

About the Authors

Name:	Amitava Banerjee, Hiromu Takehara and Pawan Kumar
Title:	Applications Engineer Staff
Background:	Amitava Banerjee has Master’s degree in Electrical Engineering from IIT Kharagpur, India.
	Hiromu Takehara is system-level expert working in Cypress Semiconductor for 14 years in Timing Solution Business Unit.
	Pawan Kumar has a Master’s in Electrical Engineering from IIT Delhi, India.

Document History

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**	4661163	TAVA	02/16/2015	New Application Note.
*A	5302085	TAVA	06/09/2016	In the section Design Guidelines, the text PLL frequency is changed to VCO frequency Updated template
*B	5698212	PAWK	05/05/2017	Updated Section 2.3 Updated template

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