AN94024

Getting Started with CY27410/30: 4-PLL Spread-Spectrum Clock Generator

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Associated Part Family: CY27410

Software Version: N/A

Related Application Notes: AN93892, AN94074

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Cypress's latest-generation high-performance clock generator device – CY27410 - is a 4-PLL, 12-output PCIe 3.0-compliant device that provides a host of value-added features. This application note describes how to configure the device in both clock generator and buffer modes with details on input/output standards, external design considerations, reference selection including crystal, and the internal memory structure.

Contents

Overview

CY27410 is a 4-PLL spread-spectrum clock generator targeted at consumer, industrial, and networking applications. CY27410 has two inputs and twelve outputs, frequencies up to 700 MHz with a low RMS phase jitter of 1 ps max. CY27410 supports value-added features such as voltage-controlled crystal oscillator (VCXO), frequency select, and zero/nonzero delay buffer (ZDB/NZDB) modes. The part is designed to support reference clocks for key interface standards such as PCI Express (PCIe) 1.0/2.0/3.0, USB 2.0/3.0 and 10-Gigabit Ethernet (GbE).

This application note describes how to configure the device for different applications and device mode configurations. In addition, the I^2C interface of the device, its signaling levels, and external design considerations are explained in the application note.

CY27410 has three major modes of operation: clock generator (CLKGEN) mode, zero-delay buffer (ZDB) mode, and nonzero-delay (NZDB) buffer. In the Clock Generator mode, the device generates multiple clock frequencies using an internal PLL from an external reference clock or crystal. In the ZDB mode, the device generates the same clock frequency as input clock, or integer-multiple or integer-divide frequencies with little delay with respect to the input. In the NZDB mode, the device bypasses the PLL and buffers the input signal to outputs with support of additional dividers.

CY27410 also provides value-added features such as phase delay of outputs, voltage controller frequency synthesis (VCFS), spread spectrum, frequency select, and glitch-free outputs.

Key Specifications

- Input frequencies
  - Crystal input : 8 MHz to 48 MHz
  - Reference clock : 8 MHz to 250 MHz LVCMOS
  - Reference clock : 8 MHz to 700 MHz differential
- Output frequencies
  - LVDS, LVPECL, host-clock signal level (HCSL), current mode logic ((CML) 25 – 375 MHz, 400 – 500 MHz, 600 – 700 MHz))
  - LVCMOS (3 MHz to 250 MHz)
  - 1 kHz to 8 MHz for one LVCMOS output
- RMS phase jitter < 1 ps max at 12-kHz to 20-MHz Offset
- PCIe 1.0/2.0/3.0, SATA 2.0, USB 2.0/3.0, 1/10GbE
- Maximum 12 outputs split in two banks of 6 outputs each.
  - Up to 8 differential output pairs (HCSL, LVPECL, CML, or LVDS)
  - Up to 12 LVCMOS outputs
- Up to 75-ps skew for differential outputs within a bank
- Four fractional N-type PLL with
  - VCXO (+/-120 ppm)
  - Spread-spectrum capability (Logic SS and Lexmark profile 0.1 to 5% in 0.1% steps, down or center-spread)
- Supply voltage: 1.8 V, 2.5 V and 3.3 V
- ZDB/NZDB configurations
- I^2C-configurable with On-board programming
- Industrial and Automotive grade devices
- 48-pin QFN package.

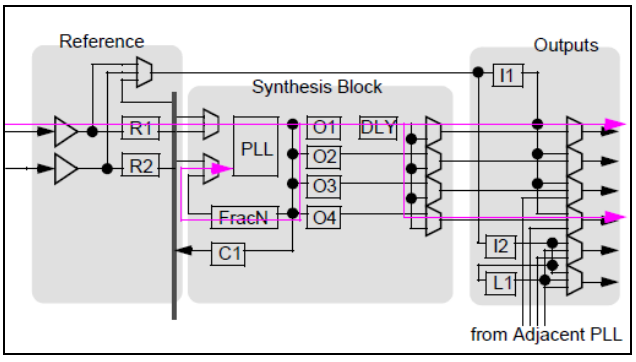
Modes of Operation

CY27410 has CLKGEN, ZDB, and NZDB modes. It can also be configured in a combination of CLKGEN and ZDB, CLKGEN and NZDB, and ZDB and NZDB modes.

CLKGEN Mode

Figure 1 shows the PLL block diagram in CLKGEN mode. In this mode, CY27410 generates multiple clock frequencies from one reference crystal or clock input. Up to four *unrelated* clock frequencies can be generated in this mode from the four PLLs of the device. Each PLL has again four independent dividers, so you may generate up to four different related frequencies from a PLL. Two frequencies are said to be *unrelated* if there is no common multiple for the two clock frequencies within the PLL VCO range of 2.4 GHz to 3.0 GHz.

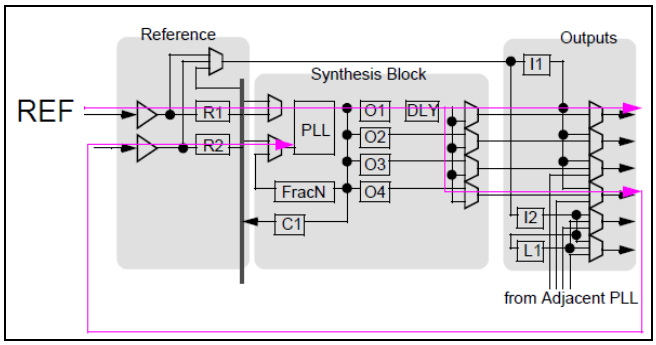
Figure 1: Clock Generator Configuration



ZDB Mode

In ZDB mode, the device acts as a zero-propagation-delay device from input to output as shown in Figure 2. In order to achieve this functionality, CY27410 requires a feedback clock from one of the outputs for tracking its phase.

Figure 2. ZDB Configuration



Input frequency range (Single Ended): 8 MHz to 250 MHz

Input frequency range (Differential): 8 MHz to 300 MHz

Typical ZDB input/output delay is less than 250 ps. CY27410 can also provide the Frequency Multiplying/ Dividing ZDB configuration by modifying R1 or R2 divider appropriately.

When R1 = R2, the output frequency is the same as IN1, when R1 value is half of R2, the output will be twice of IN1. CY27410 provides R1 and R2 value of 1, 2, 4, or 8, so you can configure CY27410 as ZDB with the frequency multiplying/dividing function.

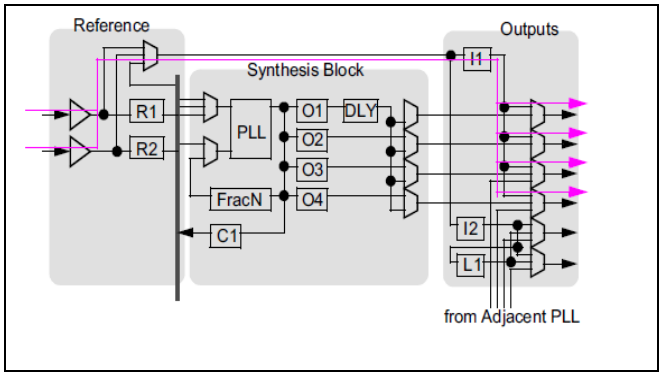
NZDB Mode

In NZDB mode, the device acts as simple buffering of the input signal to outputs, also known as fan-out buffer. In the NZDB mode as shown in Figure 3, the PLL is bypassed making the device act as a fanout buffer.

Input frequency range (Single-Ended): 8 MHz to 250 MHz

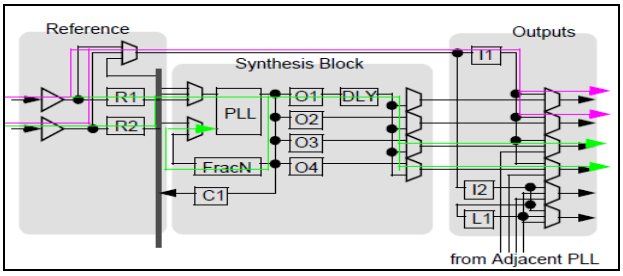
Input frequency range (Differential): 8 MHz to 700 MHz

Figure 3. NZDB Configuration



CY27410 can also be configured in combination of CLKGEN and ZDB, CLKGEN and NZDB, and ZDB and NZDB modes. This offers unprecedented flexibility to the customer. Figure 4 shows how the CLKGEN and NZDB mode can be used in CY27410.

Figure 4: CLKGEN AND NZDB Configuration



Input Subsystem

The device can accept both crystal and reference input. The crystal input pins are XIN and XOUT, which are connected to a crystal oscillator block to generate the required clock to be fed into the VCO. The differential tuning-capacitor range supported is 8 pF to 12 pF.

The device also support four reference input pins (IN1P, IN1N, IN2P, and IN2N). These pins are designed to receive a reference input which can either be single-ended or differential clock.

IN1 is multiplexed with IN1 (clock signal: single-ended or differential) or crystal oscillator.

IN2 can be configured as differential or single-ended.

See Table 1 for input frequency specifications.

Table 1. Input Frequency Specifications

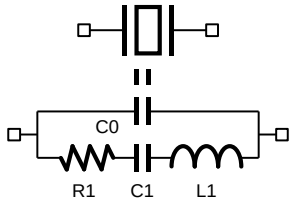
Input Frequency	Min.	Max.
Crystal	8 MHz	48 MHz
IN1,2-SE	8 MHz	250 MHz
IN1,2-DE	8 MHz	700 MHz

Note CY27410 incorporates a narrow-bandwidth PLL (VCO). Therefore, you cannot use the reference clock that has large distortion/drift; for example, spread-spectrum clock (typically 0.5 to 1.0% modulation). Switching from one frequency to another (different) frequency cannot be used as the reference clock either.

Choosing the Crystal

CY27410 supports a crystal input between 8 MHz and 48 MHz. The equivalent crystal circuit with components is shown in Figure 5.

Figure 5. Equivalent Crystal Circuit with L-R-C Components



C0 = Crystal Shunt Capacitance

C1 = Crystal Motional Capacitance

R1 = Equivalent series Resistance

For CY27410, we recommend a crystal with parameters as shown in the Table 2.

Table 2. Equivalent Resistance and Shunt Capacitance for Values for Crystal

Nominal Frequency (in MHz)	R1 (MAX)	CL (pF)
8 to 12	150 ohms	8 to12
12 to 20	70 ohms	8 to12
20 to 48	50 ohms	8 to12

CL for All ranges	Associated Max C0 (pF)
8	2
9	2
10	2
12	3

CY27410 Crystal oscillator circuit implements a low-power (up to 100 micro watt drive level) and high-precision buffer so that the crystal selection is important. Layout designers are advised to keep the trace length between CY27410 and crystal as short as possible, and not to route any active signal around the trace and crystal.

Input Reference Block

This section describes how to interface the input reference signals to CY27410 and design considerations for input signals.

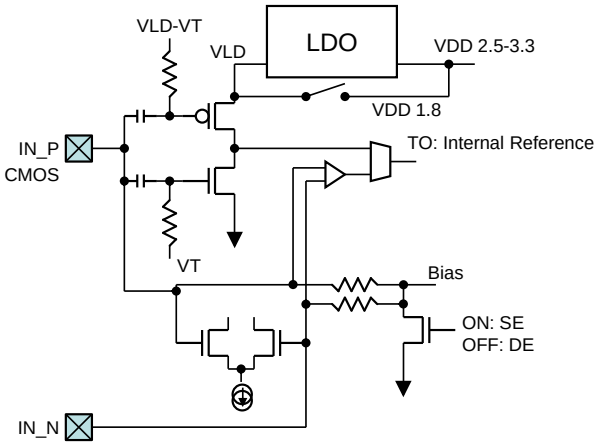
Input Frequency Tolerance

The CY27410 design incorporates a narrow-bandwidth, high-performance, low-noise PLL. The device cannot track input clock tolerance more than 300 ppm. As a result, the ceramic resonator that would vary in order of 1000s of ppm cannot be used as a reference crystal. Also, spread-spectrum clocks cannot be used as inputs to CY27410.

Input Circuitry

Figure 6 shows the input structure for the CY27410 device.

Figure 6. Input Structure for CY27410



When the single-ended (LVCMOS) configuration is selected, both IN_P and IN_N pins are pulled down to GND, and the AC coupled input signal is fed to P-N- transistors shown above. Both P- and N- transistors are then biased as fixed level (VLD-VT and VT). This voltage difference provides enough margins for noisy inputs and act with small input amplitude defined in the datasheet, such as 0.8 Vp-p for clipped sine wave.

Input P-N- transistors are high-voltage (5 V) tolerant. You may apply the input voltage more than the VDD, even though VDD core supply is 1.8 V.

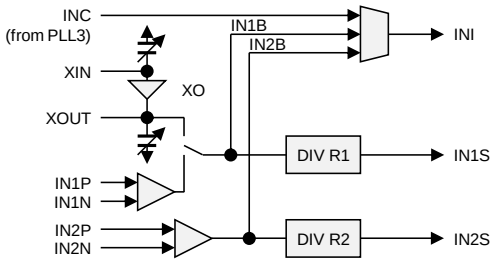
When DE (differential) input is selected, both IN_P and IN_N are biased to certain level (1.2 V typical).

Input Reference System

Figure 7 shows the input reference system of CY27410. IN1 and XO signal will be multiplexed and fed to internal reference as IN1B. IN2 can be used for feedback input in ZDB mode or can be used as another input reference clock for NZDB mode.

The output from DIV-C of PLL3 is the special-purpose input that will be used, if you need more than four copies of the same clocks.

Figure 7. Input Reference System of CY27410

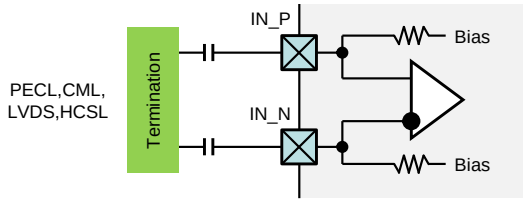


Differential Input Signals

The CY27410 supports various differential I/O standards like LVPECL, CML, LVDS and HCSL. These I/O standards have different common mode voltages. The common-mode voltage (VCM) for various interface standards are VDD - 1.2 V (LVPECL), VDD - 0.2 V (CML), 1.2 V (LVDS), and 0.4 V (HCSL).

To maintain multiple differential signals, inputs must be AC-coupled (100-pF capacitors in series), and termination resistors should be added outside if needed. Figure 8 illustrates this design recommendation.

Figure 8. Sample Design Recommendation for Differential I/O Standards



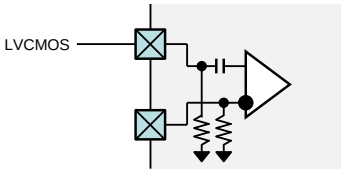
As described in the previous section, CY27410 accepts multiple differential signals using AC-coupled inputs. The input swing amplitude should be more than 300 mV pp for the signal to meet the VIH/VIL specifications.

LVCMOS Input Signal

Figure 9 shows a simplified LVCMOS input buffer structure of CY27410. The CMOS input signal is AC-coupled inside the device. Cypress recommends the minimum peak-to-peak amplitude to be 300 mV. Both the inputs are pulled down internally in LVCMOS configuration, so unused pins can be left floating for CMOS input.

The input circuit of CY27410 uses overvoltage-tolerant cells. In case an input voltage is applied higher than VDD, it will not cause any reliability issues. Multiple input voltage levels can be interfaced to CY27410. Any combination of different voltages may be used (VDD core=1.8 V, 2.5 V, or 3.3 V, and input voltage level=1.8 V, 2.5 V, or 3.3 V)

Figure 9. Simplified LVCMOS Input Buffer Structure



Clipped Sine Wave Signal

A typical TCXO output signal is a clipped sine-wave signal. CY27410 treats this input signal in the same manner as LVCMOS. The device guarantees only functional operation when using clipped sine-wave inputs. The datasheet parameters are not guaranteed for clipped sine-wave inputs.

Do not use a series capacitor between TCXO and IN1_P if the CY27410 input mode is configured as LVCMOS (typically recommended by TCXO vendors). Use a series capacitor if the input setting is configured as differential.

Figure 10. Connection to the TCXO module

The typical TCXO output signal is shown in figure 11. The typical peak-to-peak voltage (V_{P-P}) is 0.8 V-1.0 V.

Figure 11. Typical TCXO Output Signal

Output Subsystem

CY27410 consists of two banks of outputs. Each bank consists of six outputs with OUT11–OUT14 and OUT21–OUT24 supporting both differential and single-ended outputs and OUT15–OUT16 and OUT25–OUT26 supporting only single-ended outputs. Each output is fed from a PLL through a divider and then to a MUX, which helps in selecting the source for the output, as shown in Figure 12 and Figure 13.

Figure 12. Output Bank 1

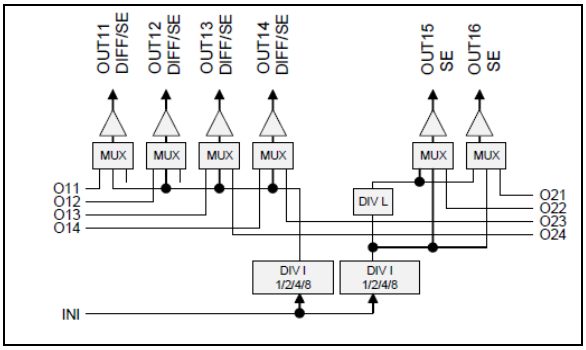
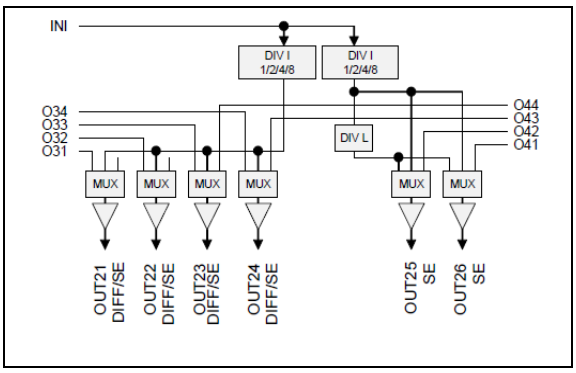


Figure 13. Output Bank 2



Output Termination

CY27410 supports LVCMOS, LVPECL, CML, LVDS, and HCSL standards for output. This section describes the recommended termination circuits for the outputs.

HCSL Output Standard

HCSL interface standard is a differential I/O standard and is defined in PCIe SIG standard. Figure 14 shows the typical interface termination, while Table 3 summarizes the recommended trace length parameters and termination resistors.

Figure 14. Typical HSCL Interface Termination

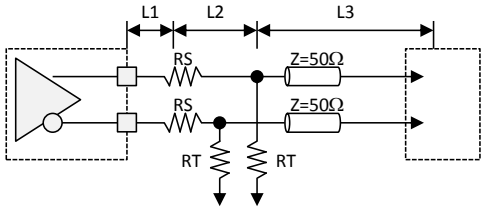


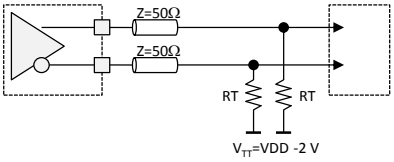
Table 3. HSCL Interface Parameters

Parameter	Value	Unit
L1 length	0.5 (max)	Inch
L2 length	0.2 (max)	Inch
L3 length	10	Inch
RS	33 (3.3 V or 2.5 V supply)	Ohm
RS	20 (1.8 V supply)	Ohm
RT	49.9	Ohm

LVPECL Output Standard

LVPECL standard signaling level is a differential I/O standard and is defined in JEDEC JESD8-2 (Emitter Coupled Logic). Figure 15 shows the typical termination scheme for this standard.

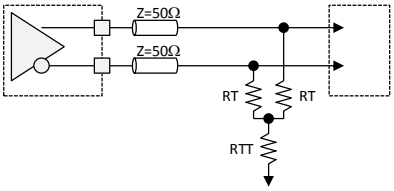
Figure 15. LVPECL Output Termination Scheme



In the above scheme, RT= 50 Ω

Since VDD – 2 V (1.3 V for 3.3-V operation) may be difficult to generate, you may use the Y-Termination instead (see Figure 16).

Figure 16. Y-Termination Scheme

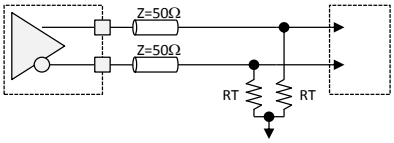


In the above scheme, RT=50Ω derives the RTT value:

$$R_{TT} = \left[\frac{1}{((V_{OH} + V_{OL}) + (V_{DD} - 2)) - 2}\right] \times Z_O$$

Figure 17 shows a simple termination scheme that is sometimes employed when there is a very short trace length, but is not always recommended.

Figure 17. Simple LVPECL Termination Scheme



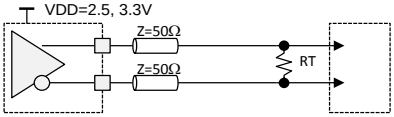
In the above scheme, RT=150Ω

Note VDD=1.8 V is not applicable for LVPECL standard.

LVDS Output Standard

LVDS signaling standard is also a differential I/O standard and is defined by TIA/EIA-644-A (JEDEC standard) and its typical termination is shown in Figure 18.

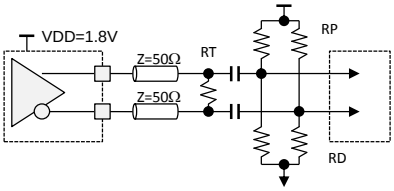
Figure 18. LVDS Signaling Termination (2.5 V, 3.3 V)



Outputs (OUTxP and OUTxN) should be connected together through a 100-Ω resistor (RT=100 Ω).

For VDD=1.8 V operation, you require AC coupling (100-nF series capacitor) and bias at the destination using termination resistors. Figure 19 shows such a termination scheme.

Figure 19. LVDS Signaling Termination (1.8 V)



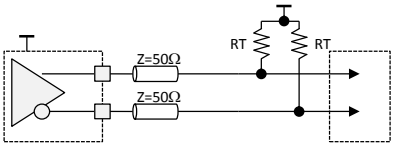
In the above scheme, RT=100 Ω.

RP and RD must be chosen to meet VCM (common-mode voltage) of 1.2 V (Typical).

CML Output Standard

CML interface is a differential I/O standard and is defined in IEEE 802.3 spec. Figure 20 shows the termination scheme of this standard.

Figure 20. CML Signaling Termination

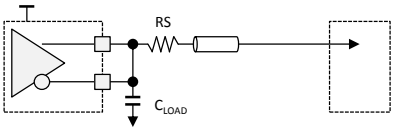


In the above figure, RT=50Ω and should be terminated to VDD.

Using Differential Output as LVCMOS

The CY27410 device is highly flexible, enabling the use of differential outputs in single-ended mode. Figure 21 illustrates the same: OUTxP and OUTxN should be tied together for LVCMOS output.

Figure 21. Using Differential Output as LVCMOS standard



RS should be chosen for impedance matching appropriately.

C_{LOAD} represents the capacitive load of entire circuits.

Additional Features

CY27410 supports additional features like early/late output phase synchronization circuit, voltage controller frequency shift (VCFS), spread spectrum clock generator (SSCG) and cascading PLLs.

Phase Delay of Outputs

Outputs of CY27410 can be configured to introduce a certain delay in the outputs. This feature can be used in both CLOCKGEN and ZDB mode. This feature is provided as some ASIC and SoCs require fixed delay between 2 clocks.

The following equation derives one period unit for delay circuit:

$$t_{DL} = \frac{2}{f_{VCO}}$$

Wherein t_{DL}=1 delay unit

Example: If f_{VCO}=3.0 GHz, t_{DL} = 0.666 ns

Figure 22 shows an example of a conceptual delay circuit.

Figure 22. Phase Delay Circuit Example

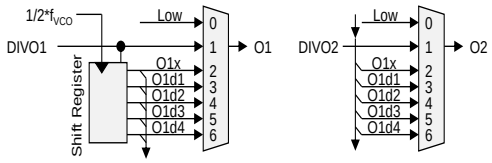
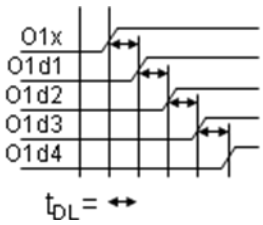


Figure 23. Phase Delay Timing Diagram

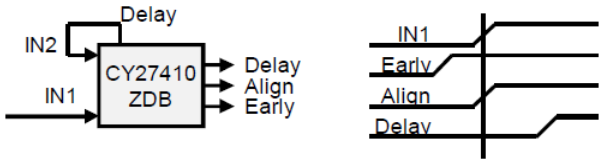


CY27410 supports a maximum of four units (t_{DL}) of delay(s)

Even when you choose the same DIVO (Ox above) value for O1 and O2 (O3, O4), it does not guarantee phase-aligned clocks between outputs. To get phase-aligned outputs, use O1x for other output(s).

Most of the ZDB outputs should use O1x for all outputs. However, if you intentionally choose delayed output to provide feedback, you can get the Early (or Late) phase clocks described below.

Figure 24. Alignment of Delayed Outputs of CY27410



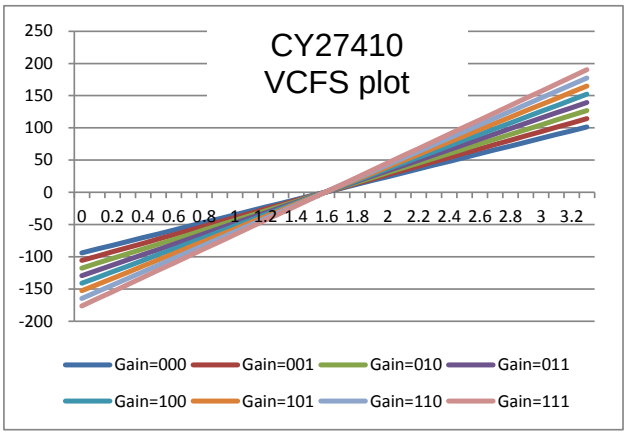
In the example shown in figure 24, one delayed output (O1d1) is fed back to IN2, while early clock selected is O1x, and delayed output selected is O1d3.

In CLKGEN mode, you may use this delay circuit to generate N (x t_{DL}) delayed phase clock(s). For applications that need to adjust some skew or need fixed delay phase, you may use this function. For example, if trace characteristics are such that the propagation delay is 175 ps/inch, then a four inch-delay will be 700 ps.

Voltage-Controlled Frequency Shift (VCFS)

CY27410 mimics the VCXO feature found in crystal oscillators with VCFS. The device modulates the PLL (VCO) frequency up to 120 ppm. The modulation is completely programmable. Please see Figure 26 for the VCFS shift profile.

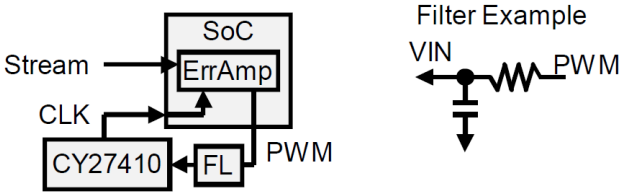
Figure 25. VCFS Shift Profile



VCFS in Applications

For some applications, the output clock frequency should track incoming data stream by using analog feedback. The CY27410 device acts as a part of the large phase lock loop shown in Figure 26. The ASIC or SoC tracks the incoming stream, calculates the error, and generates the PWM signal (typically), following which the error information is fed back to the local clock generator (CY27410) for frequency tuning.

Figure 26. VCFS Example



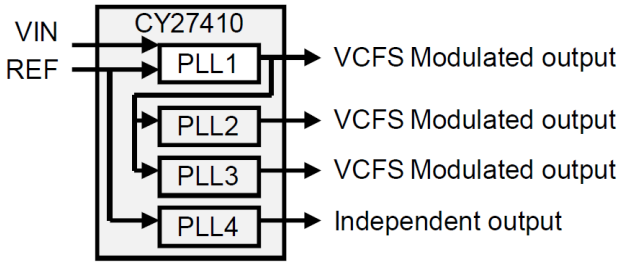
The VCFS function modifies the PLL frequency, so the frequency pulling is not dependent on the crystal characteristic, temperature, voltage, or device process.

The VCFS modulation profile is linear and accurate and you may use clock reference as well.

Cascading PLLs

With CY27410, you can make the output of one PLL and provide it as an input to another PLL. This feature is called PLL cascading. This feature can be used to generate very precise frequencies using multiple dividers from two PLLs. It can also take the VCFS modulated output from one PLL and feed it to other PLLs, thus generating multiple frequencies that track the change in the frequency. Figure 27 shows PLL1 configured in VCFS mode, its output cascaded to PLL2 and PLL3, but PLL4 will run as the fixed (un-modulated) frequency generation.

Figure 27. Cascading PLLs

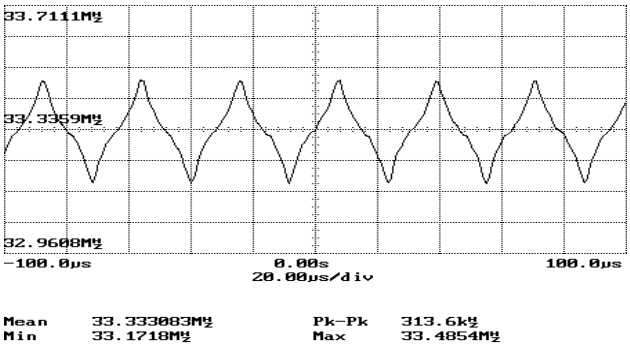


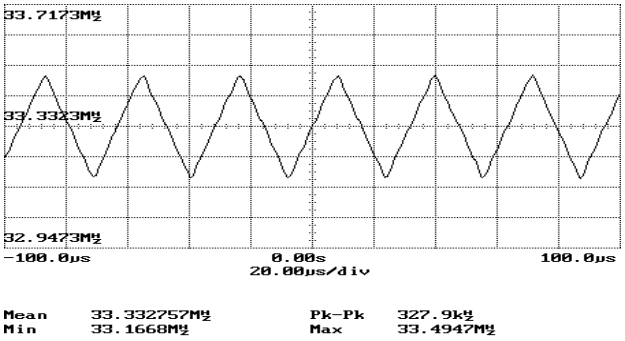
SSCG (Spread-Spectrum Clock Generator)

CY27410'S spread-spectrum feature helps overcome EMI/EMC concerns. The device supports both linear and nonlinear spread profiles, and by using the patented Lexmark profile as the nonlinear profile, offers the best peak EMI reduction in the industry.

Figure 28 shows the scope sot for the Modulation Domain Analyzer (time is plotted on the X-axis, while frequency is shown on the Y-axis).

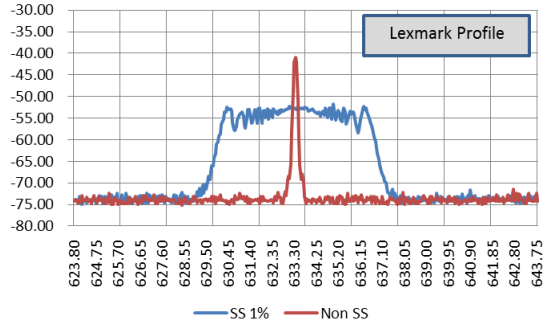
Figure 28. Spread Spectrum Clock Generator Profile

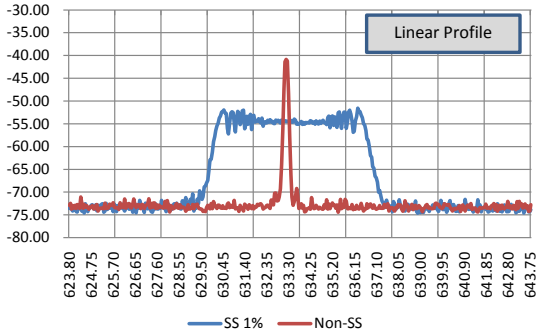




The spectrum is flat for nonlinear profiles, and raised at the edges for linear profiles. In Figure 29, the nonspread-spectrum profile is shown in red, while the modulated nonlinear (Lexmark) and linear modulation spectrums, ~10 dB peak reduction at 633 MHz are shown in blue.

Figure 29. Spread-Spectrum Profiles Supported by CY27410



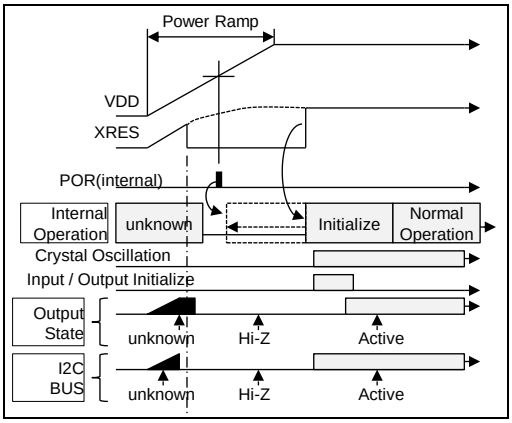


Power-Up Sequence

CY27410 has a CPU inside. While the supply (VDD) is ramping, the CPU initializes its internal settings, input configuration, output standard, output driver setting, etc.

Before CPU startup, all inputs and outputs are in an unknown state. Figure 30 shows the start-up sequence.

Figure 30: Start-Up Sequence

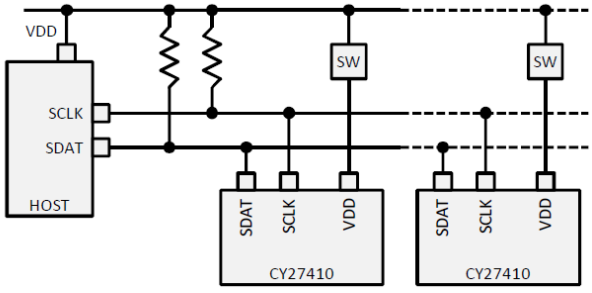


Power Supply Ramp

CY27410 requires a timing sequence for power ramp (please see CY27410 datasheet). If your system cannot meet this specification, provide the XRES (active LOW) signal to ensure startup.

While XRES is asserted, CY27410 enters low-power mode; outputs and the I²C bus signals are in a high impedance (HI-Z) state until initialization is complete after XRES is de-asserted. Figure 31 shows the considerations for bus signals during power supply ramp.

Figure 31: I²C Bus Signal Consideration



In this section, the I²C behavior during power ramp is discussed. Further details about the I²C interface are discussed in the section “Programming CY27410”.

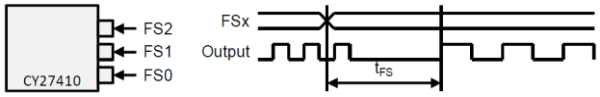
If you have a power supply switching while VDD is approximately 0.7 V to 0.9 V, CY27410 may pull the SCK signal LOW; therefore the I²C bus transaction may get affected by this behavior. You should pay close attention to this when you turn the CY27410 power supply ON or OFF.

Frequency Select (FS)

CY27410 supports up to eight user profiles that contain individual configurations. For FS pin transitions, CY27410 has two timing specifications – fast switching and slow switching.

Fast switching is applicable for the output ON/OFF, output-divider value change, and output MUX setting change. Slow switching is applicable for changes to the PLL parameter (including PLL ON/OFF). As the name implies, the output will change fast in fast switching and slow for slow switching. For each case, the output will be turned off and on without any glitch. See Figure 32 that shows the timing relationship between FS and the output clock. You can refer to the device datasheet for further details.

Figure 32: Frequency Select Operation



Power Ramp Considerations

CY27410 contains an internal CPU and requires reliable POR (Power-on-Reset) for proper operation. The device requires XRES signal when the power ramp is greater than the specification.

Multiple Power Supply Domains

CY27410 has six different types of power supply pins - VDD, VDDIO1D, VDDIO1S, VDDIO2D, VDDIO2S, and VCCD. VDD is the core power supply, while the VDDIOx supplies are for I/Os. The VCCD is the analog power supply. There is no sequencing requirement for power supplies, but VDD and VCCD must be monotonic.

Power Supply Filtering

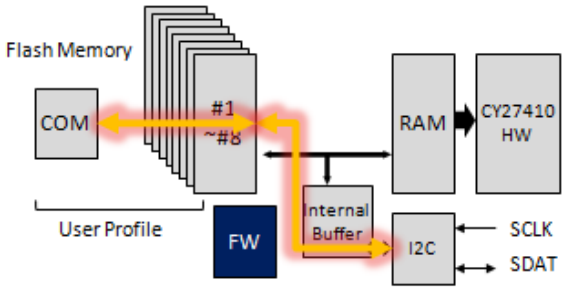
Power supply filtering is especially important for clock signal integrity. Each VDD and VDDIO pin must have a 100-nF capacitor close to the pin, and a 2.2-µF (or higher) capacitor

VCCD is an additional power supply pin for this device, since the device (CY27410) internal power supply is 1.8 V, this pin will be the LDO (Low Drop Out) output when using 2.5 V or 3.3 V range of core power supplies (VDD and VDDA), so you should connect the 100-nF capacitor to this pin closely and not connect any power from external sources. However, if you use the device with a 1.8-V power supply, the internal LDO will be bypassed, so this pin requires 1.8 V externally generated power supply for the core, 100-nF capacitor must be connected close to this pin.

Internal Memory Structure

Figure 33 shows the internal memory structure of the CY27410 device. It has a nonvolatile (NV) and a volatile (RAM) inside. The RAM directly controls the CY27410 hardware. An internal hardware communication buffer handles I²C communications.

Figure 33: Internal Memory Structure



Programming CY27410

CY27410 programming is done using the I²C bus interface.

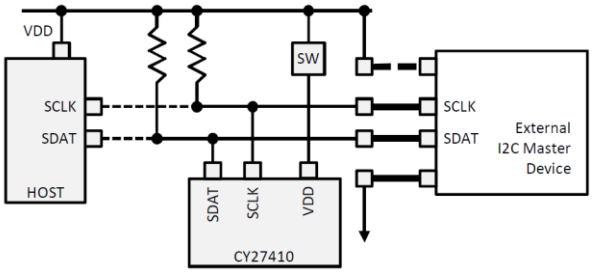
On-Board Programming

On-board programming can be done by the on-board Host that communicates with CY27410 through commands and data that contains COM, FS, and miscellaneous information like I2C address, read/write protection etc.

Using an External I²C Master

You can use an external I²C master device such as Cypress MiniProg™, Cypress TT-Bridge™ or another I²C-qualified device to program user configuration into an un-programmed (virgin) CY27410 device on the system.

Figure 34. Using an External I2C Master to Program CY27410



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Conclusion

CY27410 is a 4-PLL spread-spectrum clock generator targeted at consumer, industrial, and networking applications. Its superior specifications and value-added features such as voltage-controlled crystal oscillator (VCXO), frequency select, and zero/nonzero delay buffer (ZDB/NZDB) modes make it an ideal choice for a wide variety of applications.

Document History

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Document Number: 001-94024

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4664885	XHT	02/18/2015	New Application Note
*A	5847700	GNKK	08/08/2017	Updated the Cypress logo and copyright information.

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