

## Solving PCI Express Timing Challenges with CY27410

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**Associated Project: No**

**Associated Part Family: CY27410**

**Related Application Notes: [AN94024](#), [AN94074](#)**

AN93892 introduces Cypress's latest CY27410 clock device that solves timing challenges of PCI Express interfacing. The device can generate eight differential and four single-ended clock outputs up to 700 MHz with subpicosecond jitter. From a high-speed system design point of view, CY27410 simplifies the clock-buffering scheme, where a single clock source can be fanned out to multiple PCI Express inputs in multifunction module systems.

### Introduction

Cypress's latest generation four-PLL clock device CY27410 is ideal for PCI Express (PCIe)-based multifunction module systems. CY27410 can generate eight differential and four single-ended clock outputs at up to 700 MHz with sub-picosecond jitter.

The device's architecture is based on Cypress's proven S8™ technology, which integrates the frequency-synthesis capability of four low-jitter PLLs in a single IC. To maximize design flexibility, each of the eight differential pins can also be configured to eight LVCMOS clocks to support any signal format and I/O voltage.

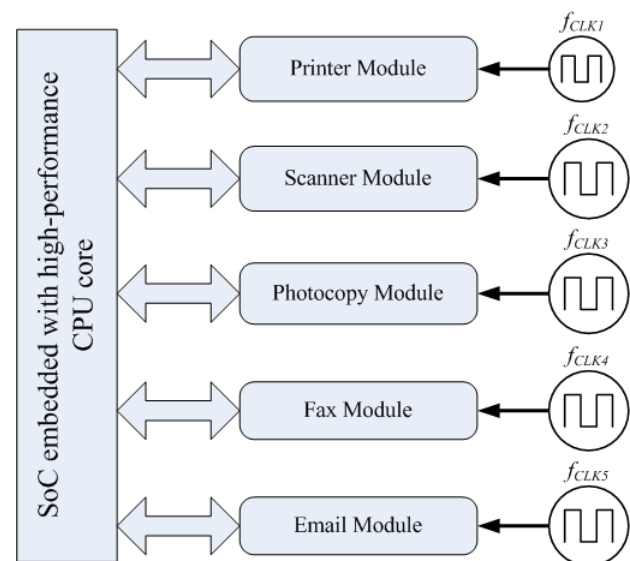
From a high-speed system design point of view, this architecture simplifies the clock-buffering scheme, as multiple clock signals from a single IC can synchronously be applied to PCIe interfaces. This will replace the use of individual ICs like clock buffers, level translators, and crystal oscillators with a single device that can minimize cost, PCB area, and power consumption.

#### General features of CY27410: Configurable Frequencies, Voltages, and I/O Standards

CY27410 is mainly targeted for the application-specific devices like multifunction printer (MFP). ASIC or SoC modules of MFPs have built-in PCIe stack to simplify system design. A typical clocking interface of functional modules of an MFP is shown in [Figure 1](#).

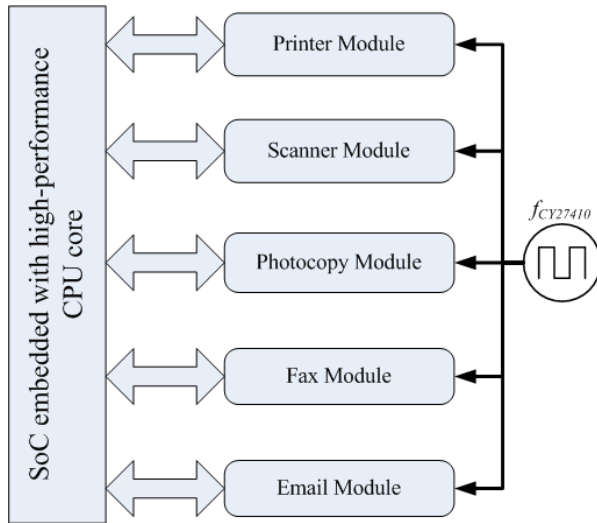
Here, multiple modules need multiple clocks in multiple formats, but synchronized with respect to the central clock-generation device. Each module's clock requirement is satisfied by separate clock generators. This approach of clock sourcing requires several different parts, with significant impact on PCB area, BOM complexity, power budget, and cost.

Figure 1. Typical Multifunction Printer Module Driven by Multiple Clock Sources



Design with CY27410 will be a better solution for such complex system designs. In [Figure 2](#), all individual clock sources shown in [Figure 1](#) are replaced with a single CY27410 clock generator.

Figure 2. System Block Diagram If CY27410 Is Used in Multifunction Printer



The CY27410 can easily meet mixed-format clocking requirements. It can provide eight independent differential (LVDS, LVPECL, HCSL, and CML) clocks, and four single ended (LVCMOS) clocks, all synthesized from a single crystal reference or externally supplied clock. The stand-alone jitter performance of this device is less than 1 ps and phase-noise bandwidth is 12 kHz to 20 MHz. In addition, there is independent choice of supply voltages (1.8 V, 2.5 V, and 3.3 V) with configurable output drivers for design flexibility. CY27410 supports PCIe-compliant spread-spectrum modulation for PCIe Gen 2.0 and 3.0 reference clock applications. The latest-generation PCIe specifications are listed in Table 1.

Table 1. Characteristics of PCIe Links

PCIe Version	Nominal Bit Rate	Per Lane Data Throughput	Max Data Throughput (32 Lanes)	Year of Release
2.1	5.0 Gbps	1 Gbps	32 Gbps	2007
3.0	8.0 Gbps	2 Gbps	64 Gbps	2010

### Various Sources of Clock Jitter

CY27410 is chosen to be suitable for PCIe-based systems as it meets the system-level PCIe jitter specifications. These system-level and the IC-level jitter specifications are listed in Table 2.

Table 2. Transmitter and Receiver Jitter Specifications for PCIe Applications

System/Device	TX / RX Ref Freq	Spread-Spectrum	RMS Jitter Spec
PCIe 3.0	100 MHz	0.5 % (down spread)	1.0 ps
CY27410	100 MHz	0 to 0.5 % (down spread)	< 1.0 ps

The jitter performance of any clock IC may largely get affected if the system design constraints are not properly followed. Typical noise sources of increased clock jitter are as follows:

- If the on-board voltage regulator is a Buck/Boost type of circuit, the switching frequency and its higher order harmonics typically introduce noise in the PCB, thereby adding noise on clock signal lines
- The Input-Output buffers of the interfaced ICs like DSP/FPGA/SoC may switch at a very high frequency. If the power supplies to the clock ICs are not properly isolated from the power supplies of the interfaced switching devices, it induces noise to the clock output
- If there is no proper shielding between two nearby clock lines, the mutual inductance between the two lines causes crosstalk, and thereby increases clock jitter.

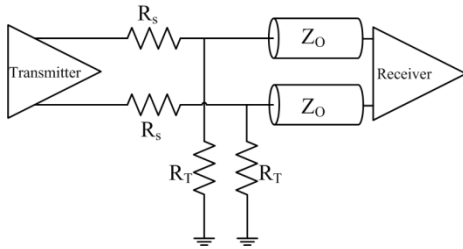
Excessive clock jitter can potentially render the clock unsuitable for intended PCIe-based applications and has negative impact on system-jitter margins, or increase the bit error rate. Therefore, it is important for the system designers to follow proper design guidelines, and ensure proper board layout of power planes, ground planes, and high-speed signal lines.

## HCSL I/O Standard

CY27410 supports the 100-MHz high-speed current steering logic (HCSL) output for the PCIe interface. HCSL is the differential-output standard with a current source, which is derived from an open-source transistor. This unterminated current source, when terminated through an external 33-Ω series resistor ( $R_s$ ) and a 50-Ω termination resistor ( $R_T$ ) to ground, drives a current of 25 mA (see Figure 3).

An HCSL driver is a high-impedance output with quick switching times. The  $R_s$  resistors can be fine-tuned on the PCB to reduce overshoot and ringing. The HCSL driver of CY27410 provides the required switching speeds, and phase-noise performance that meets I/O standard requirements of PCIe applications.

Figure 3. HCSL Termination for Applications Where a Point-to-Point PCIe Connection Is Used



## Spread-Spectrum Clock Source

High-speed clock generators are the sources of electromagnetic interference (EMI) that creates noise on other signal lines, thereby causing jitter. Therefore, CY27410 is enabled with a programmable spread-spectrum feature.

This spread-spectrum-enabled clocking is an important consideration for a PCIe clock source. In spread spectrum, the high-frequency clock is modulated by a low-frequency signal to spread out the radiated energy across a wide range of frequencies. This technique lowers the radiation from high-frequency lines driven by a spread-spectrum clock.

PCIe devices are specified to reliably transmit data using a reference clock with a specific spread-spectrum modulation rate of 30 to 33 kHz and modulation amplitude of 0 to -0.5%. CY27410 supports 30 kHz to 60 kHz modulation frequency, and 0.1% to 5% modulation amplitude.

In a PCIe application, each device must transmit data within a bit rate of  $\pm 300$  ppm of each other. Therefore, the same reference clock must be supplied to both devices synchronously if spread-spectrum is enabled. See Table 3 for a summary of typical AC characteristics of CY27410 spread-spectrum clock output.

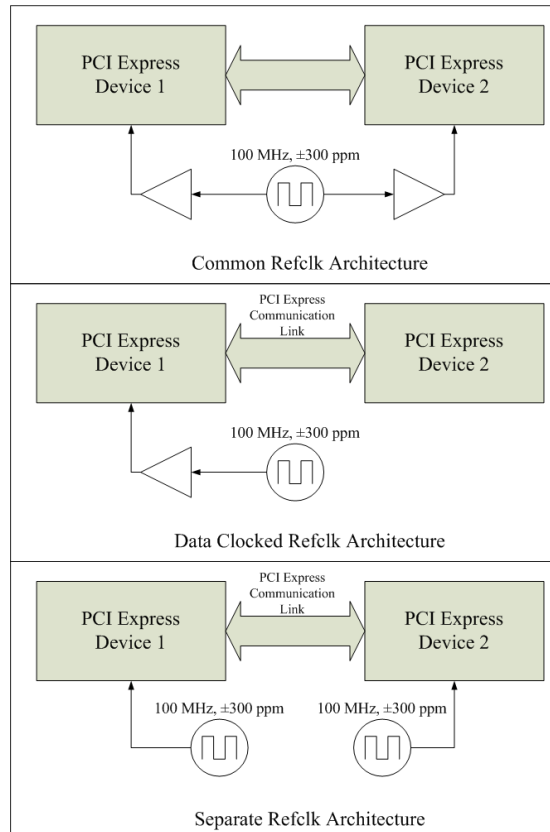
Table 3. AC Electrical Specification of Spread-Spectrum Enabled Clock Output of CY27410

AC Characteristics	Conditions	Specification
Accuracy of average clock period (100 MHz)	Measurement taken from differential waveform, Spread Spectrum enabled (0.5% down spread)	-300 ppm to 2800 ppm
Absolute period		9.874 ns to 10.203 ns
Additive phase noise		0.4 ps (RMS)

## PCIe Clocking Architectures

CY27410 supports all the three types of PCIe clocking architectures (Common Refclk, Separate Refclk, and Data Clocked Refclk). Figure 4 shows a block diagram of all the three architectures.

Figure 4. Clock Architectures for PCIe Interfacing



The *Common Reference clock* (Common Refclk) architecture is the most commonly used architecture that uses spread-spectrum clocking to reduce EMI. As this architecture requires, CY27410 clock source can be distributed to every PCIe device while keeping minimum skew between multiple clock outputs.

The *Data Clocked Reference clock* (Data Clocked Refclk) architecture is the simplest clock implementation because it requires only one clock source located at the transmitter. Here, receivers will simply extract the embedded clock from CY27410.

In the *Separate Reference clock architecture* (Separate Refclk), a different clock source is used at each end of the PCIe link. Both clock sources can still have a frequency accuracy of  $\pm 300$  ppm because the PCIe standard allows for a total frequency deviation of 600 ppm between the transmitter and receiver. In this architecture, the frequency margin is very small to enable the spread-spectrum feature, but the use of a single CY27410 IC will allow tightly-controlled clock distribution over different devices.

## Conclusion

The CY27410 provides a solution to PCIe 3.0 timing challenges. Its frequency flexibility, support for multiple frequency profiles, and unprecedented flexibility in output formats help system designers to avoid some of the common clock design pitfalls. It replaces the use of individual clock buffers, level translators, and crystal oscillators, thereby simplifying the design, minimizing BOM cost, and reducing PCB real estate.

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## Document History

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**	4663739	TAVA	02/18/2015	New Application Note
*A	5877259	AESATMP8	09/08/2017	Updated logo and Copyright.

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