THIS SPEC IS OBSOLETE

Spec No: 001-87578

Spec Title: AN87578 - PROC(TM) - TT HARDWARE DESIGN GUIDELINES

Replaced by: NONE

PRoC™–TT Hardware Design Guidelines

Author: Selvakumar Manickam
Associated Project: N/A
Associated Part Family: CYRF89535
Software Version: N/A

AN87578 describes the recommended hardware design guidelines for PRoC–TT (Programmable Radio-on-a-Chip – TrueTouch®). Included are schematics and layout design guidelines to create designs with capacitive touch and wireless capabilities. PRoC–TT, which is part of the PRoC–UI (Programmable Radio-on-a-Chip–User Interface) product family, is a single-chip-solution that combines Cypress's TrueTouch technology with a 2.4-GHz, gaussian frequency shift keying (GFSK)-modulated, 1-Mbps wireless transceiver.

Contents

1 Introduction

The PRoC–TT is a 2.4-GHz RF solution integrated with Cypress' TrueTouch capacitive touch-sensing, 8-bit MCU. The PRoC–TT is a complete solution, featuring 32 KB flash with support for up to two finger gestures, and a GFSK data rate of 1 Mbps over the wireless link. Here are some key applications that you can create using PRoC–TT:

- Wireless touch mouse
- Wireless trackpad
- Wireless keyboard with integrated trackpad
- Wireless remote control with integrated trackpad

This application note includes a reference schematic to illustrate the best practices to apply if you are designing a wireless touch mouse using PRoC–TT.

The following sections explain how to create schematics and layout for a PRoC–TT-based application. Included is a checklist to ensure conformance to hardware design guidelines.

2 WirelessUSB Resources

Cypress provides a wealth of data at www.cypress.com to help you to select the right WirelessUSB device for your design, and quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the wireless webpage

- **Overview**: Wireless Roadmap , Modules Roadmap , Wireless Portfolio
- **Product Selectors**: Wireless Product selector
- **Datasheets**: Describe and provide electrical specifications for various device families. You can access the datasheet of all wireless products here.
- **Application Notes and Code Examples**:

  Cover a broad range of topics, from basic to advanced level. Many of the application notes include code examples. You can access the complete list of wireless AN here and code examples here.
- **Technical Reference Manuals (TRM)**:

  Provide detailed descriptions of the architecture and registers in each WirelessUSB device family.

  You can access the complete list of wireless products TRM here.
- **Development Kits**:

  You can access the complete list of wireless kits and reference designs here

  Cypress also offers ARM Cortex-M0 based, single-chip Bluetooth Low Energy (BLE) or Bluetooth Smart solutions. You can learn more about Cypress BLE devices here

2.1 PSoC Designer

PSoC Designer is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system bring-up and time-to-market. Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. Finally, debug and test your designs with the integrated debug environment including in-circuit emulation and standard software debug features.

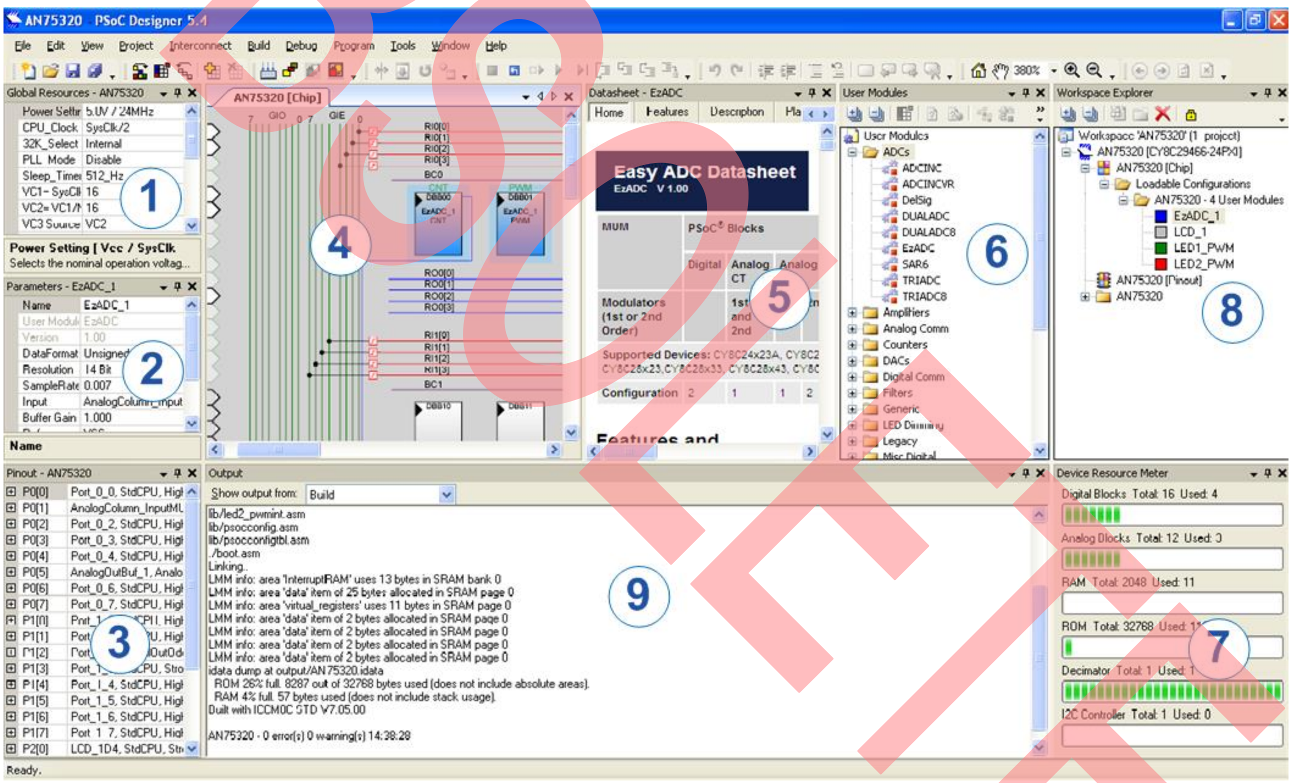
- Application Editor GUI for device and User Module configuration and dynamic reconfiguration
- Extensive User Module Catalog
- Integrated source code editor (C and Assembly)
- Free C compiler with no size restrictions or time limits
- Built-in Debugger
- Integrated Circuit Emulation (ICE)
- Built-in Support for Communication Interfaces:
  - Hardware and software I2C slaves and masters
  - Low/Full-speed USB 2.0
  - Up to 4 full-duplex UARTs, SPI master and slave, and Wireless

Figure 1 shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources –** all device hardware settings.
2. **Parameters –** the parameters of the currently selected User Modules.
3. **Pinout –** information related to device pins.
4. **Chip-Level Editor –** a diagram of the resources available on the selected chip.
5. **Datasheet –** the datasheet for the currently selected UM
6. **User Modules –** all available User Modules for the selected device.
7. **Device Resource Meter –** device resource usage for the current project configuration.
8. **Workspace –** a tree level diagram of files associated with the project.
9. **Output –** output from project build and debug operations.

Note: For detailed information on PSoC Designer, go to **PSoC® Designer** > **Help** > **Documentation** > **Designer Specific Documents** > **IDE User Guide**.

Figure 1. PSoC Designer Layout



3 Typical PRoC–TT Hardware Design

Figure 2. Typical PRoC–TT-based Design

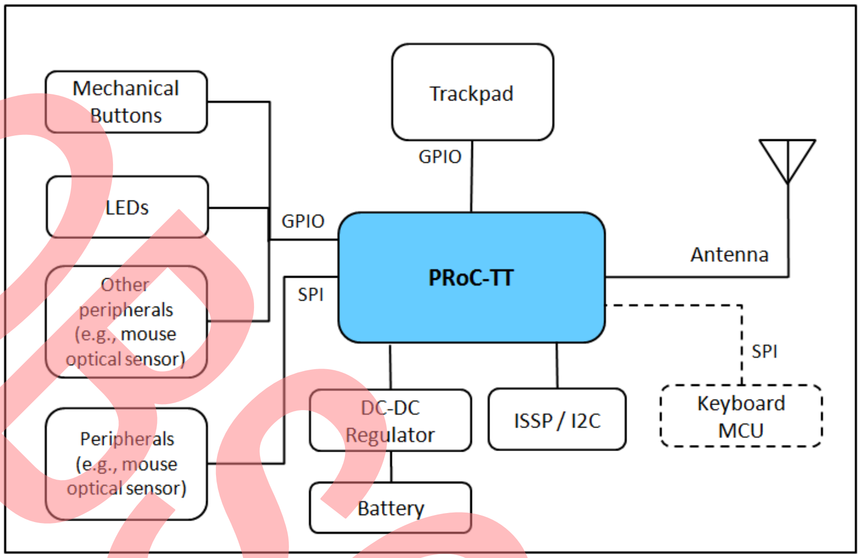


Figure 2 illustrates a typical PRoC–TT-based hardware design. You can use these designs with a PRoC-USB-based dongle design that acts as the wireless receiver to a PC to receive data from PRoC–TT based devices.

The following sections briefly describe the subsystems that make up the design. Detailed schematics and layout guidelines are covered later.

If your application requires touch button and slider type capacitive-sensing interfaces, you can create them using PRoC-CS, is another device that belongs to the PRoC-UI family. For more details, see PRoC-CS Hardware Design Guidelines in Reference Documents.

3.1 Trackpad

A trackpad is a two-dimensional area implemented using a set of sensors arranged in rows and columns, with each row and column connected to a GPIO. Twenty-six GPIOs are available to create the trackpad based on application requirements.

3.2 2.4-GHz Wireless Capability

PRoC-TT provides wireless capability using a built-in 2.4-GHz RF transceiver. To implement RF functionality, connect an antenna and a matching network to PRoC–TT.

3.3 Mechanical buttons, LEDs, and Other Peripherals

To implement mechanical buttons and LEDs, use GPIOs. You can connect other peripherals, such as mouse optical sensors, GPIOs as well.

3.4 Power Supply

The power supply consists of a power source, such as AA/AAA batteries, and an optional DC-DC regulator. PRoC–TT can operate in the range of 1.9 V – 3.6 V.

3.5 Programming (ISSP) and Debugging (I^{2}C)

An in-system serial programming (ISSP) Interface is required to program the firmware onto a PRoC–TT device. PRoC–TT supports I^{2}C slave, and it is used to tune and debug the trackpad functionality by measuring sensor capacitance. You can access both interfaces using the MiniProg3 kit. For more information, refer to the development kit listed in the Reference Documents section.

3.6 Keyboard MCU

A separate MCU needs to be interfaced with PRoC-TT to create a wireless keyboard with an integrated trackpad capability. This MCU processes the keyboard events and sends the keyboard data to PRoC-TT over an SPI interface. PRoC-TT combines the keyboard data along with trackpad data and transmits over an RF link to the dongle.

4 PRoC–TT vs. PRoC–LP/PRoC–LPStar

Table 1 lists the differences between PRoC–TT and other PRoC devices, such as PRoC-LP and PRoC-LPStar.

Table 1. PRoC–TT vs. PRoC-LP/PRoC-LPStar

Parameter	PRoC–TT (CYRF89535)	PRoC-LP/PRoC-LPStar (CYRF6936/ CYRF6986)
Radio	2.4 GHz with GSFK modulation	2.4GHz with GFSK or DSSS modulation
Radio Tx Power	+1 dBm	+ 4 dBm
Max Tx Power consumption	22.5 mA	45 mA
Touch capabilities	Trackpad	None

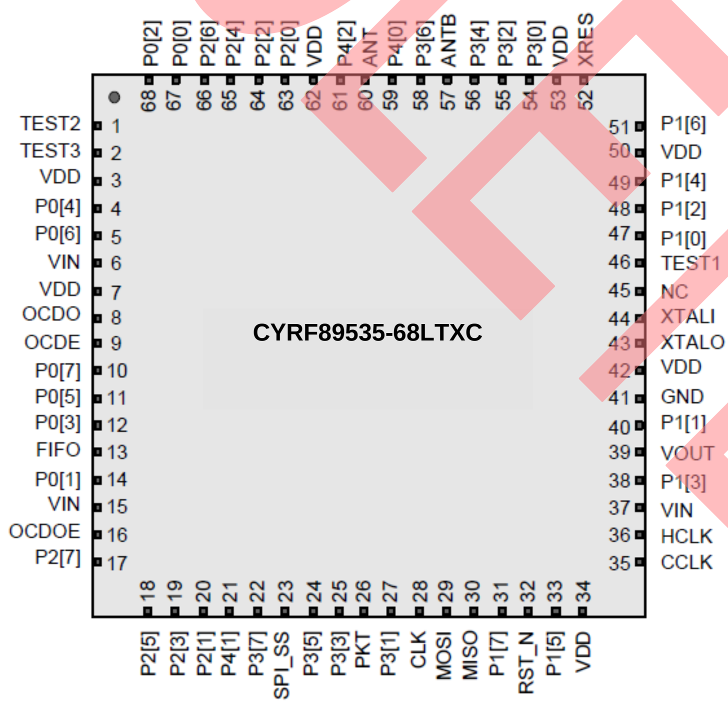
To summarize, PRoC–TT provides additional capacitive touch capabilities with the next-generation, low-power, 2.4-GHz transceiver.

5 Schematics Design

5.1 PRoC–TT Pinout

PRoC–TT is available in a 68-QFN package. Figure 3 describes the pinout details:

Figure 3. 68-QFN PRoC–TT Pinout



5.2 Power Supply

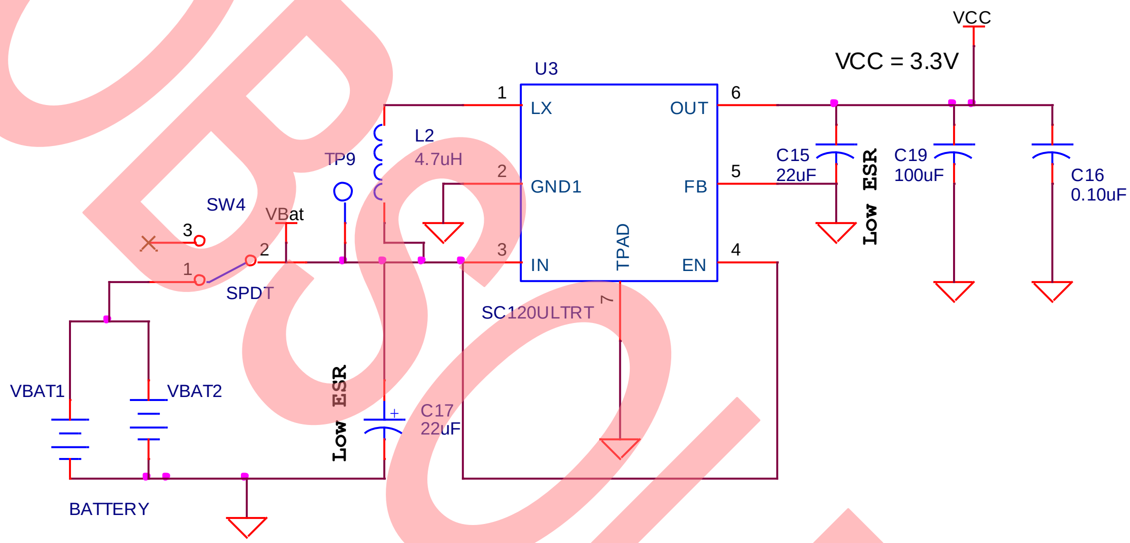
5.2.1 Power Supply Design

PRoC–TT can operate in the voltage range of 1.9 V to 3.6 V. Cypress recommends that you use an external DC-DC regulator for the following types of applications:

- Applications powered by a single AA or AAA battery
- Applications, such as mouse optical sensors, with parts that require a constant supply voltage

Figure 4 shows a reference power supply design for PRoC–TT using an external DC-DC regulator.

Figure 4. Reference Power Supply Design Schematics



VBAT1= VBAT2 = (0.95V - 1.65V)

5.2.2 DC-DC Regulator Part Selection Criteria

The DC-DC regulator part must meet the following criteria:

- The output voltage range is 1.9 V to 3.6 V.
- The output noise at the 50-kHz component must be less than 50 mV pk-pk.

5.2.3 Reference DC-DC Regulator Parts

The recommended DC-DC regulator parts that you can use in PRoC–TT-based hardware designs are as follows:

SC120ULTRT: Semtech Corp.'s part is a high-efficiency, low-noise, synchronous step-up/boost DC-DC regulator that provides boosted voltage levels in low-voltage handheld applications. The reference Power Supply Design Schematics described in Figure 4 use this regulator.

LT1763CS8-3.3: The LT1763 series LDO by Linear Technology is a low-noise, low dropout regulator capable of supplying 500 mA of output current with a dropout voltage of 300 mV. LT1763 parts are available in an eight-pin package. Because these parts can support an input voltage range of 3.7 V to 20 V, you can use them in designs in which an AC-DC adapter or lithium-ion batteries are used as a power source.

Table 2. Reference DC-DC Regulator Parts

Regulator Part Number (Manufacturer)h	Type	Vin (V)	Vout (V)
SC120ULTRT (Semtech)	Step-up DC-DC Regulator	0.7 – 3.8	3.3
LT1763CS8-3.3 (Linear Technology)	LDO Regulator	3.7 – 20	3.3

5.2.4 Handling Low Battery Condition

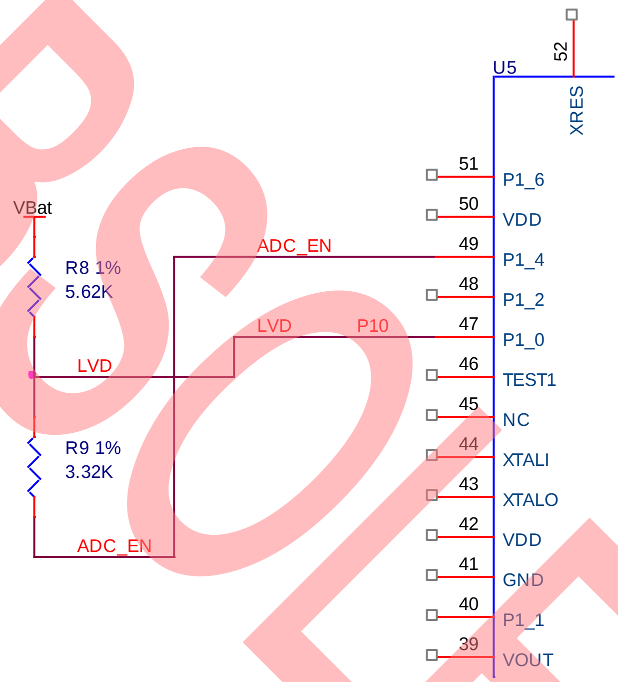
The power supply design should ensure that battery leakage does not occur when the battery is running low. If you use a DC-DC regulator, determine whether the regulator has a feature called undervolt lockout, which causes automatic shutdown when the battery gets low.

If the regulator does not support this feature, add a mechanism in the firmware to detect a low battery condition. This also applies to designs that do not use a DC-DC regulator.

Figure 5 describes a schematic to detect the battery voltage level using the built-in ADC of PRoC–TT.

We recommend that you choose resistors with a 1% tolerance for those used on a PRoC-TT-based design.

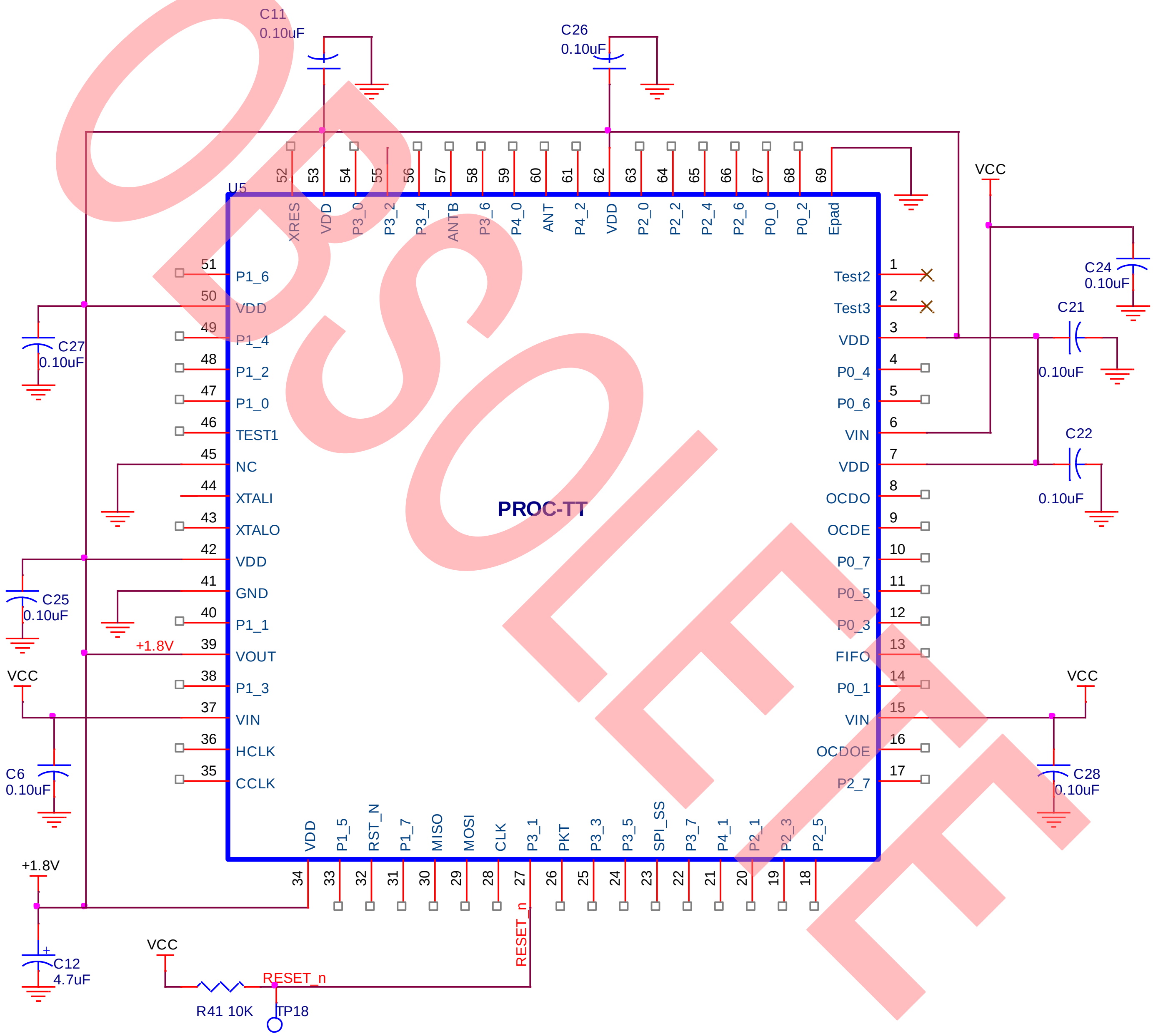
Figure 5. Detecting Battery Level



5.2.5 Power Supply Connectivity

PRoC–TT has 3 Vin pins. Vin supports the operating voltage, which can vary between 1.9 V and 3.6 V. PRoC–TT has a built-in LDO that provides a constant output of 1.8 V (Vout), which powers seven VDD pins, as shown in Figure 6. The following schematics describe the connectivity among VIN, VOUT, and VDD pins.

Figure 6. PRoC–TT Power Supply Connectivity

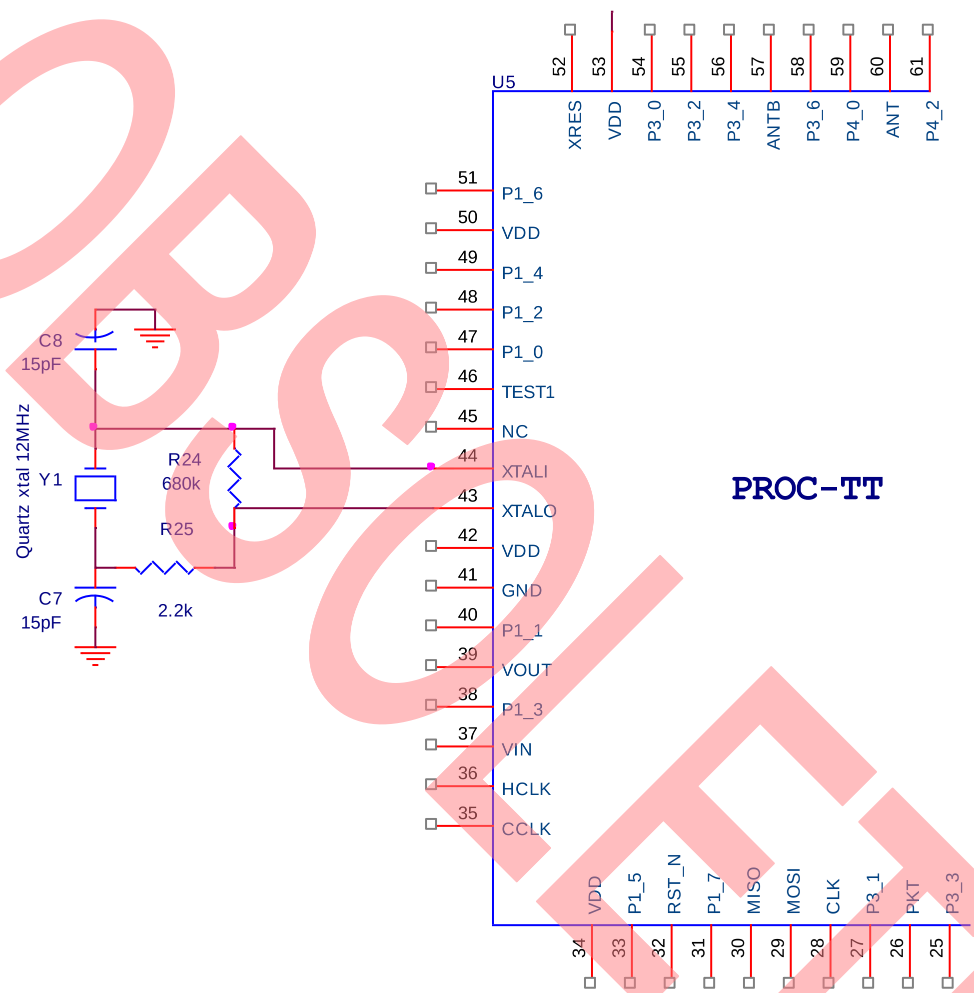


5.3 Clock

5.3.1 Clock Circuit Design

PRoC–TT requires an external crystal. Figure 7 shows the reference schematic for the clock circuit.

Figure 7. Clock Circuit Design



5.3.2 Crystal Part Selection Criteria

The crystal used on a PRoC–TT-based design must meet the following criteria:

- Fundamental mode, parallel resonant 12.000 MHz
- Frequency tolerance of ±40 ppm. This tolerance must be calculated by using the RSS (root square sum) approach involving the following four types of errors represented in ppm:
  - Base, or initial error, measured at room temperature (I_{ppm})
  - Drift due to temperature changes within the operating temperature range of 0 ^{o}C to 70 ^{o}C (T_{ppm})
  - Drift attributed to aging (A_{ppm})
  - Uncertainty caused by load capacitance error (L_{ppm})

Apply the following formula to calculate the total frequency tolerance using RSS:

Equation 1

$$Frequency\,Tolerance = \sqrt{I_{ppm}^2 + T_{ppm}^2 + A_{ppm}^2 + L_{ppm}^2}$$

Maximum ESR value of 80 ohms

- 10-pF load capacitance is preferred

5.3.3 Reference Crystal Parts

Table 3. Reference Crystal Parts

Manufacturer Part Number	Manufacturer	Stability	Load Cap.
7B-12.000MEEQ-T	TXC Corp.	10 ppm	10 pF
7M-12.000MEEQ-T	TXC Corp.	10 ppm	10 pF
NXK12.000AE12F-KAB5	JenJaan Quartek	20 ppm	12 pF

5.3.4 Calculating Load Capacitance Values

Load capacitors play a critical role in providing an accurate clock source to PRoC–TT, which is important for PRoC–TT to generate accurate RF signals. These capacitors must be chosen carefully based on the load capacitance value of the crystal. The following section explains how to choose the correct load capacitance values.

Figure 8. Crystal Circuit

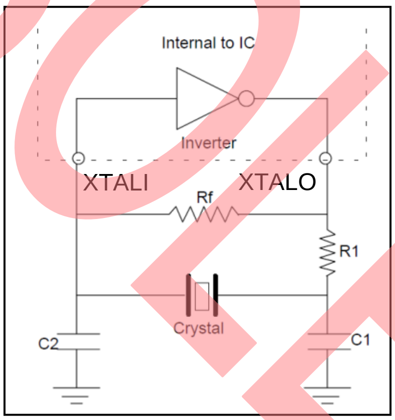


Figure 8 illustrates the crystal circuit. To provide the most accurate clock source, crystal manufacturers specify the optimum load capacitance value that must be supported on the circuit. The two capacitors (C1 and C2) determine the load capacitance, and the net load capacitance is calculated using the following equation:

Equation 2

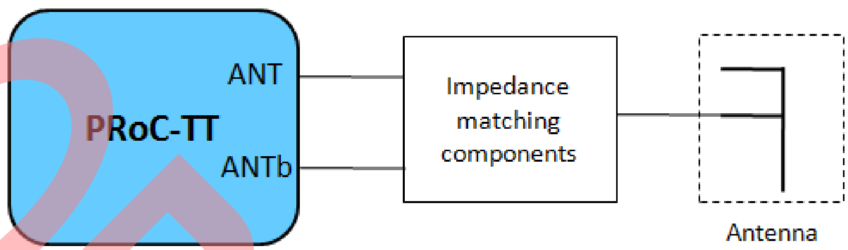
$$C_L = \frac{C_1 * C_2}{C_1 + C_2} + C_S$$

Cs is the stray capacitance of the printed circuit board whose typical value is 2.5 pF. Therefore, values of C1 and C2 must be chosen in such a way that they match the crystal's specification. For a crystal with a 10-pF load capacitance, the load capacitance value will be 15 pF for both C1 and C2.

5.4 2.4-GHz RF

5.4.1 2.4-GHz RF Design Overview

Figure 9. PRoC–TT RF Design Overview



PRoC–TT has a WUSB-NL RF transceiver that can provide up to 1-Mbps data throughput. PRoC–TT supports differential RF input/out using ANT and ANTb pins. You must connect these pins to a two-element matching network to provide 50-ohm impedance matching for PRoC–TT.

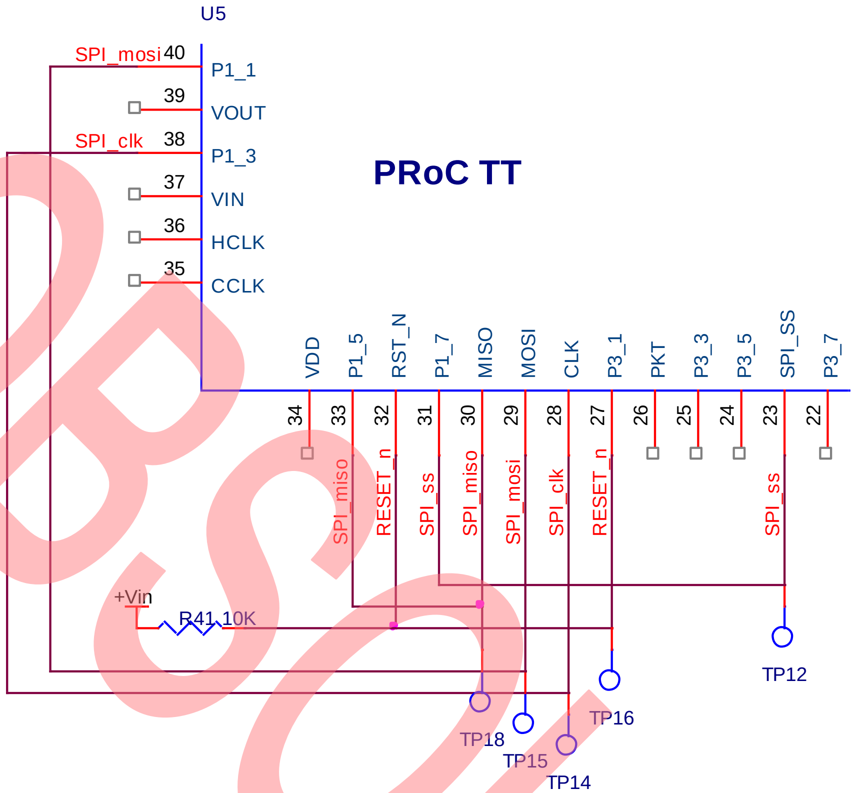
5.4.2 MCU and RF Connectivity

The built-in MCU and WUSB-NL blocks must be connected over SPI externally. All PRoC–TT-based hardware designs must implement this connectivity externally by following these steps:

- Connect MOSI to P1.1
- Connect MISO to P1.5
- Connect CLK to P1.3
- SPI_SS can be connected to any GPIO (preferably P1.7)
- Connect RESET_n to a GPIO with a pull-up resistor. The WUSB-NL block must be reset using this GPIO.

Figure 9 shows the connectivity between the MCU and WUSB-NL blocks. Make sure to add test points on the previously mentioned signal lines to enable debugging during firmware development.

Figure 10. MCU and RF Connectivity



5.4.3 Matching Circuit Design

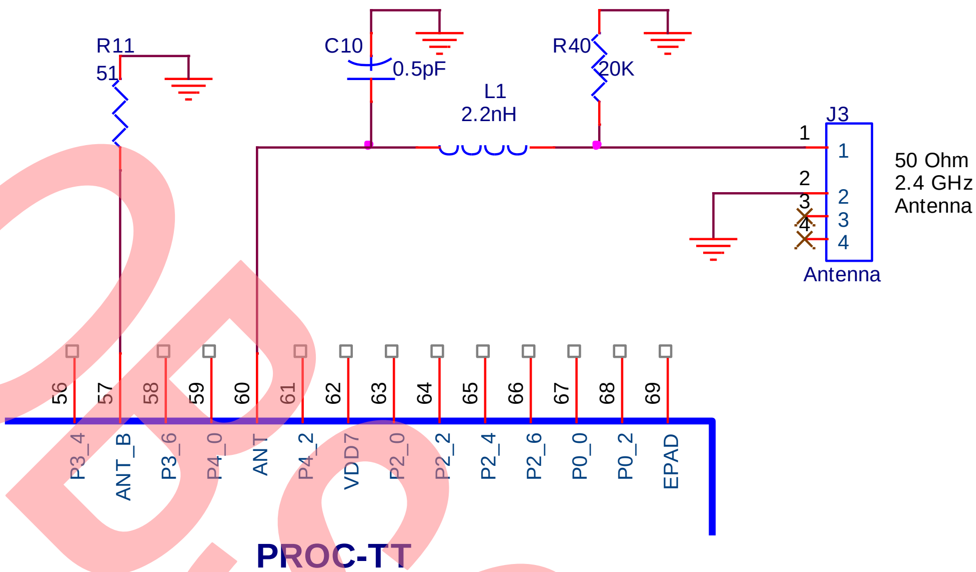
A shunt capacitor (0.5 pF) and a series inductor (2.2 nH) form the matching network to match the impedance between PRoC–TT and the antenna. Do not modify the values shown below. When you select these components, choose parts that have low loss at RF. The chosen parts should exhibit a minimum Q of approximately 20 or better at 2.4 GHz. The reference part numbers for the matching network are shown:

Table 4. Matching Network Passives

Type	MPN	Manufacturer
0.5-pF capacitor	500R14N0R5CV4T	Johanson Dielectric
2.2-nH inductor	MLG1608B2N2S	TDK

The differential antenna input/output (ANTb) pin should have a resistance to ground of 51 Ω ± 20%, to match its 50-Ω impedance. In addition, the ANT pin requires a DC path to ground. A resistor of 20 kΩ, ± 20%, to ground must be placed on the antenna-side end of the matching network, as shown in Figure 11.

Figure 11. Matching Network Design

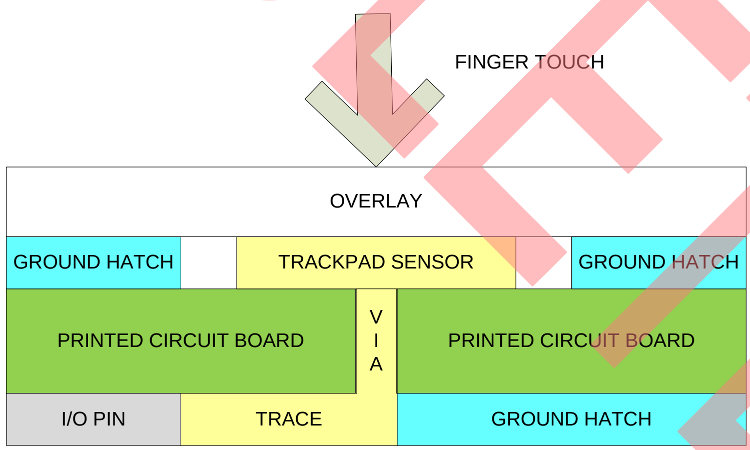


5.5 Trackpad

5.5.1 Basics of capacitive sensing

Capacitive touch sensing technology measures the change in capacitance due to the presence of a finger on each I/O pin that is designated as a sensor. A sensor is implemented using copper pads etched on the surface of the PCB. That sensor is connected to a GPIO of the PRoC–TT controller. A non-conductive overlay serves as the touch surface for the button. Figure 12 shows you how to build a trackpad sensor on a two-layer PCB design.

Figure 12. How a Capacitive Sensing Interface Works



The sensor capacitance measured by PRoC–TT is called Cx. When a finger is not on the sensor, Cx is equal to the parasitic capacitance of the system (Cp). When a finger is placed on the sensor, Cx increases to Cp+Cf, where Cf is the finger capacitance. This increase in capacitance is used to detect a TOUCH or NO TOUCH state for the sensor. These sensors are arranged as rows and columns in a trackpad. By checking the state (TOUCH / NO TOUCH) of each row and column, you can track the precise location of up to two fingers and the direction in which those fingers are moving on the trackpad.

5.5.2 Trackpad Design

The available number of GPIOs determines the trackpad area that can be implemented on a hardware design. The following table lists the total GPIOs available on PRoC–TT.

Table 5. Available GPIOs for Trackpad

Total GPIOs	Reserved GPIOs	GPIOs available for Trackpad
35	9	26

Table 6 provides more details about the reserved GPIOs and their usage:

Table 6. Reserved GPIOs of PRoC–TT

#	GPIO	Purpose
	P1[0]	Programming Interface (ISSP SDATA)
2	P1[1]	Programming Interface (ISSP SCLK) and SPI MOSI for WUSB-NL block
3	P1[3]	SPI CLCK for WUSB-NL block
4	P1[5]	SPI MISO for WUSB-NL block
5	P0[1]/P0[3]	To connect CMOD CAP
6	P4[0]	RESET for WUSB-NL block
7	P4[2]	SPI SS for WUSB-NL block
8	P3[6]	For non-trackpad usage
9	P3[4]	For non-trackpad usage

Figure 13. Trackpad Design

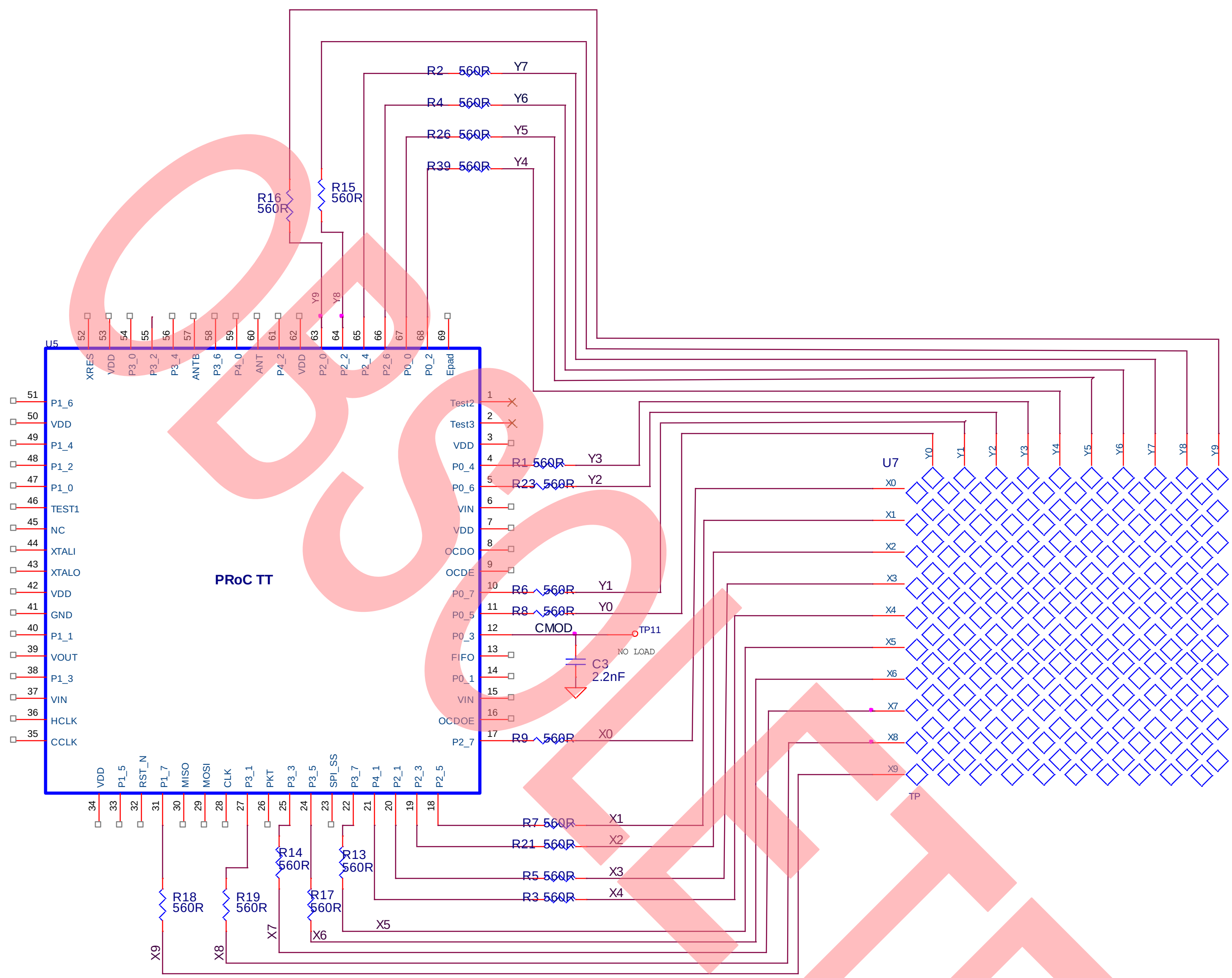


Figure 13 illustrates the design of a trackpad area consisting of 10 row sensors and 10 column sensors. Note that each row and column sensor needs to be allocated a dedicated GPIO pin.

Note: Remember these important points while designing a trackpad:

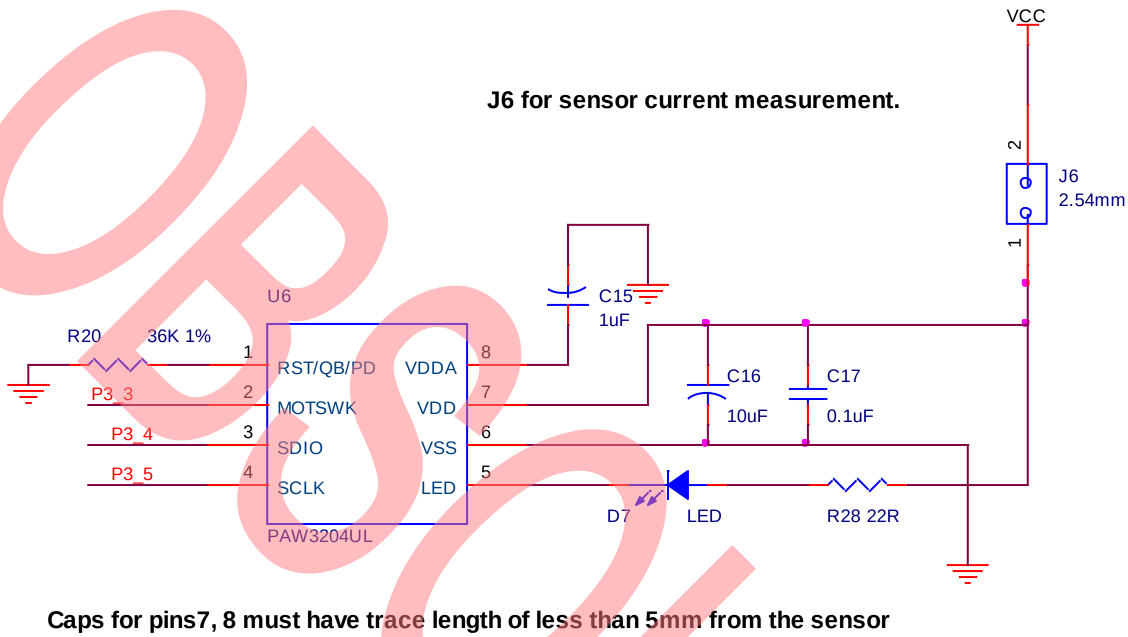
- Use a 560-ohm series resistor for all GPIOs employed as sensors.
- Connect an integration capacitor, called ‘CMOD’, with a value of 2.2 nF. Connect it to either pin P0.3 or P0.1 only.
- Do not use GPIO P1.0 or P1.1 as trackpad sensors, because they need to be reserved for programming (ISSP) and debug (I^2C) interfaces.
- Do not use two pins adjacent to ANT and two pins adjacent to ANTb for touch sensors.

5.6 Peripherals

5.6.1 Integrating Peripherals Over GPIO

You can use PRoC–TT GPIO lines to create an interface with LEDs, mechanical buttons, and peripherals, such as a mouse optical sensor. Figure 14 shows how to use these GPIOs to connect a mouse optical sensor (PAW3204UL).

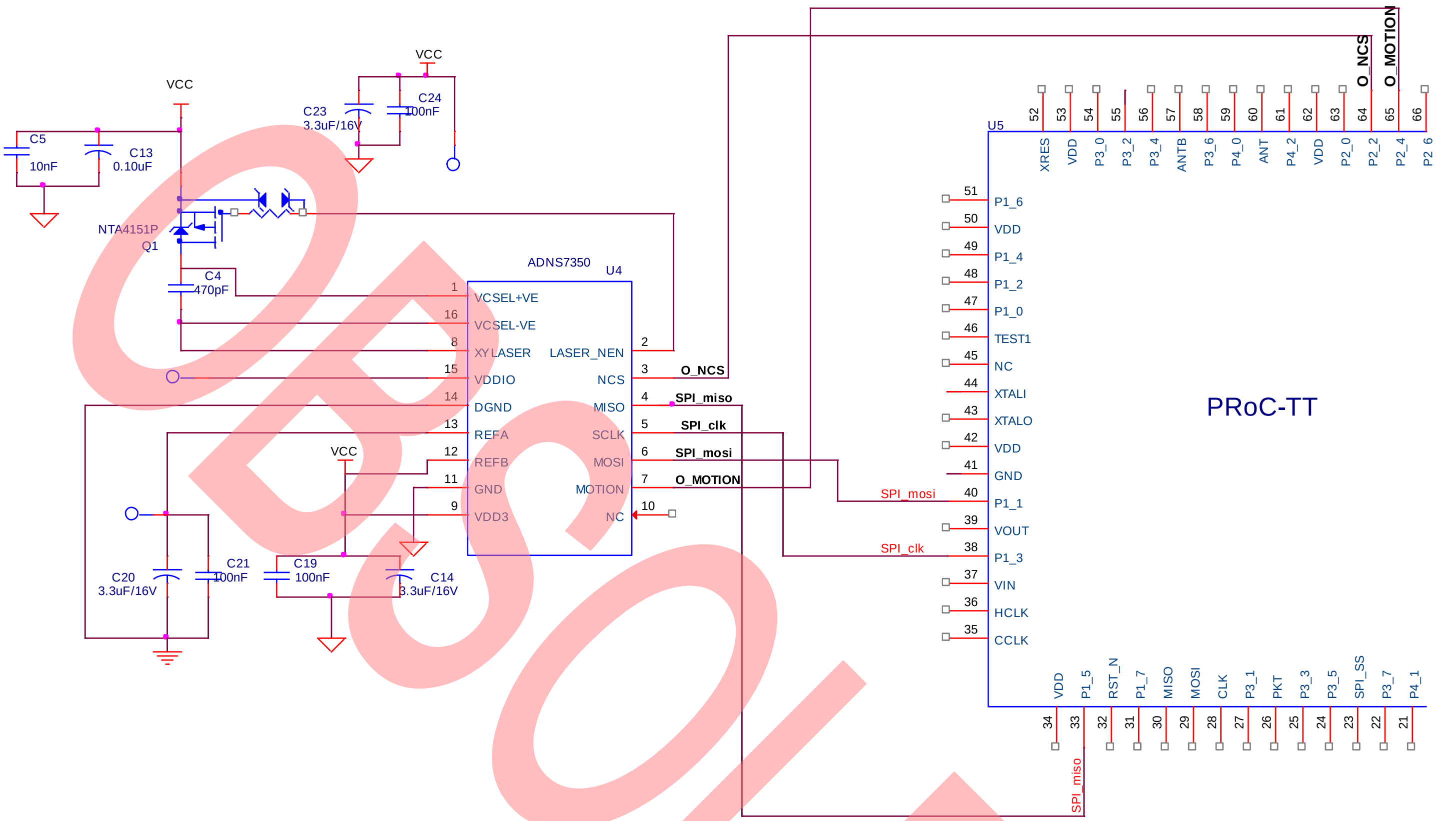
Figure 14. Interfacing Mouse Optical Sensor over GPIO



When you connect LEDs, use the negative terminal of the LED to GPIO, and the positive terminal to VCC, because the sink current for PRoC–TT is higher than the source current.

5.6.2 Integrating Peripherals Over SPI

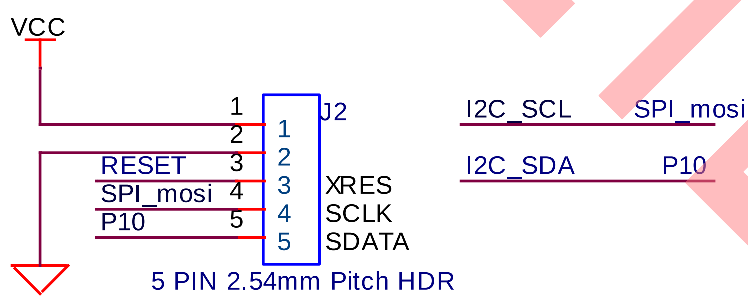
Figure 15. Interfacing Mouse Optical Sensor over SPI



You can connect SPI-based peripherals to PRoC–TT in multi-slave mode. Figure 15 shows how to add an SPI-based mouse optical sensor (ADNS7350) over an SPI interface to PRoC–TT. This forms a two-slave SPI network, because the built-in WUSB-NL also acts as another SPI slave.

5.7 Programming (ISSP) and Debugging (I^{2}C)

Figure 16. Programming and Debugging Interface



The ISSP interface is used to download firmware onto PRoC-TT's flash. The I^{2}C interface is used to debug and fine-tune sensor capacitance while developing firmware to implement the trackpad features. Cypress can help you tune the sensor capacitance during your firmware development. Please contact the Cypress tech support team (procui@cypress.com) whenever you require such support. Note that ISSP and I^{2}C share common lines, as shown in Figure 16.

6 Layout Design

The following sections describe the layout guidelines to create PRoC–TT-based hardware designs:

6.1 Layer Stack Up

You can design PRoC–TT-based hardware on either a two-layer or a four-layer PCB design. A four-layer approach is preferred because it enables a compact design by allowing you to place components below the trackpad area, while meeting the layout guidelines. However, if you use a two-layer design, make sure you meet all of the layout guidelines.

Figure 17 and Figure 18 illustrate the layer stack up for two- and four-layer designs.

Figure 17. Two-Layer Stack Up

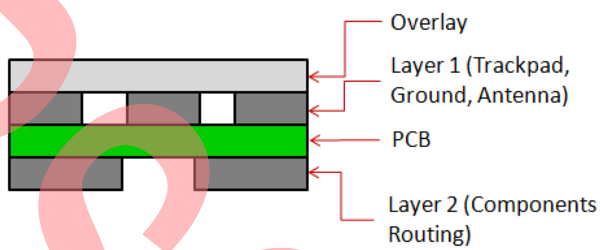
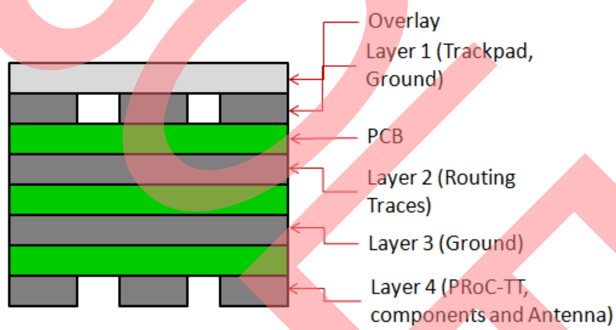


Figure 18. Four-Layer Stack-Up



FR4-based PCB designs perform well, with board thicknesses ranging from 0.020 inches (0.5 mm) to 0.063 inches (1.6 mm).

Refer to the Trackpad Layout Guidelines: Quick Reference table for a complete list of recommended values for various layout parameters.

6.2 PRoC–TT Device Package Dimensions

PRoC–TT is available in an 8-mm x 8-mm package, and the recommended width of the solder pad to use on the PCB is 0.2 mm.

6.3 Power Supply

6.3.1 Power Supply Design

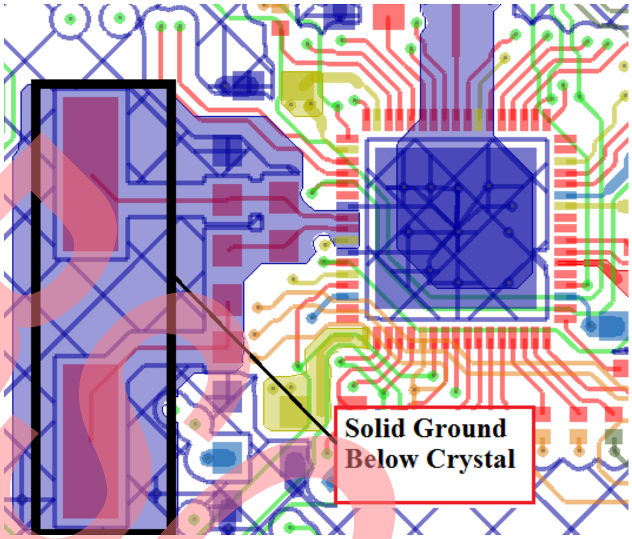
- Decoupling capacitors must be placed as close as possible to PRoC–TT.
- Do not gang the decoupling capacitors. Instead, connect them individually to the corresponding power terminals.

6.4 Clock

6.4.1 Clock Circuit Design

- Do not route any trace beneath the crystal pads. The layer beneath the crystal pads must have solid ground, as shown in Figure 19.

Figure 19. Crystal Layout Design

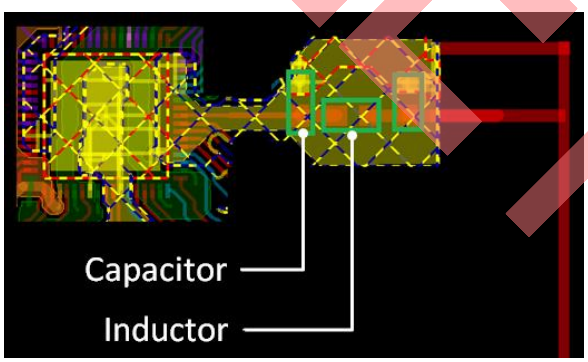


- Place the crystal as close as possible to PRoC–TT.

6.5 2.4-GHz RF Design

- PRoC–TT supports different types of antenna designs. Refer to the section Antenna Recommendations for the list of antenna designs. This application note also provides the dimension details of PIFA Antenna Dimension. Pick an antenna design that suits your application. The guidelines provided in this document are based on the PIFA antenna, and these guidelines apply to other antenna types, too.
- Place the Antenna Matching Network Passives, as shown in Figure 20.

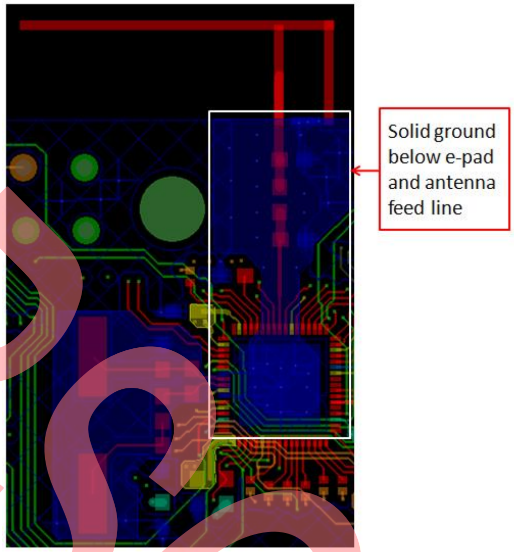
Figure 20. Antenna Matching Network



- Use vias to implement ground stitching between the top and bottom layers.
- Maximize ground in complete design. Note that hatched ground must be used in areas where CapSense buttons and sliders are located. The rest of the area can use solid ground.
- The layer beneath the PRoC–TT e-pad must be solid ground, and it must be extended until the antenna feed line, as shown in Figure 21. Note that the ground regions are marked in blue.

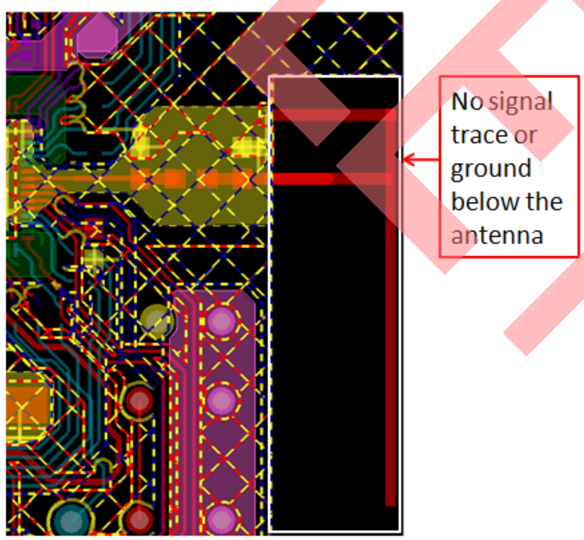
- The top layer on which PRoC–TT is mounted must have solid ground pad, which aligns with the PRoC–TT e-pad, and this pad must be soldered to the e-pad. In addition, this ground pad on the top layer must be connected, using thermal vias, to the ground pad located in the layer beneath.

Figure 21. Ground Below E-pad and Antenna Feed Line



- Neighboring I/Os near ANTb and ANT must not be routed in parallel to ANT and ANTb lines
- All grounds on the hardware must be connected
- The antenna must be isolated from other layers, and no signal traces or ground must be added in any of the layers, as shown in Figure 22.

Figure 22. Isolation of Antenna

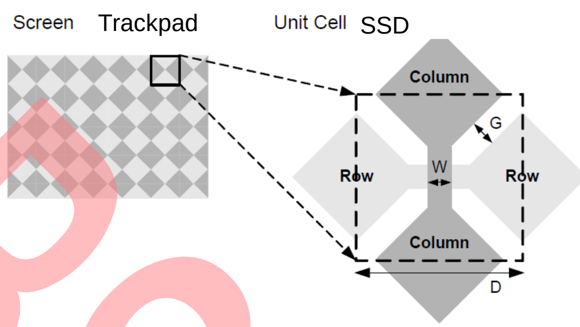


- During PCB manufacturing, do not place metal content, such as a PCB vendor logo, Pb-free symbol, or manufacturing lot number, under the antenna, because any metal under the antenna can affect the RF radio range. You must ensure that this is mentioned explicitly in the fabrication notes of layout design files.

7 Trackpad Design

A trackpad is implemented using a set of sensors arranged in rows and columns. Each row and column is connected to a GPIO. The sensor layout supported by PRoC–TT is called a single solid diamond (SSD), and the following image illustrates its design.

Figure 23. Design of SSD



The diamond pitch has three sensor parameters: sensor pitch (D), gap (G), and bridge width (W).

Sensor Pitch (D): Sensor pitch refers to the distance between neighboring rows or columns; that distance can differ in the X (D_x) and Y (D_y) directions. However, the ratio between the lower distance value and the higher distance value should be within the range of 80% to 100%.

The sensor pitch affects the accuracy of a touch panel; in general, the smaller the pitch, the higher the accuracy. The pitch can vary from 3.5 mm to 6.5 mm, and the recommended pitch is 5 mm. The trade-off for having better accuracy with a smaller pitch is a higher I/O count and a slower scan rate.

Gap (G): The gap refers to the distance between the edges of adjacent diamonds. This gap ranges between 8 mils and 12 mils, and the recommended distance is 12 mils.

Bridge Width (W): The bridge width refers to the width of the interconnecting bridges for row or column sensors. The recommended width is 7 mils.

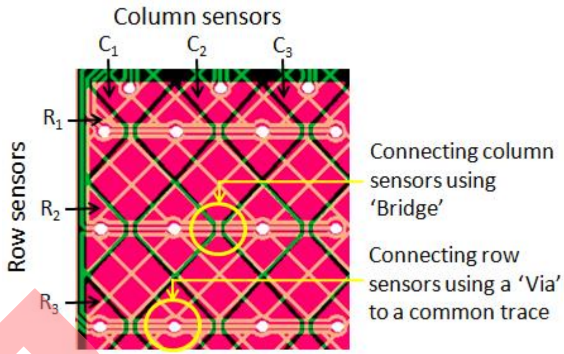
In addition, the overlay material (e.g., Mylar) can have a dielectric of 3 – 8, and the thickness can vary from 0.5 to 1.0 mm.

8 Trackpad layout guidelines

- Decide on the number of row and column sensors for the trackpad based on the trackpad size requirement and the values frozen for Sensor Pitch (D), Gap (G) and Bridge Width (W). For example, a 60- x 40-mm (width x height) trackpad can be realized using eight row sensors and 12 column sensors.
- The sensors can be connected using one of the following two approaches:
  - **Connection using Bridge**. All sensors located in a row or column are connected using a bridge trace.
  - **Connection using Via.** Sensors are connected to a trace, which is routed in the layer underneath using vias. This trace is common for all sensors located in a row or a column.

  The figure below illustrates the approach used to connect sensors using bridge and via.

Figure 24. Interconnecting Sensors



After the number of row and column sensors is decided, identify the type of sensors larger in number (row / column). Connect that sensor type using 'Bridge' approach and the other sensor type using 'Via' approach. This approach will minimize the use of vias in the design.

- Ensure that the diamond is filled up without any gaps. The following image illustrates incorrect and correct diamond construction.

Figure 25. Incorrect Diamond Construction

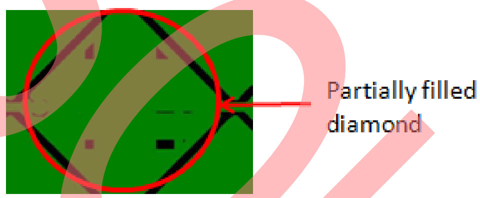
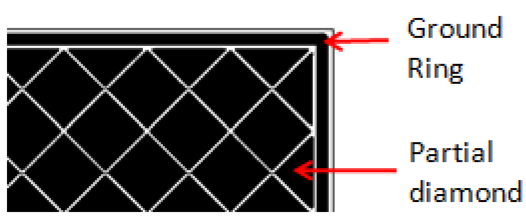


Figure 26. Correct Diamond Construction

- Fill the edges with partial diamonds, as shown, and ensure that there are no empty regions. Also, add a ground ring around the trackpad area for ESD protection. The width of the ring can vary from 1 mm to 3 mm, with 3 mm as the preferred width. This ground ring is closed, and it needs to be connected to the ground plane in beneath layer at as many places as possible.

Figure 27. Partial Diamonds and Ground Ring



- Note that 26 GPIOs are available to construct the trackpad. Assuming a sensor pitch of 6.5 mm, you can create a trackpad with a maximum size of 105 mm x 65 mm by using 10 row sensors and 16 column sensors. You can change the aspect ratio of this trackpad by re-arranging the row and column sensors, as required.

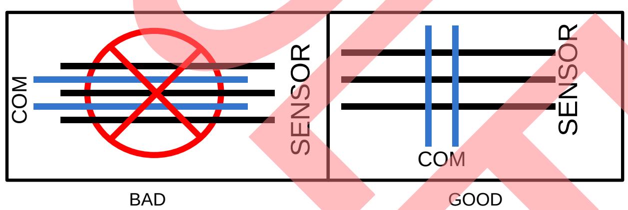
8.1 Sensor Placement and Vias

- Minimize the trace length from PRoC–TT GPIO pins to the trackpad diamonds, to optimize signal strength
- Mount series resistors within 10 mm of PRoC–TT GPIO pins to reduce RF interference and to provide ESD protection
- Isolate switching signals, such as PWM, I^2C communication lines, and LEDs, from the sensor diamond and the sensor PCB traces. Do this by placing a ground trace or by filling a hatched ground between trackpad traces and non-trackpad traces to avoid crosstalk.
- Avoid connectors between the diamond sensor and PRoC–TT GPIO pins because connectors increase parasitic capacitance and decrease noise immunity.
- Use the minimum number of vias to route sensors to minimize parasitic capacitance.

8.2 Trace Length, Width, and Routing

- Minimize the parasitic capacitance of the traces and sensor pad. Trace capacitance is minimized when the traces are short and narrow.
- Trace width should not exceed 7 mil (0.18 mm) and should be surrounded by hatched ground with trace-to-ground clearance of 10 mil to 20 mil (0.25 mm to 0.51 mm).
- Route sensor traces on the bottom layer of the PCB, so that the only user interaction with the trackpad sensors is with the active sensing area. Do not route traces directly under any sensor diamond unless the trace is connected to that sensor.
- Do not run trackpad traces close to communication lines, such as I^2C or SPI masters. If you need to cross communication lines with sensor pins, make sure the intersection is at a right angle, as shown in Figure 28.

Figure 28. Routing of Trackpad and I^2C/SPI Traces



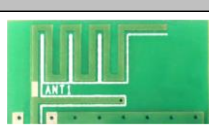
Cypress can help you create sensor designs for your products, including FPC-based sensor designs for products with a curved overlay. Please contact the Cypress tech support team (procui@cypress.com) to use the sensor design service.

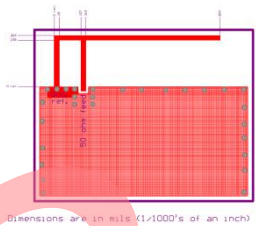
8.3 Antenna Recommendations

The antenna is usually the biggest factor in achieving successful RF performance. A rigorous antenna tutorial is beyond the scope of this application note, but let's look at some simple antenna recommendations you can easily apply to PRoC–TT-based applications.

You can use virtually any type of high-quality 50-ohm, 2.4-GHz antenna with the PRoC–TT. Table 7 lists several available choices.

Table 7. Antenna Choices

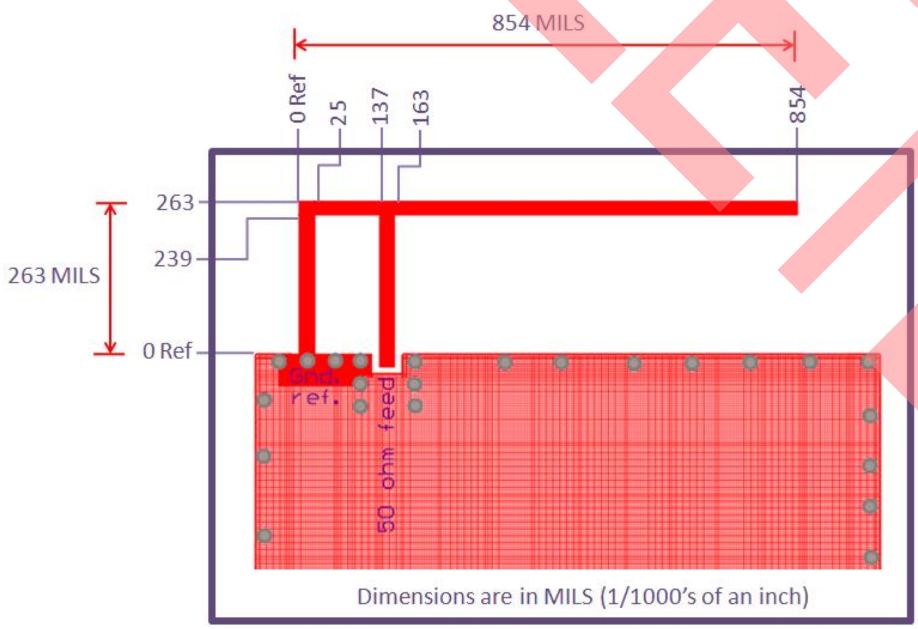
Antenna Type	Picture or Drawing	DC Grounded?	Description / Notes
Wiggle antenna		Yes	Described in the Cypress application note *AN48610 - Design and Layout Guidelines for Matching Network and Antenna for WirelessUSB™ LP Family*. Cost: Almost free of cost when added to the existing PCB.

Antenna Type	Picture or Drawing	DC Grounded?	Description / Notes
PIFA		Yes	The Printed Inverted-F Antenna (PIFA). Cost: Almost free when added to the existing PCB. See Figure 29 for details of antenna dimensions
Custom printed-trace antenna	This is a specialized antenna, customized to each application.	Depends on the design	Cost: Almost free of cost when added to the existing PCB.
Chip antenna	 Model 2450AT18B100E, Johanson Technology Inc.	No	Easy to use. You must read the datasheet and follow the manufacturer's instructions. The manufacturer's specifications for mounting and layout must be followed precisely. Cost: Can be expensive.
1/2 wave end-fed dipole	 Illustrated: Model W1010, by Pulse.	No	Delivers 'textbook' 0-dBd performance. Easy removal and replacement. Accommodates EMC compliance and end applications. Requires RF connector on the board. Cost: Relatively expensive.

8.4 PIFA Antenna Dimension

Figure 29 shows detailed dimensions of the PIFA antenna for PRoC–TT designs.

Figure 29. PIFA Antenna Dimensions



9 Trackpad Layout Guidelines: Quick Reference

Table 8. Trackpad Layout Guidelines

Sl.	Category	Min	Max	Recommendations/Remarks
1	Sensor Pitch (D)	3.5 mm	6.5 mm	Sensor pitch refers to the distance between neighboring rows or columns, and that distance can differ in the X and Y directions. 5 mm is the recommended sensor pitch.
2	Gap (G)	12 mils	12 mils	The gap refers to the distance between the edges of adjacent diamonds.
3	Bridge Width (W)	7 mils	7 mils	The bridge width refers to the width of the interconnecting bridges for row and column sensors.
4	Overlay Thickness	0.5 mm	1.0 mm	Overlay material (e.g., Mylar) can have a dielectric of 3 – 8, and the thickness can vary from 0.5 mm to 1.0 mm.
5	Trace Pitch	14 mils	14 mils	A trace or routing pitch is the sum of trace width (7 mils) and spacing between the traces (7 mils).
6	Ground Flood – Top Layer	-	-	Hatched ground 7-mil trace and 45-mil grid
7	Ground Flood – Bottom Layer	-	-	Hatched ground 7-mil trace and 70-mil grid

10 Schematics and Layout Review Checklist

The following table lists all the important guidelines as a checklist. Please assign an answer to each of the checklist items to find out the extent to which your hardware design meets the guidelines.

Table 9. Schematics and Layout Review Checklist

#	Checklist Item	Answer (Yes / No/ NA)
1	Is correct load CAP values used based on 'Load Capacitance' value of the crystal?	
2	Are all seven VDD pins of PRoC–TT connected to VOUT?	
3	Is connectivity between MCU and WUSB-NL blocks of PRoC–TT established over SPI?	
4	Are test points added on the SPI lines connecting the MCU and WUSB-NL blocks?	
5	Are all the sensors attached with a 560-ohm series resistor?	
6	Is the value of the CMOD capacitor used 2.2 nF?	
7	Are ISSP SDATA and ISSP SCLK connected to P1[0] and P1[1], respectively?	
8	Does the power supply design ensure that battery leakage does not occur under low battery condition?	
9	Is the antenna laid out exactly according to the dimensions?	
10	Is it ensured that no ground/trace running below the PIFA antenna?	
11	Are matching network passives placed on the antenna feedline?	
12	Is adequate solid ground added below the ANT, ANTb pins, and antenna feed line?	
13	Are de-coupling capacitors placed close to power pins?	
14	Is ground ring added around the trackpad area?	
15	Is hatched ground laid out in a 45 degree angle?	
16	Is it ensured that there are no breaks in the diamonds in each of the row sensors?	
17	Is it ensured that there are no breaks in the diamonds in each of the column sensors?	
18	Is it ensured that the adjacent pins of ANT and ANTb are not used to create trackpad area?	
19	Is it ensured that GPIO P1.0 or P1.1 is not used to create trackpad area?	
20	Is solid ground added below crystal pads?	
21	Is hatched ground added around trackpad area?	
22	Is hatched ground added below trackpad area?	
23	Are all the grounds connected?	
24	Is the trackpad laid out per the 'Trackpad layout guidelines – Quick Reference' table?	
25	Are the solder pads laid out with 0.2-mm width for the PRoC-TT pins?	

#	Checklist Item	Answer (Yes / No/ NA)
26	Is ground on each layer connected to each other using as many vias as possible?	
27	Are series resistors placed within 10 mm from PRoC–TT pins?	
28	Is the ratio between the lower sensor pitch value and higher sensor pitch value within the range of 80% to 100%?	
29	Is the higher number of sensor type (row / column) connected using 'Bridge' approach?	
30	Is the lower number of sensor type (row / column) connected using 'Via' approach?	

11 Reference Documents

- AN72428 – Schematic Review Checklist for WirelessUSB™ NL
- AN64285 – WirelessUSB™ NL Low Power Radio Recommended Usage and PCB Layout
- AN48610 – Design and Layout Guidelines for Matching Network and Antenna for WirelessUSB™ LP Family
- AN86272 – PRoC™-CS Hardware Design Guidelines
- 001-83907 Design Guide – Getting Started with PRoC™ – UI
- PRoC™-TT Datasheet (released only under NDA)

12 Development Kit

- CY8CKIT-002 PSoC® MiniProg3 Program and Debug Kit

Document History

Document Title: AN87578 - PRoC™ – TT Hardware Design Guidelines

Document Number: 001-87578

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3981960	SELV	05/14/2013	New Spec.
*A	4788109	DEJO	06/05/2015	Updated template
*B	4862112	DEJO	07/28/2015	Sunset Review Added WirelessUSB Resources section
*C	6268696	ANKC	07/31/2018	Obsoleting the spec

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/usb
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone : 408-943-2600
Fax : 408-943-4730
Website : www.cypress.com