AN87209

Overview of nvSRAM I²C I/O Specs Standardized by Cypress across I²C Modes

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Associated Part Family: Serial I²C nvSRAMs
Software Version: None
Related Application Notes: AN74875

AN87209 highlights the differences between the I²C nvSRAM I/O specifications and the NXP I²C-bus specifications. Note that these differences should not have an impact in typical I²C systems.

Introduction

Cypress's I²C nvSRAM is a standard serial I²C nonvolatile RAM (NVRAM) that offers the highest I²C access speed (up to 3.4 MHz), zero delay nonvolatile data write, and infinite writes to SRAM. Alternatively, most I²C EEPROMs, which are used as serial nonvolatile memory, offer speeds up to 1 MHz, page programming delay of a few milliseconds (~5 ms), and limited write endurance count. These EEPROM limitations make it unable to meet key system requirements, such as fast nonvolatile memory write and higher endurance cycles in some applications. Since the Cypress nvSRAM does not have these limitations, it is an ideal replacement for EEPROMs in such applications. The I²C nvSRAM's electrical specifications (DC and AC specifications of I²C) are aligned with the majority of I²C compliant EEPROM devices that allow an I²C nvSRAM to share the same I²C bus without any change to the system setup.

The I²C nvSRAM offers all four standard I²C bus modes (Standard-mode: 100 KHz, Fast-mode: 400 KHz, Fast-mode plus: 1 MHz, and High-speed mode: 3.4 MHz) through a single solution. As a result, Cypress has standardized some of the I/O specifications across all modes to offer consistent I/O behavior across the modes.

Differences between I²C nvSRAM I/O and the NXP I²C-bus Specification

This section describes the I²C nvSRAM specifications, which are not fully aligned with the NXP I²C-bus specifications and also discusses their impact (if any) at the system level. Refer to Table 1 through Table 3 for a specification comparison between the I²C nvSRAM I/O and the NXP I²C-bus specification.

I_{OL} – Low-Level Output Current

The Fast-mode plus I²C standard specifies SCL and SDA I/O drive strength as 20 mA (sink current), whereas it is 3.0 mA for the rest of the standard I²C-bus modes, as shown in Table 1.

Table 1. Low-Level Output Current

I²C-bus Mode	NXP		nvSRAM	
	Min	Max	Min	Max
Standard-mode	3 mA	–	3 mA	–
Fast-mode	3 mA	–	3 mA	–
Fast-mode plus	20 mA	–	3 mA	–
High-speed mode	3 mA	–	3 mA	–

Since the I²C standard allows sharing an I²C-bus with mixed I²C-bus mode slave devices, the output drive strength with I_{OL} = 3.0 mA for V_{OL} = 0.4 V is within the specified operating range of a standard I²C slave device and can easily drive the I²C-bus to logic LOW.

V_{hys} - Hysteresis of Schmitt Trigger Inputs

The I²C nvSRAM implements two-stage noise filtering on its input signal path: the first-stage filter removes the high-frequency noise components (input signal pulse width (t_{SP}) less than 10 ns) through an on-chip glitch filter, whereas the other noise components are filtered out by the Schmitt trigger input buffer. The Schmitt trigger input hysteresis (V_{hys}) helps in filtering out any spurious noise on the I²C-bus and prevents input buffers from any false trigger.

The I²C nvSRAM supports an input hysteresis specification of 0.05 x V_{CC} (or 5%), which is aligned with the hysteresis specification of all standard I²C-bus modes except for the High-speed mode for which the hysteresis spec is 0.1 x V_{DD} as shown in Table 2.

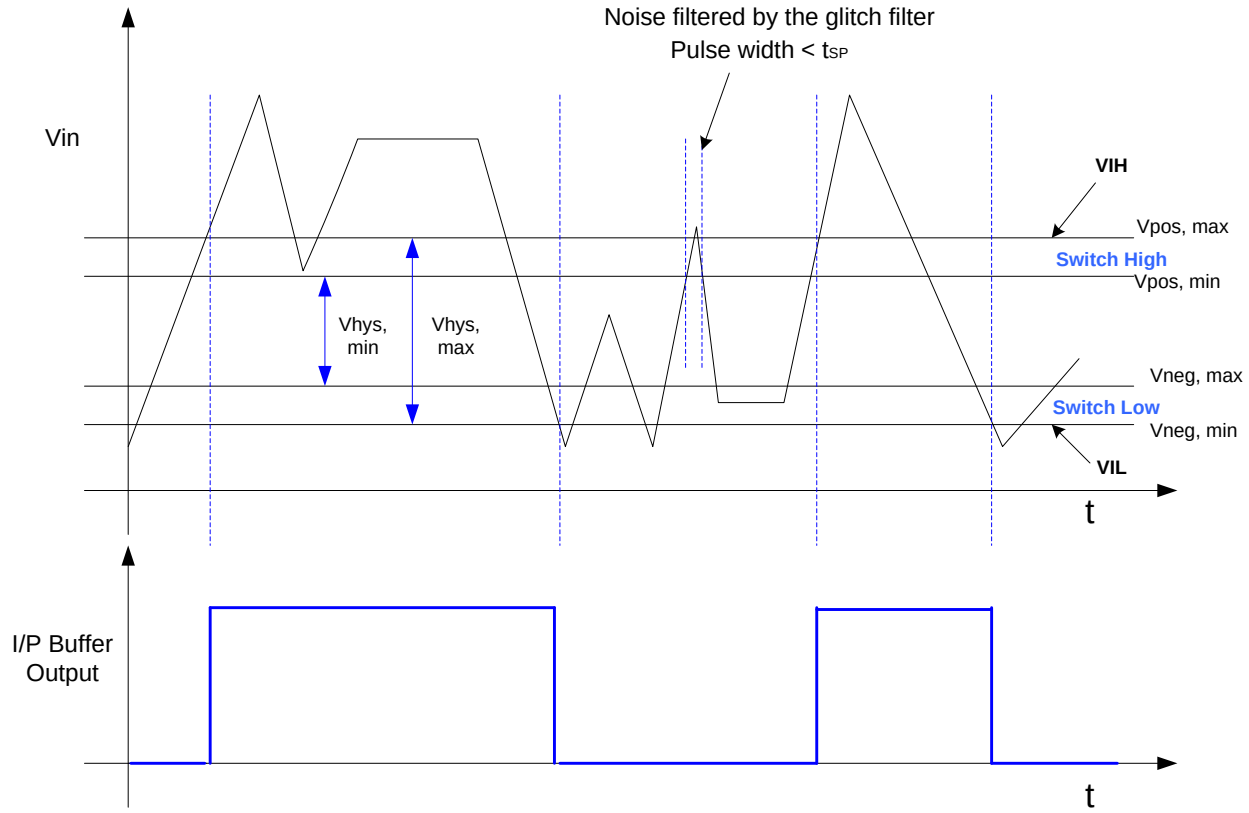
Table 2. Hysteresis of Schmitt Trigger Inputs

I²C-bus Mode	NXP		nvSRAM	
	Min	Max	Min	Max
Standard-mode	0.05 x V_{DD}	–	0.05 x V_{CC}	–
Fast-mode	0.05 x V_{DD}	–	0.05 x V_{CC}	–
Fast-mode plus	0.05 x V_{DD}	–	0.05 x V_{CC}	–
High-speed mode	0.1 x V_{DD}	–	0.05 x V_{CC}	–
Note: V_{CC} and V_{DD} refer to the same voltage in a system.				

Since the I²C standard allows sharing a common I²C bus with mixed I²C-mode devices, a hysteresis specification of 0.05 x V_{DD} is sufficient and will meet the requirement of all I²C slave devices. In addition, the I²C nvSRAM supports an operating voltage range from a minimum of 2.4 V to a maximum of 5.5 V (though not a continuous supply) for which the 5% hysteresis provides a noise margin of 120 mV to 275 mV. This noise margin is added to the device's standard noise margin created by its logic levels. Therefore, the total noise margin becomes sufficiently large enough to protect the I²C nvSRAM from any false trigger. A 10% hysteresis may be only needed when the device operates at a lower operating voltage (V_{DD} < 2.0 V) because at a lower power supply, 5% hysteresis may not be able to provide sufficient noise margin to filter out all unwanted noise components. The I²C nvSRAM currently does not support V_{DD} < 2.0 V.

The I²C nvSRAM 0.05 x V_{CC} hysteresis specifications allows it to operate in any standard I²C system environment. To further explain, the input buffer behavior with Schmitt trigger inputs and glitch filter is illustrated in Figure 1.

Figure 1. The Input Buffer Behavior with Schmitt Trigger Inputs and Glitch Filter



On the rising edge of the input signal, the device is guaranteed to switch between Vpos (min) and Vpos (max). Whereas on the falling edge, the device is guaranteed to switch between Vneg (max) and Vneg (min). The Schmitt trigger input has the switching threshold adjusted such that the part will switch at a higher point (Vpos) on the rising edge and at a lower point (Vneg) on the falling edge. The hysteresis is the delta between where the device switches on the rising edge and where it switches on the falling edge. The max and min hysteresis is calculated using the following two equations.

V_{hys} (min) = (Vpos, min) – (Vneg, max) Equation 1

V_{hys} (max) = (Vpos, max) – (Vneg, min) Equation 2

t_{OF}/t_F (min) – Minimum Output fall time

The NXP I²C standard specifies a minimum fall time for its Fast-mode and Fast-mode plus as 20 x (V_{DD} / 5.5 V) ns and for its High-speed mode as 10 ns for both the output stage buffer (t_{OF}) and the bus timing (t_F) as shown in Table 3. This specification has no effect on the I²C nvSRAM protocol functionality. A faster edge rate of t_{OF}/t_F (output fall time smaller than its minimum spec) may solely affect the EMI on boards where the I²C signals are the fastest switching signals.

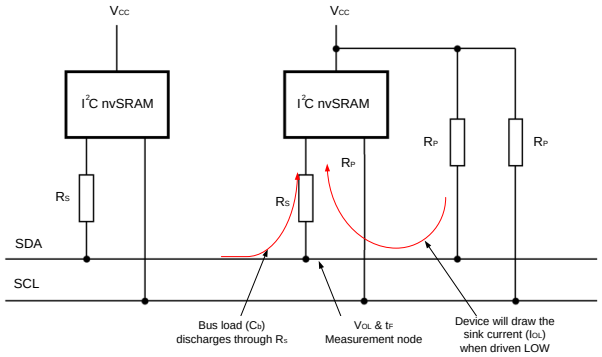
Table 3. Output Fall Time

I²C-bus Mode	Spec	NXP		nvSRAM	
		Min	Max	Min	Max
Standard-mode	t_{OF}	–	250 ns	–	250 ns
	t_F	–	300 ns	–	300 ns
Fast-mode	t_{OF}	20 x (V_{DD} /5.5 V) ns	250 ns	–	250 ns
	t_F	20 x (V_{DD} /5.5 V) ns	300 ns	–	300 ns
Fast-mode Plus	t_{OF}	20 x (V_{DD} /5.5 V) ns	120 ns	–	120 ns
	t_F	20 x (V_{DD} /5.5 V) ns	120 ns	–	120 ns
High-speed Mode	t_F	10 ns	80 ns	–	80 ns

The I²C nvSRAM does not specify minimum values for t_{OF} and t_F parameters. However, based on the system configuration, you can estimate the I²C nvSRAM output fall time value by using the Input/Output Buffer Information Specification (IBIS) model of the device.

The NXP I²C standard suggests using a series resistor (R_s) for protection against high-voltage spikes on the SDA and SCL lines (resulting from the flash-over of a TV picture tube, for example) as shown in Figure 2. Using a series resistor (R_s) adds delay to the output fall time (t_F = t_{OF} + delay (Δt)). Therefore, in a system where t_F is a critical requirement, a series resistor (R_s) between I²C nvSRAM's SDA pin and the system's I²C-bus will slow down the output fall time edge rate and can bring the t_F within the desired limit. Note that the I²C nvSRAM's SCL pin is an input-only pin; therefore, the t_F and t_{OF} specifications are not applicable for this pin.

Figure 2. Using Series Resistor (Rs) For Fall Time Control



If series resistors are used, the additional resistance should be taken into the calculations for R_p and the allowable bus capacitance. In addition, the series resistance (R_s) will increase the net output voltage level to a higher level (V_{OL} + R_s x I_{OL}), which will effectively reduce the noise margin at the receiving device end. The output fall time delay due to the additional R_s can be calculated using Equation 3:

Δt (ps) = 0.8473 x R_s (Ω) x C_b (pf) Equation 3

The total bus fall timing (t_F) can be calculated using Equation 4:

$t_F = t_{OF} + \Delta t$ Equation 4

Summary

The I²C nvSRAM specifications are compliant with the standard I²C-bus specification, except for a few specifications that are standardized across all the supported modes and differ from the NXP I²C-bus specification. These differences will not cause any impact in typical I²C systems.

Document History

Document Title: AN87209 - Overview of nvSRAM I²C I/O Specs Standardized by Cypress across I²C Modes

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3980381	ZSK	04/24/2013	New Spec.
*A	5240169	ZSK	04/25/2016	Updated “Differences between I²C nvSRAM I/O and the NXP I²C-bus Specification”: Updated “tOF/tF (min) – Minimum Output fall time” (for better clarity). Updated to new template.
*B	5848982	HARA	08/16/2017	Updated logo and copyright.

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