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AN84783

Accurate Measurement Using PSoC® 3 and PSoC 5LP Delta-Sigma ADCs

Author: Nidhin M S

Associated Project: Yes

Associated Part Family: PSoC 3 and PSoC 5LP

Software Version: PSoC Creator™3.3 SP2 and higher

For a complete list of the application notes, click here.

More code examples? We heard you.

To access an ever-growing list of hundreds of PSoC code examples, please visit our code examples web page. You can also explore the PSoC video library here.

AN84783 shows how to increase the accuracy of measurements using the 20-bit Delta-Sigma ADC in PSoC 3 and PSoC 5LP. Major topics include effective resolution, gain and offset errors, nonlinearity, and accuracy improvement techniques. A spreadsheet is provided to assist ADC performance analysis and to optimize ADC Component configuration.

Contents

1 Introduction

Accurate measurement of physical quantities is important for many applications. In most measurement systems, you use a transducer to convert a physical quantity to a voltage. This voltage is sent through signal conditioning circuitry, if necessary, and then to an analog-to-digital converter (ADC).

PSoC® 3 and PSoC 5LP integrate the signal-conditioning circuitry, ADC, microcontroller, and other peripherals (such as I^2C, Segment LCD, PWM, and so on) into a single chip. You can easily create high-precision analog systems using the integrated, highly configurable, 20-bit Delta-Sigma ADC.

The accuracy of an overall measurement system depends on the accuracy of its components: the transducer, the PCB and its layout, the noise in the environment, the signal processing circuitry, and the ADC. This application note focuses on those portions of the system that are within PSoC—the signal-processing circuitry and the ADC. It describes how to configure the PSoC Delta-Sigma ADC for maximum accuracy. A spreadsheet tool is provided with this application note to assist with ADC performance analysis and optimizing ADC Component configuration.

2 Using this Document

If you are familiar with PSoC 3, PSoC 5LP, and developing applications using PSoC Creator™, you can jump right in and quickly read this application note starting from section 6 ADC Parameters.

If you are new to these products, see AN54181 – Getting Started with PSoC 3 or AN77759 – Getting Started with PSoC 5LP. In addition, sections 2, 3 and 4 give a comprehensive list of resources to learn more about PSoC and PSoC Creator.

For more Delta-Sigma ADC code examples, see section 5.

3 PSoC Resources

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and quickly and effectively integrate the device into your design. For a comprehensive list of resources, see KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP. The following is an abbreviated list for PSoC 5LP:

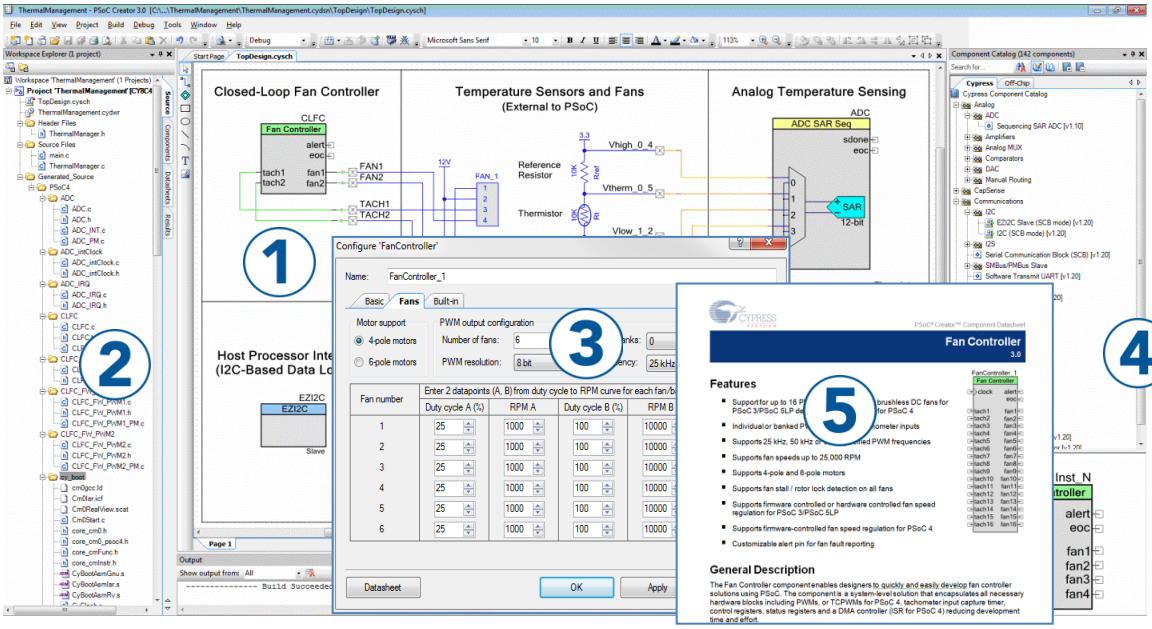
- **Overview:** PSoC Portfolio, PSoC Roadmap
- **Product Selectors:** PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP. In addition, PSoC Creator includes a device selection tool.
- **Datasheets** describe and provide electrical specifications for the PSoC 3, PSoC 4, and PSoC 5LP device families.
- **CapSense® Design Guides:** Learn how to design capacitive touch-sensing applications with the PSoC 3, PSoC 4, and PSoC 5LP families of devices.
- **Application Notes** and **Code Examples** cover a broad range of topics, from basic to advanced level. Many of the application notes include code examples.
- **Technical Reference Manuals (TRM)** provide detailed descriptions of the architecture and registers in each of the PSoC 3, PSoC 4, and PSoC 5LP device families. **PSoC Training Videos:** These videos provide step-by-step instructions on how to get started building complex designs with PSoC.
- **Development Kits:**
  - CY8CKIT-050 is a PSoC 5LP kit designed for analog performance. It enables you to develop and evaluate high-precision analog, low-power, and low-voltage applications.
  - CY8CKIT-030 is a PSoC 3 kit designed for analog performance. It enables you to develop and evaluate high-precision analog, low-power, and low-voltage applications.

4 PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of systems based on PSoC 3, PSoC 4, and PSoC 5LP. See Figure 1 – with PSoC Creator, you can:

1. Drag and drop Components for hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware
3. Configure Components using configuration tools
4. Explore the library of 100+ Components
5. Review Component datasheets

Figure 1. PSoC Creator Features



4.1 PSoC Creator Help

Visit the PSoC Creator home page to download the latest version of PSoC Creator. Then, launch PSoC Creator and navigate to the following items:

- **Quick Start Guide:** Choose the menu item **Help** > **Documentation** > **Quick Start Guide**. This guide gives you the basics for developing PSoC Creator projects.
- **Simple Component example projects:** Choose the menu item **File** > **Open** > **Example projects**. These example projects demonstrate how to configure and use PSoC Creator Components.
- **Starter designs:** Choose the menu item **File** > **New** > **Project** > **PSoC 5LP Starter Designs**. These starter designs demonstrate the unique features of PSoC 5LP. Similarly, choose **File** > **New** > **Project** > **PSoC 3 Starter Designs** for a list of PSoC 3 starter designs.
- **System Reference Guide**: Choose the menu item **Help** > **System Reference** > **System Reference Guide**. This guide lists and describes the system functions provided by PSoC Creator.
- **Component datasheets:** Right-click a Component and select “Open Datasheet.”. Visit the PSoC 5LP Component Datasheets page or PSoC 3 Component Datasheets page for a list of all component datasheets.
- **Document Manager:** PSoC Creator provides a document manager to help you to easily find and review document resources. To open the document manager, choose the menu item **Help** > **Document Manager**.

4.2 Technical Support

If you have any questions, our technical support team is happy to assist you. You can create a support request on the Cypress Technical Support page.

If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 8 at the prompt.

You can also use the following support resources if you need quick assistance.

- Self-help
- Local Sales Office Locations

5 Code Examples

PSoC Creator includes a large number of code example projects. These projects are available from the PSoC Creator Start Page, as Figure 2 shows.

Example projects can speed up your design process by starting you off with a complete design, instead of a blank page. The example projects also show how PSoC Creator Components are used in various applications. Code examples and datasheets are included, as Figure 3 shows.

In the Find Example Project dialog shown in Figure 3, you have several options:

- Filter for examples based on architecture or device family, i.e., PSoC 3, PSoC 4, or PSoC 5LP; category; or keyword.

  For example, select “PSoC 5LP” as Device Family and filter by “ADC_DelSig” to get a list of PSoC 5LP Delta-Sigma ADC code examples, as Figure 3 shows.
- Select from the menu of examples offered based on the Filter Options
- Review the datasheet for the selection (on the **Documentation** tab)
- Review the code example for the selection. You can copy and paste code from this window to your project, which can help speed up code development, or
- Create a new project (and a new workspace if needed) based on the selection. This can speed up your design process by starting you off with a complete, basic design. You can then adapt that design to your application.

Figure 2. Code Examples in PSoC Creator

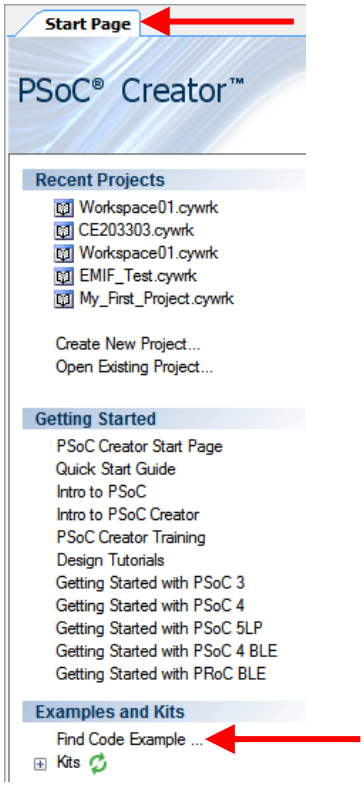
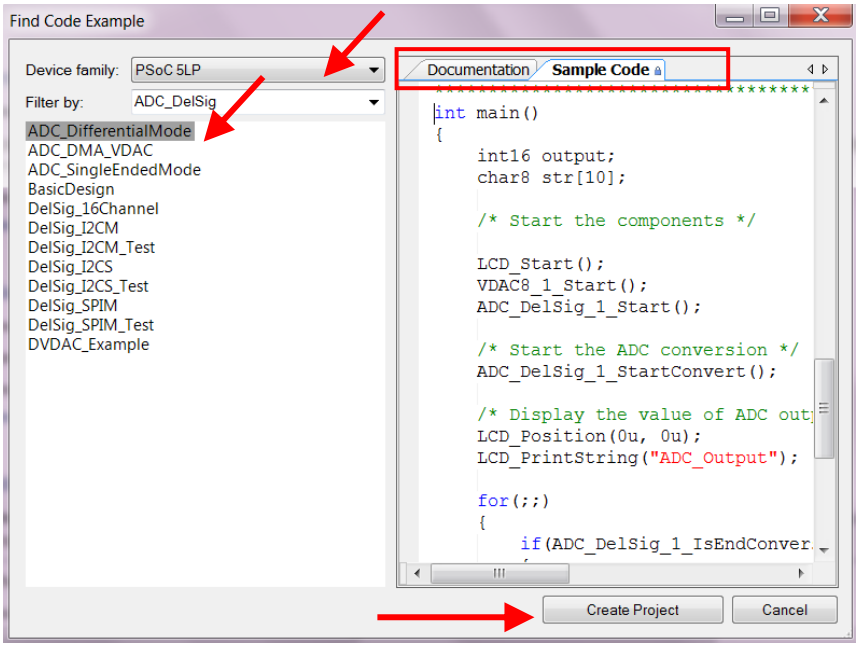


Figure 3. Code Example Projects, with Sample Code



6 ADC Parameters

This section describes various Delta-Sigma ADC parameters and how they affect measurement accuracy. Table 1 shows a summary of these parameters. For a complete list of Delta-Sigma ADC specifications, see the Delta-Sigma ADC Component datasheet.

Table 1. Delta-Sigma ADC Parameters

Parameter	Condition	Max Value	
		PSoC 3	PSoC 5LP
Maximum resolution		20 bits	20 bits
Offset error	Buffered, 16-bit mode, 25 °C	±0.1 mV	±0.2 mV
Gain error	Range = ±1.024 V, buffered, buffer gain = 1, 16-bit mode, 25 °C	±0.2 %	±0.4 %
Differential nonlinearity	Range = ±1.024 V, unbuffered, 16-bit mode	±1 LSB	±1 LSB
Integral nonlinearity	Range = ±1.024 V, unbuffered, 16-bit mode	±2 LSB	±2 LSB
Common-mode rejection ratio	Range = ±1.024 V, buffered, buffer gain = 1, 16-bit mode	85 dB	85 dB
Power-supply rejection ratio	Range = ±1.024 V, buffered, buffer gain = 1, 16-bit mode	90 dB	90 dB

6.1 Resolution

The resolution of an ADC is the number of discrete digital values (numbers or counts) that it can produce over the analog input range. It is expressed in bits. An ADC with a resolution of 'n' bits can encode an analog input to one of 2^n different counts.

Resolution can also be expressed as the minimum voltage that can be resolved by the ADC. This term is known as voltage resolution. The voltage resolution of an ADC is given by Equation 1.

$$\text{Voltage resolution} = \frac{\text{Input voltage range}}{2^n} \qquad (1)$$

where n is the ADC's resolution in bits.

The PSoC Delta-Sigma ADC can achieve a resolution as high as 20 bits. If the input voltage range is ±1.024 V (the default for this ADC), the voltage resolution is given by Equation 2.

$$\text{Voltage resolution} = \frac{2.048}{2^{20}} = 1.96\ \mu V \qquad (2)$$

The ideal (perfect) voltage resolution of the PSoC Delta-Sigma ADC for a range of ±1.024 V is given in Table 2.

Having many bits of resolution does not always mean that all of the bits are usable. In practice, when you do continuous measurements of the same input voltage at high resolutions, the last few bits flicker due to the presence of noise. So a 20-bit ADC with a noisy amplifier front end no longer has a 20-bit resolution—the resolution is limited by the amplifier noise. A high-resolution application needs a high-resolution system and not just a high-resolution ADC. The estimated level (RMS value) of the noise gives the useful resolution of the ADC.

Table 2. Ideal ADC Voltage Resolution, Range = ±1.024 V

Bits	Ideal voltage resolution	Unit
8	8.0	mV
9	4.0	mV
10	2.0	mV
11	1.0	mV

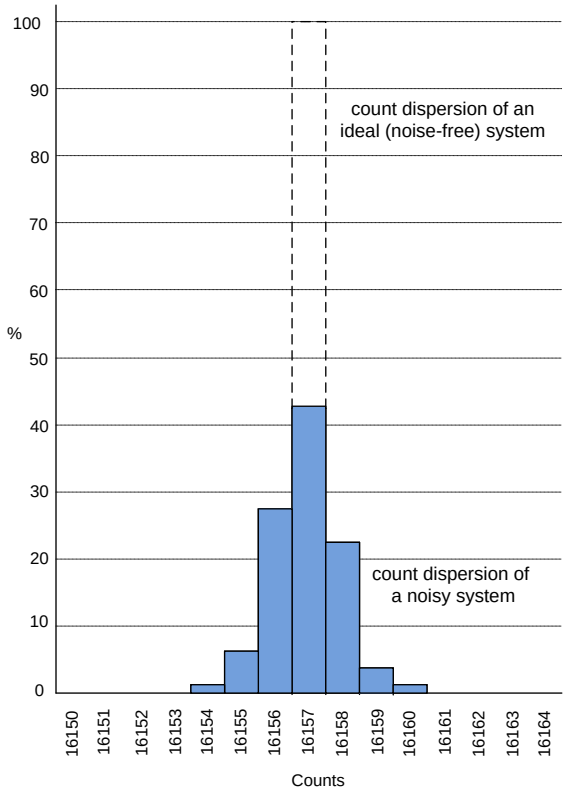
Bits	Ideal voltage resolution	Unit
12	0.5	mV
13	0.25	mV
14	125.0	µV
15	62.5	µV
16	31.3	µV
17	15.6	µV
18	7.8	µV
19	3.9	µV
20	2.0	µV

You can use Table 2 and the estimated system noise level to determine the effective number of bits (ENOB, also known as effective resolution). If the ADC ideal voltage resolution is greater than the noise level, then the ADC can operate at its specified number of bits. For example, if the noise level is 10 µV and the ADC is operating at 16 bits, the noise level is less than the ideal resolution and the ADC can in fact operate at 16 bits. However, if the ADC is operating at 20 bits, the effective resolution is actually between 17 and 18 bits.

6.2 Effective Resolution

The previous examples show that to determine the effective resolution (ENOB) of an ADC you need to know the system noise level. A simple way to measure the noise is to determine the dispersion of the output counts of the ADC. Measure a constant voltage many times and make a histogram of the ADC output count dispersion, as Figure 4 shows.

Figure 4. Example of ADC Count Dispersion at 16-Bit Resolution



The RMS value of the system noise level in counts is given by the standard deviation (σ) of the ADC's output counts. The RMS noise in counts is converted to RMS noise in volts by Equation 3.

$$\text{RMS noise in volts} = \frac{\sigma * \text{ADC input range in volts}}{2^n} \quad (3)$$

where n is the ADC's resolution in bits.

Then, you can get the ENOB from Equation 4.

$$\text{ENOB} = \text{Log}_2\left(\frac{\text{ADC input range in volts}}{\text{RMS noise in volts}}\right) \quad (4)$$

ENOB is a commonly used parameter to indicate ADC system performance, but it does not necessarily show the number of bits that do not flicker. To obtain the number of stable (flicker-free—bits), use peak-to-peak resolution instead.

6.3 Peak-to-Peak Resolution

Peak-to-peak resolution is obtained from peak-to-peak noise. The difference between the maximum and minimum ADC counts across many measurements of a constant voltage input gives the peak-to-peak noise counts (p). Use Equation 5 to determine the peak-to-peak noise voltage from the peak-to-peak noise counts (p).

$$\text{Peak to peak noise voltage} = \text{Log}_2\left(\frac{\text{ADC input range}}{\text{p}}\right) \quad (5)$$

Then you can get peak-to-peak resolution from Equation 6.

$$\text{Peak to peak resolution} = \text{Log}_2\left(\frac{\text{ADC input range}}{\text{Peak to peak noise}}\right) \quad (6)$$

Signal-to-noise ratio (SNR) is another measure of signal chain performance. SNR is the ratio of RMS signal power to RMS noise power. For a constant (DC) voltage input, SNR is calculated as the ratio of maximum input voltage and RMS noise voltage, as Equation 7 shows.

$$\text{SNR} = \frac{\text{Maximum input voltage}}{\text{RMS noise voltage}} \quad (7)$$

SNR is often expressed in decibels, as Equation 8 shows.

$$\text{SNR}_{\text{dB}} = 10\ \text{Log}_{10}\left(\frac{\text{Maximum input voltage}}{\text{RMS noise voltage}}\right) \quad (8)$$

6.4 Offset Error

The input offset voltage of the ADC causes a measurement error known as offset error. For example, Figure 5 shows the transfer characteristics of an ideal ADC and an ADC with an offset error. The red line indicates the characteristics of an 8-bit ADC operating with an input voltage range of 0 to 1.024 V with an offset of 32 mV.

The offset error causes a fixed additive error in all measurements. It also causes a shift in the ADC input voltage range. For example, the 32-mV offset shown in Figure 5 brings the maximum input voltage down from 1.024 V to 992 mV.

You can get the offset of the ADC by measuring the ADC output value for a zero input voltage.

Figure 5. Offset Error

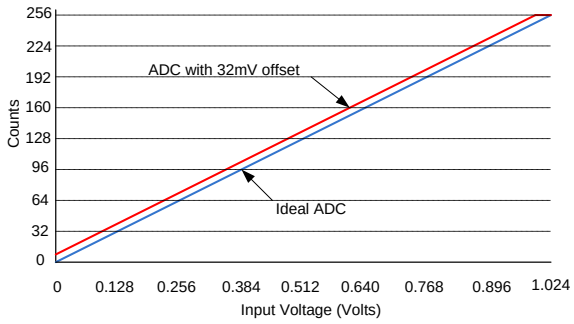


Table 1 on page 5 shows the maximum offset voltages of Delta-Sigma ADCs in PSoC 3 and PSoC 5LP.

6.5 Gain Error

Gain error is the deviation of the ADC characteristics from the ideal slope of the ADC transfer function. Equation 9 gives the ideal ADC transfer function.

$$\text{Voltage} = \text{ADC count} * \left(\frac{\text{ADC voltage range}}{2^n}\right) \quad (9)$$

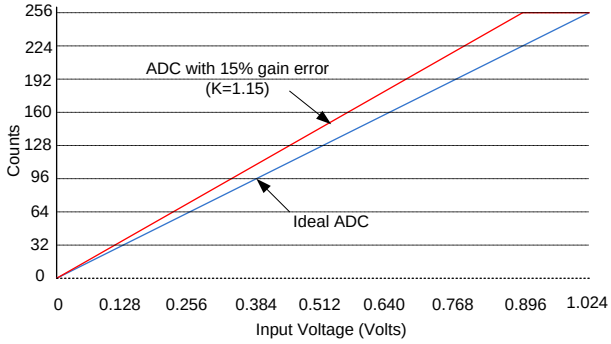
where n is the ADC's resolution in bits.

Any multiplicative factor 'K' causes a gain error, as Equation 10 shows.

$$\text{Voltage} = \text{ADC count} * \left(\frac{\text{ADC voltage range}}{2^n}\right) * K \quad (10)$$

Figure 6 shows a plot of Equations 9 and 10 for an 8-bit ADC measurement with an input range of 0 to 1.024 V.

Figure 6. Gain Error



The blue line shows the ideal transfer characteristics, and the red line shows the characteristics with a gain error of 15 percent (K = 1.15).

Equation 11 gives the combined transfer function of an ADC with gain and offset errors.

$$\text{Voltage} = \left(\text{ADC count} * \left(\frac{\text{ADC voltage range}}{2^n}\right) * K\right) + \text{offset} \quad (11)$$

Figure 7 shows a plot of the combined transfer function.

Figure 7. Combined ADC Transfer Function

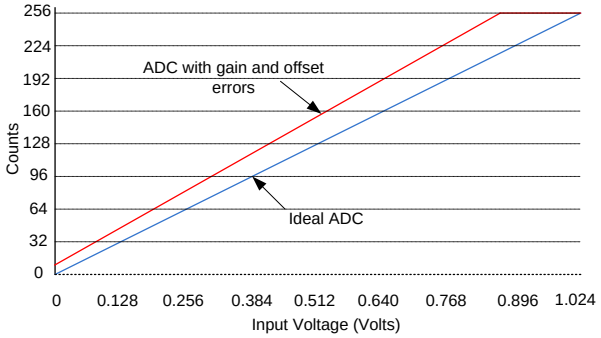


Table 1 on page 5 shows the maximum gain errors of Delta-Sigma ADCs in PSoC 3 and PSoC 5LP.

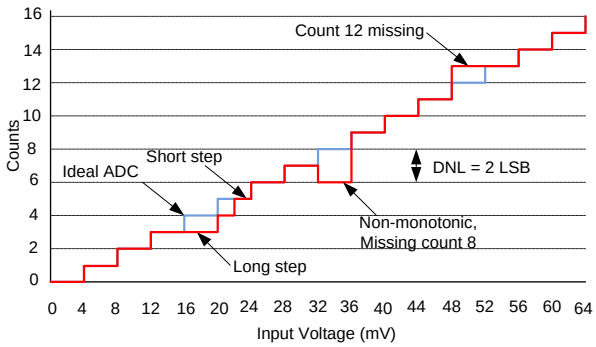
You can reduce the gain and offset errors by calibrating the ADC. See Offset and Gain Calibration for more details.

6.6 Differential Nonlinearity Error

When the input voltage changes from one voltage level to the next adjacent level, an ideal ADC steps up or down one LSB without skipping a count or holding the same count. Differential nonlinearity (DNL) error describes the maximum deviation from the ideal step size of 1 LSB between ADC counts corresponding to two adjacent input analog levels across the entire input range.

DNL errors can cause inaccurate count values at specific analog input levels. DNL is a function of the ADC architecture and is difficult to calibrate. Figure 8 shows an example of ADC characteristics with DNL.

Figure 8. DNL Example

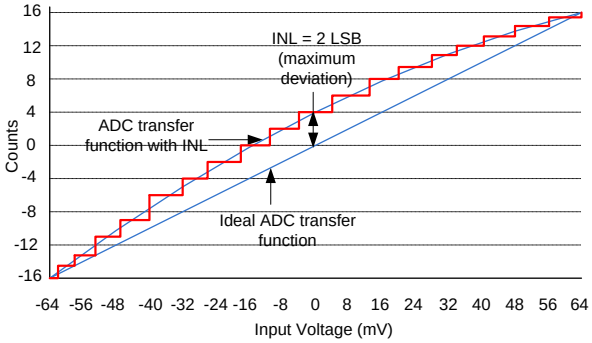


6.7 Integral Nonlinearity Error

When DNL errors add up, they create an integral nonlinearity (INL) error. An INL error is a measure of the worst case deviation of the ADC transfer function from the ideal ADC transfer function.

Figure 9 shows an example of an ideal ADC output (blue line) and an ADC with INL (red line).

Figure 9. INL Example



6.8 Common-Mode Rejection Ratio

When the ADC is in differential mode, the ADC input voltage is the difference between the voltages on two inputs: + input and – input. The common-mode rejection ratio (CMRR) of an ADC in differential mode is the ability of the ADC to filter out the input signals that are common to both inputs.

In most applications, the relevant information is contained in the voltage difference between two differential inputs, and the noise is common to both terminals. Therefore, an ADC with high CMRR rejects the noise common to both terminals while preserving the relevant differential signal information.

CMRR is often expressed in decibels, as Equation 12 shows.

$$\mathrm{CMRR_{dB}} = 20\ \mathrm{Log_{10}}\left(\frac{\mathrm{A_{DM}}}{\mathrm{A_{CM}}}\right) \qquad (12)$$

where A_{DM} is the gain of the differential mode signals and A_{CM} is the gain of the common-mode signals.

6.9 Power Supply Rejection Ratio

Power supply rejection ratio (PSRR) describes the amount of noise from the power supply that an ADC can reject. In a practical ADC, a change in power supply voltage may cause a change in the ADC's output counts. This change in output counts is generally seen as an input voltage change produced by the power supply voltage change.

PSRR is calculated as the ratio of the change in supply voltage to the corresponding change in the (differential) ADC input voltage. It is often expressed in decibels, as Equation 13 shows.

$$\mathrm{PSRR_{dB}} = 20\ \mathrm{Log_{10}}\left(\frac{\text{Change in supply voltage}}{\text{Change in input voltage}}\right) \qquad (13)$$

7 How to Achieve High Accuracy

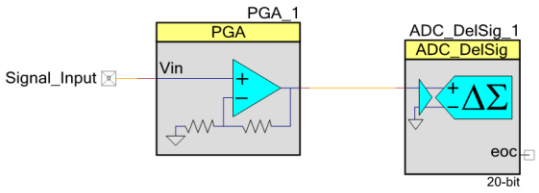
This section explains different techniques to improve the accuracy of ADC measurements.

7.1 Analog Signal Chain Selection

The accuracy of ADC measurements depends not only on the ADC but also on the front-end analog system. If analog front-end components have a lower accuracy than the ADC, they determine the overall measurement accuracy.

First, look at an example of poor signal chain selection. Figure 10 shows a signal chain in which a Programmable Gain Amplifier (PGA) Component is used to amplify the input voltage of a Delta-Sigma ADC.

Figure 10. Signal Chain Example



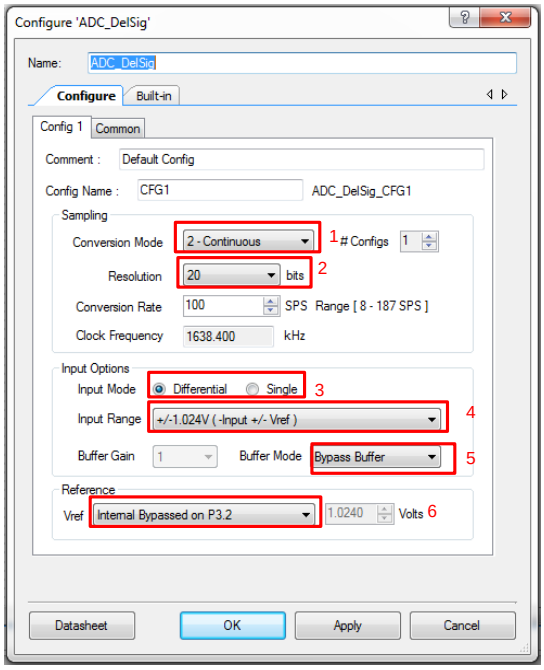
The PSoC 3 and PSoC 5LP PGA has an input offset voltage of 10 mV, a gain error of ±2.5 percent (at a gain of 16), a DC output nonlinearity of ±0.01 percent for the full-scale range, and a PSRR of 48 dB. Even though the ADC has significantly better specifications, the overall system performance is limited by the PGA. Therefore, this setup is not recommended for high-precision measurements.

Similarly, if you use one of the PSoC Opamp Components as a front-end amplifier, the Opamp specifications dictate the overall system performance. Instead, you should use the built-in input buffer of the Delta-Sigma ADC, which provides high impedance as well as a gain of 1, 2, 4, or 8. See the next section to know how to configure the ADC input buffer.

7.2 Configuring the ADC for High Accuracy

Figure 11 shows a configuration of the Delta-Sigma ADC Component for high accuracy.

Figure 11. ADC Configuration



In this example, the ADC is configured for a continuous sampling rate of 100 sps. For 20-bit continuous sampling, sample rates from 8 to 187 samples per second are possible.

Set other configuration parameters as follows:

1. Conversion Mode: Select this mode for continuous conversion if you have a single input channel. Do not use this mode when multiple signals are multiplexed and measured with a single ADC. If you have multiple input channels, you should use Multi-Sample or Multi-Sample (Turbo) mode. See the Delta-Sigma ADC Component datasheet to learn how to use these modes.
2. Resolution: Select the maximum value of 20 bits for high-precision applications.
3. Input Mode: Select differential input mode to improve CMRR and reduce external noise that is common to both input terminals.
4. Input Range: Select the delta-sigma modulator gain. Table 3 lists differential ranges and the corresponding gains.

Table 3. ADC Modulator

Input Range	Modulator Gain
Input ± 6 * Vref	0.167
Input ± 2 * Vref	0.5
Input ± Vref	1
Input ± 0.5 * Vref	2
Input ± 0.25 * Vref	4
Input ± 0.125 * Vref	8
Input ± 0.0625 * Vref	16

When the Input ± Vref range is selected, the delta-sigma modulator operates at unity gain. This configuration yields the highest accuracy; it uses the internal 1.024-V reference. As the delta-sigma modulator gain increases, the gain error also increases.

5. Buffer Mode: The Delta-Sigma ADC has a built-in buffer that gives gain and high input impedance to the ADC. You should use this buffer if your input signal requires amplification or impedance matching. If the input source is strong and has low output impedance, then you do not require the high input impedance of the buffer. In that case, you can bypass the buffer to eliminate buffer noise.
6. Reference: The 1.024-V reference yields the best accuracy among the internal references available in PSoC 3 and PSoC 5LP. You can add an external capacitor on port 0[3] or port 3[2] to decrease the reference noise. See the Delta-Sigma ADC Component datasheet for information on selecting a suitable bypass capacitor value.

7.3 Using an External Reference

The accuracy of the ADC measurements also depends on the accuracy of the voltage reference. The internal 1.024-V voltage reference in PSoC 3 and PSoC 5LP has an accuracy of 0.1 percent and a maximum temperature drift of 30 ppm/°C. For most applications, this reference is sufficient.

If you require a higher accuracy, you can connect a high-precision external voltage reference generator such as LM4140 to port 0[3] or port 3[2]. The value of the external reference voltage should be within 0.9 to 1.3 V. Change the "Reference" option in the Component configuration to External Vref and set the value of Vref (see step 6 in the previous ADC configuration).

7.4 Offset and Gain Calibration

You can use calibration techniques to correct any gain error or offset error that varies from one device to another. This can eliminate the gain and offset errors from the entire signal chain.

The Delta-Sigma ADC in PSoC has a post-processing block consisting of gain and offset calibration registers. Calibration can be applied to the ADC by writing the appropriate values into these registers. For more information, see AN68403 – PSoC 3 and PSoC 5LP Analog Signal Chain Calibration.

7.5 Correlated Double Sampling

The offset and gain correction from the previous section is valid at a specific temperature; however, both offset and gain error change with temperature. Correlated double sampling (CDS) can reduce the offset drift with temperature.

CDS is a signal-processing technique that is used to suppress low-frequency (1/f) noise and null any offset. For more information on correlated double sampling, see AN66444 – PSoC 3 and PSoC 5LP Correlated Double Sampling to Reduce Offset, Drift, and Low Frequency Noise.

7.6 Using Filters on ADC Counts

Filtering the output counts of the ADC decreases the noise in the counts, and increases the number of flicker-free bits.

You should use a filter that is suitable for your requirement. For example, if you want 17 flicker-free bits from a 20-bit conversion, use a filter that decreases the peak-to-peak noise to $2^{(20 - 17)} = 8$ counts.

You can use either the digital filter block (DFB) in PSoC 3 and PSoC 5LP or firmware to filter the ADC counts. Firmware filters are commonly used because they are easy to implement. For more information on firmware filters, see AN2099 – PSoC 1, PSoC 3, PSoC 4, and PSoC 5LP Single-Pole Infinite Impulse Response (IIR) Filters.

7.7 PCB Design

Poorly designed printed circuit boards can significantly limit the performance of an ADC-based measurement system. The following is a list of important rules to keep in mind when designing high-precision mixed-signal boards.

1. Consider separate analog and digital supplies.
2. Use four-layer boards with power planes, if possible.
3. Separate analog and digital signals and components on the board, if possible. Designate "Analog" and "Digital" areas of the PCB.
4. Do not run analog signals parallel to clocks or fast digital signals.
5. Keep analog signals close to the ground plane to minimize inductive crosstalk.
6. Use guard traces to isolate analog and digital signals.
7. If analog and digital signals must cross, make the intersection at 90 degrees to minimize coupling capacitance. Keep bypass capacitors as close to ICs as possible. Also, make sure that bypass connections to power signals are low-impedance. Avoid long traces into a high-impedance input, as they act as antennas.

For more details, see AN57821 – PSoC 3, PSoC 4, and PSoC 5LP Mixed Signal Circuit Board Layout Considerations and AN61290 – PSoC 3 and PSoC 5LP Hardware Design Considerations.

8 Example Project: DelSig_Analyzer

This PSoC Creator example project does performance analysis of the PSoC Delta-Sigma ADC. By making many continuous measurements of a constant input voltage, the project calculates several parameters:

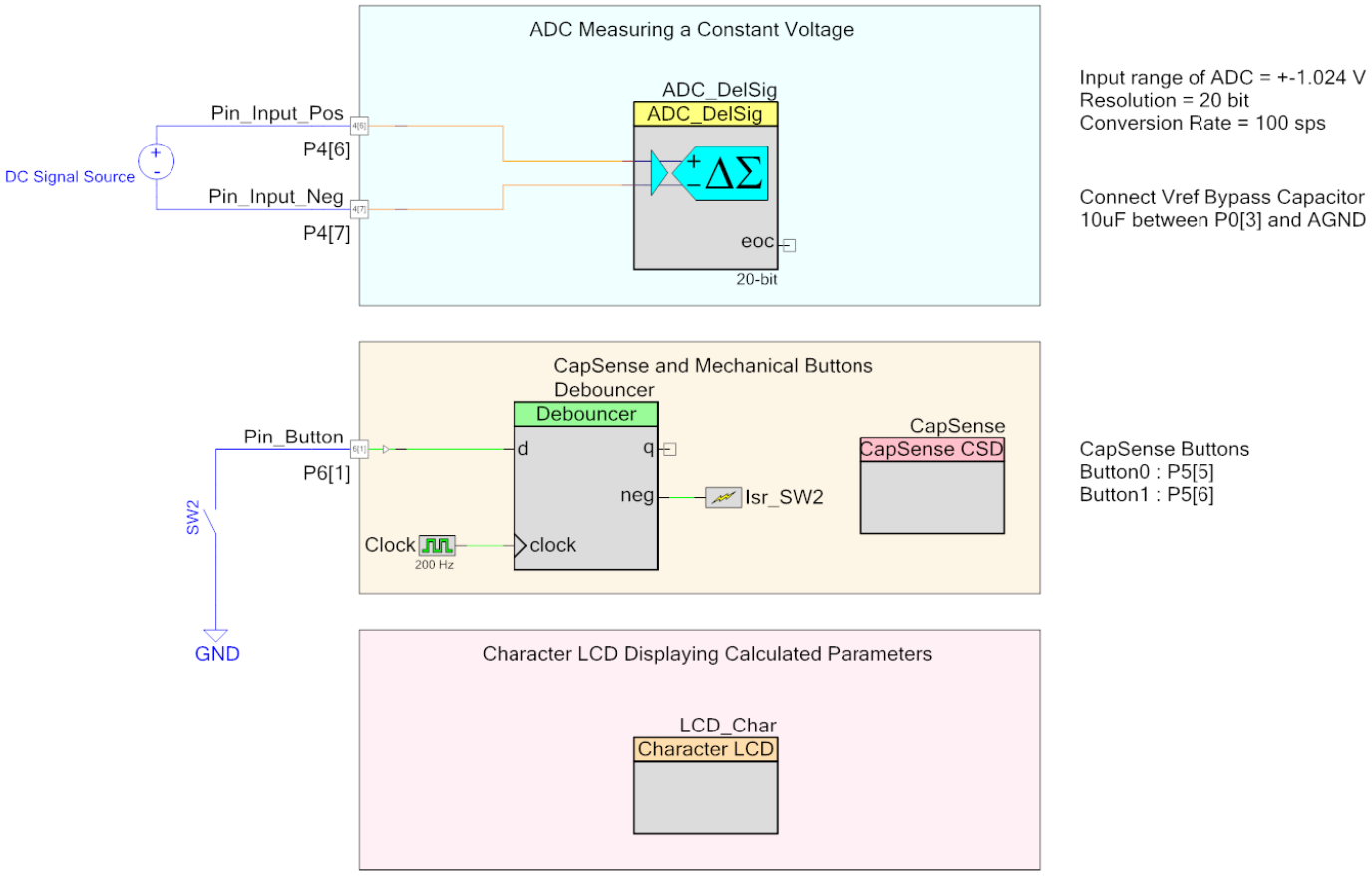
- Mean value of ADC counts
- Mean value of input voltage
- Maximum value of ADC counts
- Maximum value of input voltage
- Minimum value of ADC counts
- Minimum value of input voltage
- Standard deviation in ADC counts
- RMS noise in input voltage
- Peak-to-peak noise in ADC counts
- Peak-to-peak noise in voltage
- ENOB

- Peak-to-peak resolution
- SNR

This project supports the CY8CKIT-030 and CY8CKIT-050 development kits.

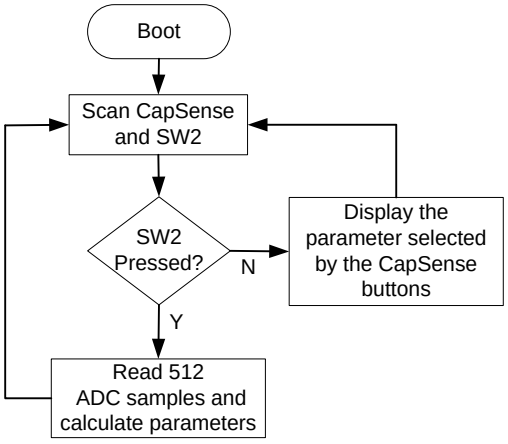
Figure 12 shows the TopDesign schematic of this example project.

Figure 12. Delta-Sigma Analyzer TopDesign



The ADC is configured for a resolution of 20 bits and a sample rate of 100 sps. The CPU calculates the ADC parameters from 512 consecutive ADC samples. The calculated parameters are then displayed on the character LCD. Figure 13 shows the firmware flow for this project.

Figure 13. DelSig_Analyzer Firmware Flow



Follow these steps to view the ADC parameters on the character LCD:

1. Build the project and program the PSoC device.
2. Connect a 10-µF capacitor between pin P0[3] and GND to bypass the internal reference.
3. Make external connections as Figure 12 on page 14 shows. Connect the low-noise, constant voltage source between pins P4[6] (Pin_Input_Pos) and P4[7] (Pin_Input_Neg). Make sure that this voltage is within the ADC's range (±1.024 V).

Note: This project measures the analog performance of your entire signal chain, including the input, board layout, and any other components in front of the ADC. You should make sure that your input voltage is noise-free if you are testing the system performance. DC power supplies and potentiometers are usually very noisy. You can use a low-noise, precision voltage reference IC to generate the input voltage. In this case, make sure that the noise level of the reference is well below the noise floor of the system.

4. Press SW2 on the development kit to start the ADC conversion and calculation of parameters. The LCD shows the message "Reading Samples, Please Wait" until calculations are finished.
5. Use the CapSense® buttons on the development kit to toggle the ADC parameter displays. The parameter menu is arranged in the following order.
    - Mean value of ADC counts
    - Mean value of input voltage
    - Maximum value of ADC counts
    - Maximum value of input voltage
    - Minimum value of ADC counts
    - Minimum value of input voltage
    - Standard deviation in ADC counts
    - RMS noise in input voltage
    - Peak-to-peak noise in ADC counts
    - Peak-to-peak noise in voltage
    - ENOB
    - Peak-to-peak resolution
    - SNR
6. Try repeating the analysis with different voltage sources or ADC Component configurations.

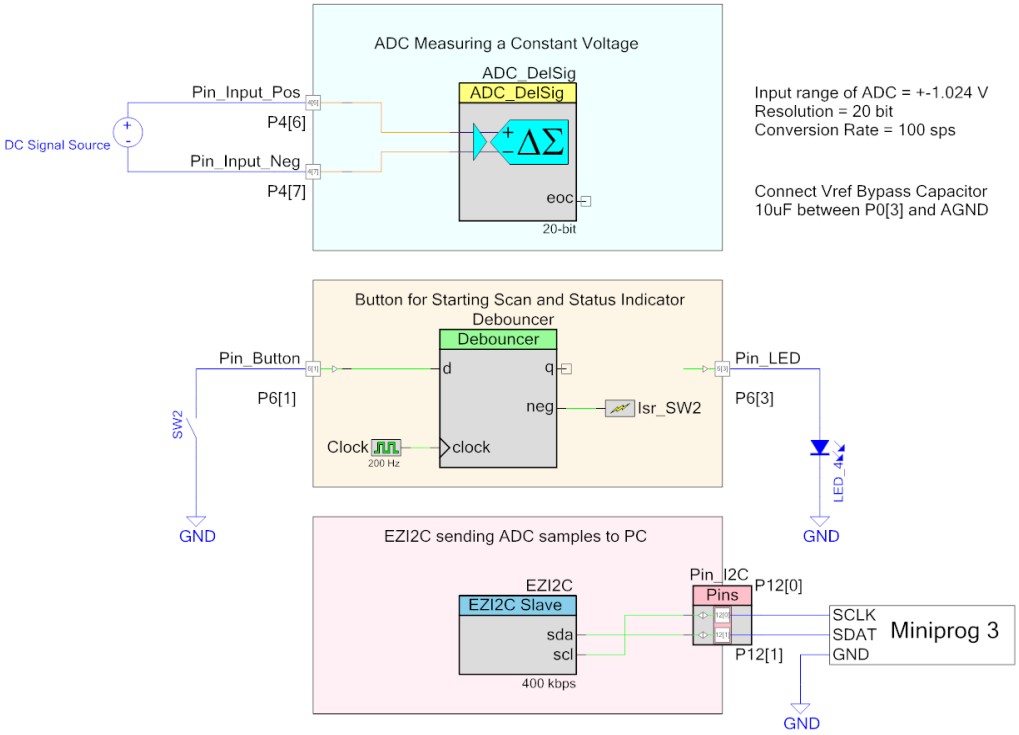
You can easily adapt this project to test the performance of your hardware design.

If your PCB does not have any CapSense buttons, edit the project and replace the CapSense buttons with mechanical buttons. If you do not have a character LCD in your design, you can send the calculated ADC parameters through I^2C or UART and view them using a PC.

9 Example Project: DelSig_I2C

This example project, together with the ADC Performance Analyzer Spreadsheet included with this application note, calculates the same parameters as those in Example Project: DelSig_Analyzer. You can also view the ADC count noise and ADC count dispersion (histogram) using the spreadsheet. Figure 14 shows the TopDesign schematic of this example project.

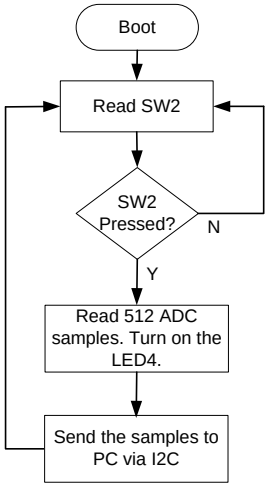
Figure 14. DelSig_I2C TopDesign



The ADC is configured for a resolution of 20 bits and a sample rate of 100 sps. This project buffers 512 consecutive ADC samples in RAM and then sends them to the PC through the I^2C interface and the MiniProg3. You can then use the ADC Performance Analyzer Spreadsheet to calculate the required parameters.

Figure 15 shows the firmware flow of this project.

Figure 15. DelSig_Analyzer Firmware Flow



9.1 ADC Performance Analyzer Spreadsheet

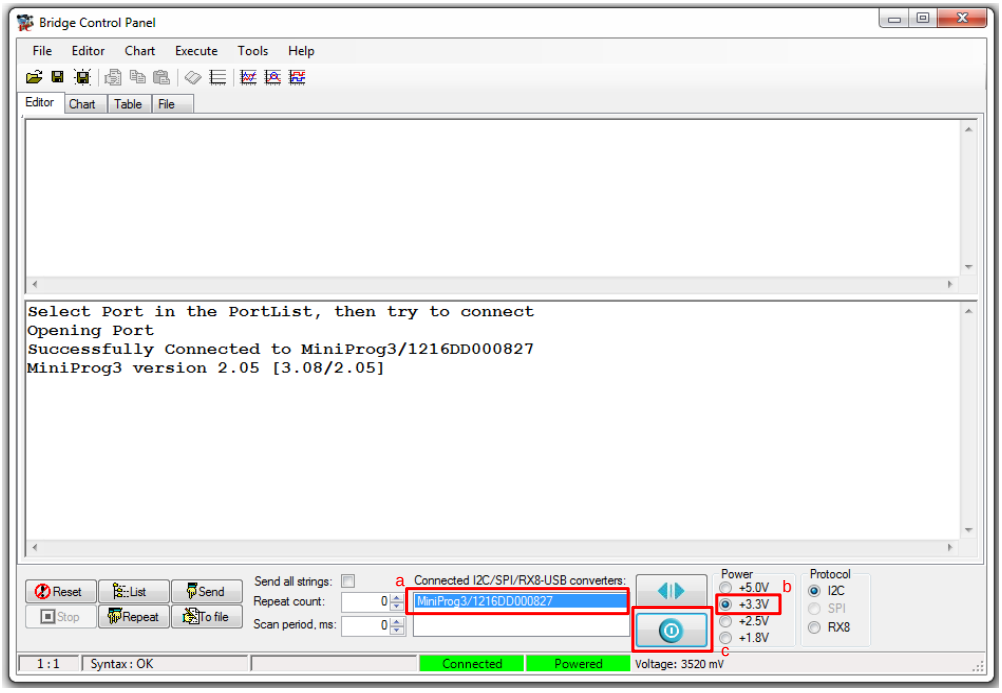
A CY8CKIT-030 or CY8CKIT-050, and a MiniProg3, are required to use this spreadsheet. Follow these steps:

1. Program the CY8CKIT-030 or CY8CKIT-050 with the example project DelSig_I2C.
2. Connect a 10-µF capacitor between pin P0[3] and GND to bypass the internal reference.
3. Make external connections as Figure 14 on page 16 shows. Connect a low-noise, constant voltage source to pins P4[6] (Pin_Input_Pos) and P4[7] (Pin_Input_Neg). Make sure that this voltage is within the ADC's range (±1.024 V).

   Note: This project measures the analog performance of your entire signal chain, including the input, board layout, and any other components in front of the ADC. You should make sure that your input voltage is noise free if you are testing the system performance. DC power supplies and potentiometers are usually very noisy. You can use a low-noise, precision voltage reference IC to generate the input voltage. In this case, make sure that the noise level of the reference is well below the noise floor of the system.
4. Press SW2 on the development kit to start ADC data buffering. LED4 on the development kit turns on when the acquisition is complete.
5. Connect the SDA (P12[1]), SCL (P12[0]), and GND pins to the SDAT, SCLK, and GND terminals of the MiniProg3.
6. Connect the MiniProg3 to the PC using a USB cable.
7. Open the Bridge Control Panel (**Start** > **All Programs** > **Cypress** > **Bridge Control Panel**), select the MiniProg3 from the connected devices (a), set the proper voltage (b), and toggle the power (c), as Figure 16 shows.

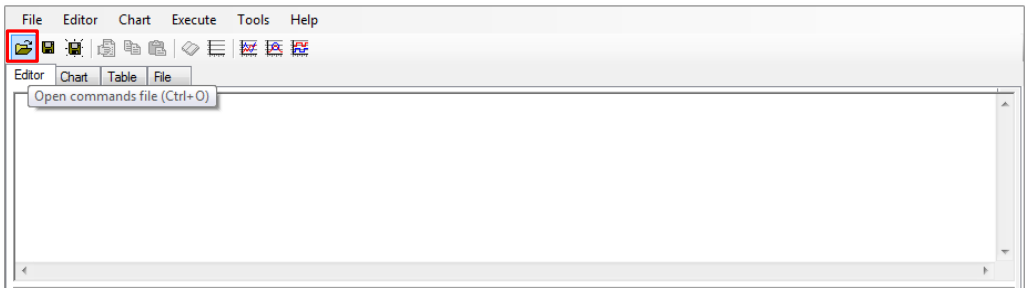
   The Bridge Control Panel software enables you to view data collected from various communication protocols. The PSoC Creator installer automatically installs this tool along with PSoC Creator.

Figure 16. Powering the MiniProg3



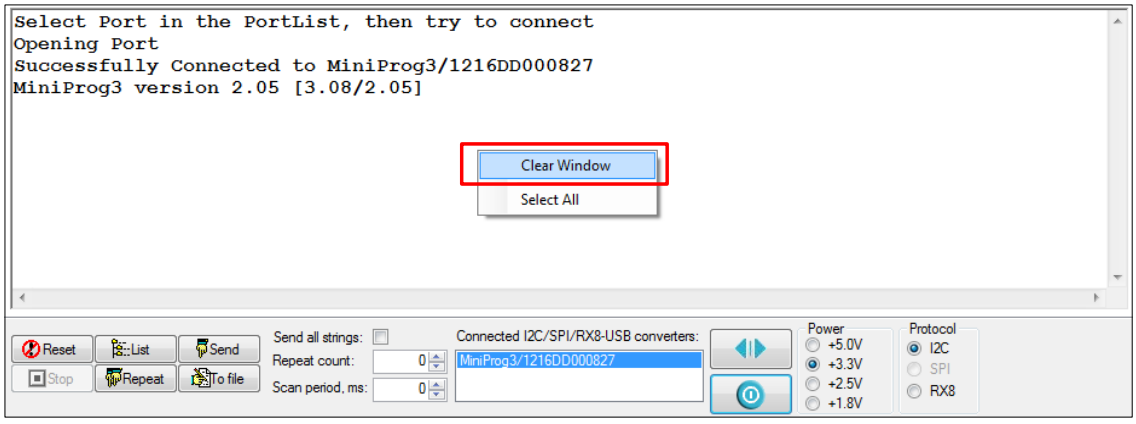
8. In Bridge Control Panel, click the "Open commands file" button, as Figure 17 shows. Then select the *BridgeControlPanel_Script.iic* file associated with this application note and click **OK**.

Figure 17. Opening Command File



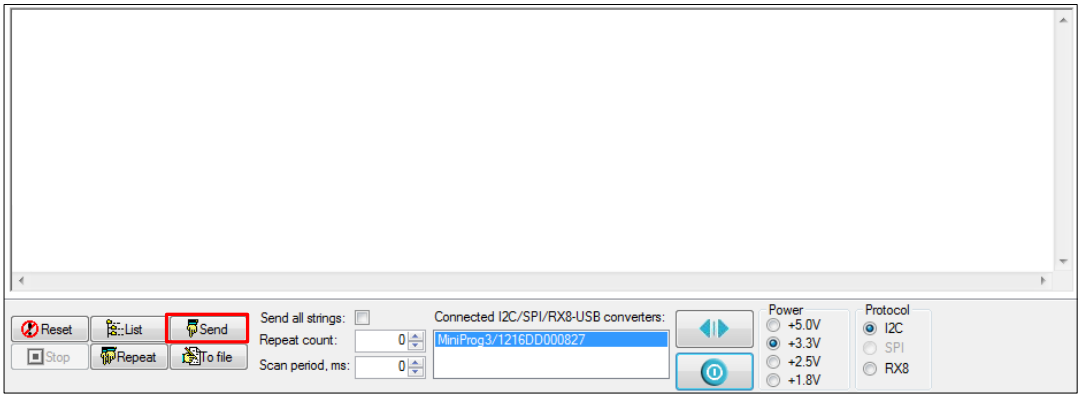
9. Right-click on the status window and select the "Clear Window" option, as Figure 18 shows.

Figure 18. Read ADC Data



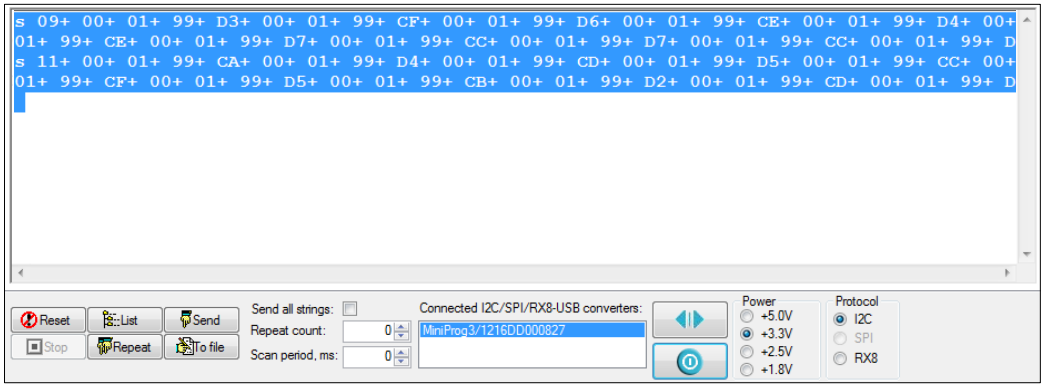
10. Click **Send** in the Bridge Control Panel, as Figure 19 shows, to read the buffered ADC data from the PSoC device.

Figure 19. Read ADC Data



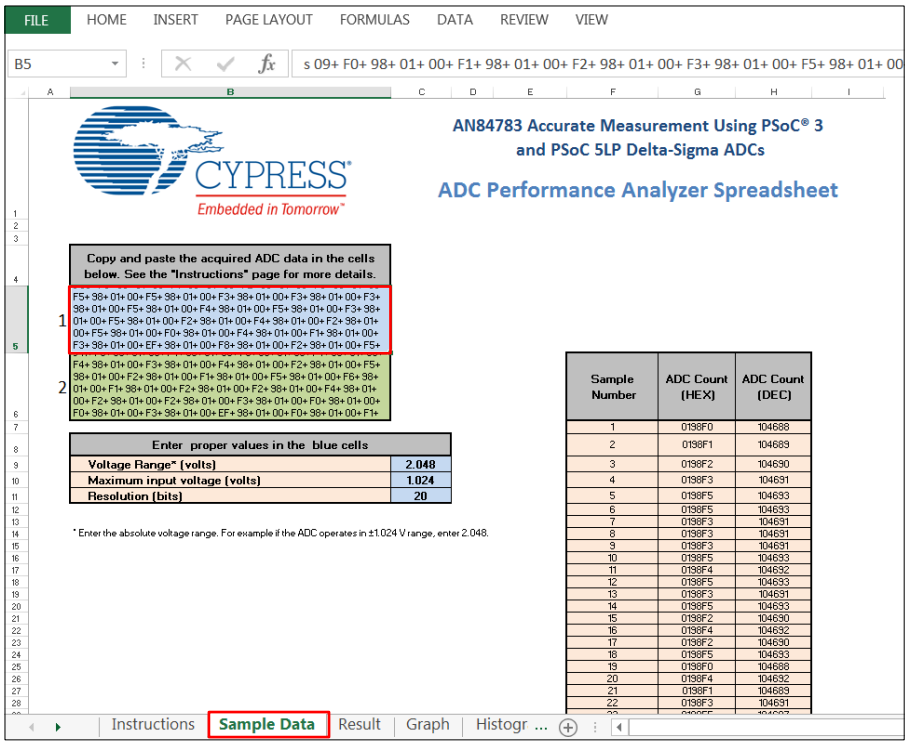
11. After the Bridge Control Panel reads the ADC counts from the PSoC device, the status window shows the ADC data as ASCII characters. Select all of these characters (you can click at the beginning of the first line and drag down, as Figure 20 shows), and then press [**Ctrl**] [**C**] to copy the data.

Figure 20. Copying Acquired Data



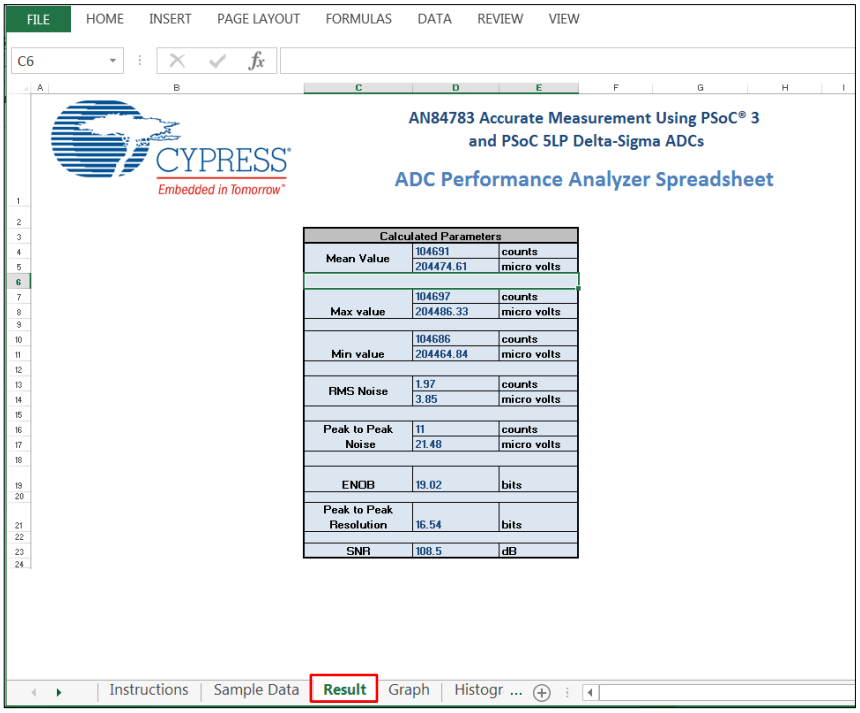
12. Open the ADC Performance Analyzer Spreadsheet, go to the "Sample Data" tab, single-click on the cell highlighted in Figure 21, and paste the data copied from the Bridge Control Panel (press [**Ctrl**] [**V**]).

Figure 21. Entering Data into Spreadsheet Tool



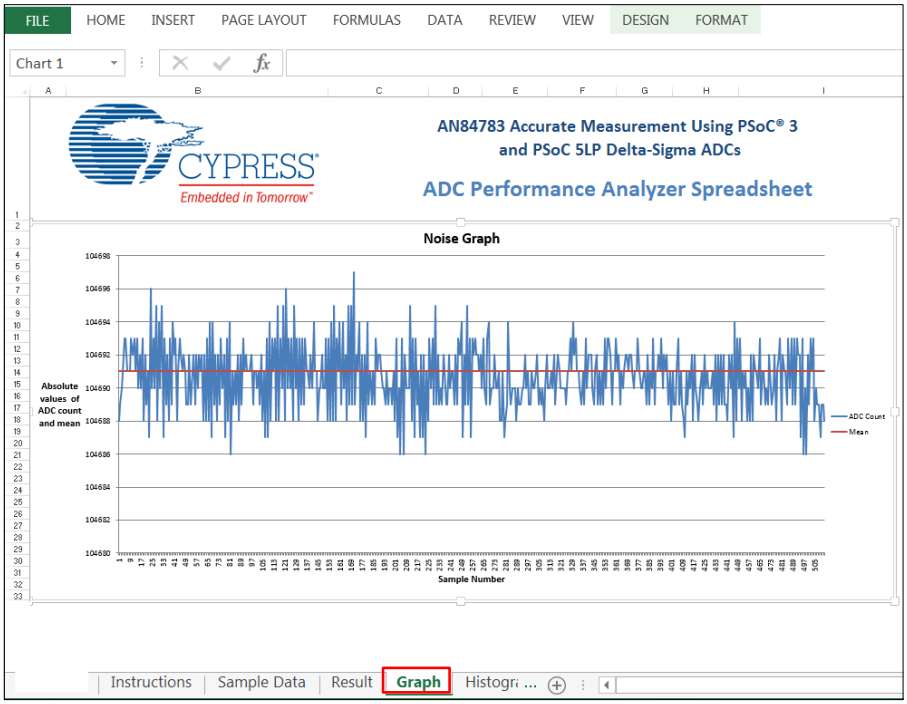
13. If you have made changes to the example project, edit the values of Voltage Range, Maximum input voltage, and Resolution. Otherwise keep the default values.
14. Go to the "Results" page to view the ADC parameters, as Figure 22 shows.

Figure 22. Results Page



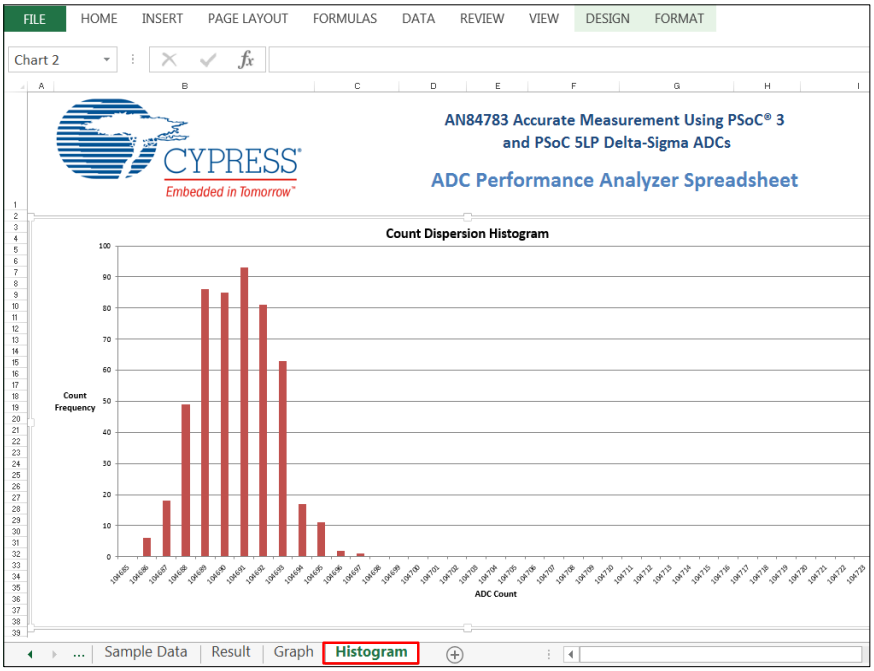
15. Click on the "Graph" page to view the ADC value versus sample number graph, as Figure 23 shows. This graph illustrates the noise in ADC counts.

Figure 23. Graph of ADC Counts



16. Go to the "Histogram" page to view the histogram that shows ADC count dispersion, as Figure 24 shows.

Figure 24. Histogram of ADC Counts



10 Summary

PSoC 3 and PSoC 5LP integrate a high-precision, highly configurable, 20-bit Delta-Sigma ADC and a variety of other analog and digital peripherals that can be used to create high-performance analog systems.

This application note has shown that the overall accuracy of a system depends on the accuracy of its components: the transducer, the PCB and its layout, the noise in the environment, and the signal processing circuitry as well as the ADC itself.

This application note has also shown that you can increase the accuracy of ADC measurements by properly designing the analog signal chain, properly configuring the ADC Component, using an external reference, using filters on the ADC counts, calibrating offset and gain, using correlated double sampling, and properly designing the PCB.

Two projects are included that demonstrate how to measure and calculate various parameters to determine the actual performance of an ADC-based system.

Note that PSoC 5LP has SAR ADCs in addition to a Delta-Sigma ADC. The techniques described in this application note can be adapted and applied to a SAR ADC–based system.

11 Related Application Notes

AN68403 – PSoC 3 and PSoC 5LP Analog Signal Chain Calibration

AN66444 – PSoC 3 and PSoC 5LP Correlated Double Sampling to Reduce Offset, Drift, and Low Frequency Noise

AN57821 – PSoC 3, PSoC 4, and PSoC 5LP Mixed Signal Circuit Board Layout Considerations

AN2099 – PSoC 1, PSoC 3, PSoC 4, and PSoC 5LP Single-Pole Infinite Impulse Response (IIR) Filters

AN61290 – PSoC 3 and PSoC 5LP Hardware Design Considerations

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3956316	NIDH	04/05/2013	New application note
*A	4621893	NIDH	01/22/2015	Added information on conversion modes
*B	4651285	NIDH	02/04/2015	Added information on how to use ADC to get accurate readings when the input to ADC is multiplexed Minor edits throughout the document Updated template
*C	5293739	NIDH	06/22/2016	Added self-help section Updated projects to PSoC Creator 3.3 SP2 Updated template and screenshots
*D	5728133	BENV	05/05/2017	Updated logo and copyright

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