AN84060

QDR®-IV Design Guide

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Associated Part Family: CY7C4*2*KV13, CY7C4*4*KV13
Related Application Notes: AN79938, AN4065

AN84060 describes the key features, functional description, operational modes, power calculation, and board design guidelines of QDR®-IV, Cypress's quad data rate family of networking SRAMs. This application note also highlights the key differences among the QDR-II, QDR-II+, and QDR-IV SRAM family members.

Contents

1 Introduction

Streaming video, cloud services, and mobile data have fueled the continuing growth of global network traffic. To support this growth, the next generation of networking systems must provide faster line rates and process millions of packets every second. Packets arrive in a random order and each packet requires several memory transactions to process. In high-performance networking systems, the flow of packets demands hundreds of millions of memory transactions every second to look up routes from a forwarding table or to update statistics.

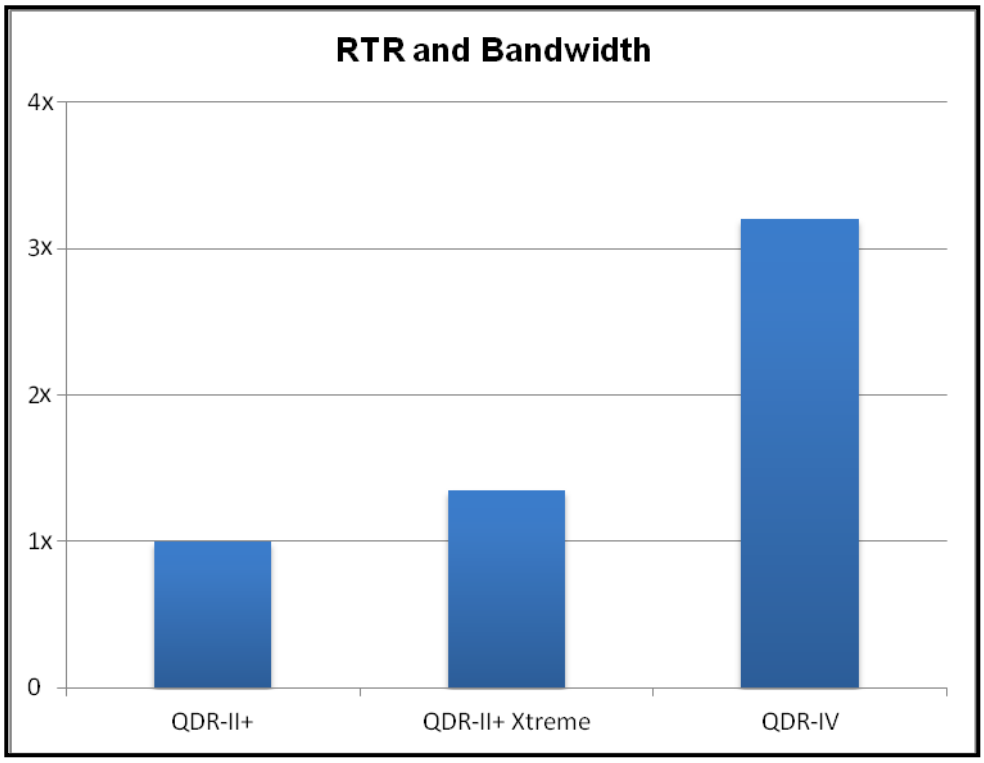
Thus, packet rates are directly proportional to the rate of random memory access. Next-generation networking equipment requires memories with very high random transaction rate (RTR) performance and bandwidth to keep pace with the ever-increasing network traffic.

Cypress's high-bandwidth QDR-IV SRAMs are designed for better RTR performance and they satisfy demanding network functions, such as updating statistics, tracking flow states, scheduling packets, and performing table lookups.

Specifically, RTR measures the number of fully random memory transactions (reads or writes) that can be performed with the memory. In other words, it is the rate at which random data can be addressed (or the random address rate). This metric is independent of the number of bits being accessed during the transaction. RTR is measured in millions of transactions per second (MT/s).

The chart in Figure 1 compares the maximum RTR and bandwidth of QDR-II+, QDR-II+ Xtreme, and QDR-IV devices. As the figure shows, QDR-IV has three times improved performance compared to QDR-II+ devices. This makes QDR-IV an ideal selection for high-performance networking systems.

Figure 1. RTR and Bandwidth Comparison



The QDR-IV family includes the following:

- QDR-IV High Performance (HP) SRAM: A two-word burst architecture device with two accesses for each cycle at a maximum frequency of 667 MHz and with a read latency of five clock cycles.
- QDR-IV Xtreme Performance (XP) SRAM: A banked two-word burst architecture device with two accesses for each cycle at a maximum frequency of 1066 MHz and with a read latency of eight clock cycles. The increase in frequency enables QDR-IV XP to deliver 2132 MT/s RTR and 153.5 Gb/s bandwidth.

2 QDR-IV High-Level Features Summary

Table 1 introduces the features of QDR-IV SRAM devices.

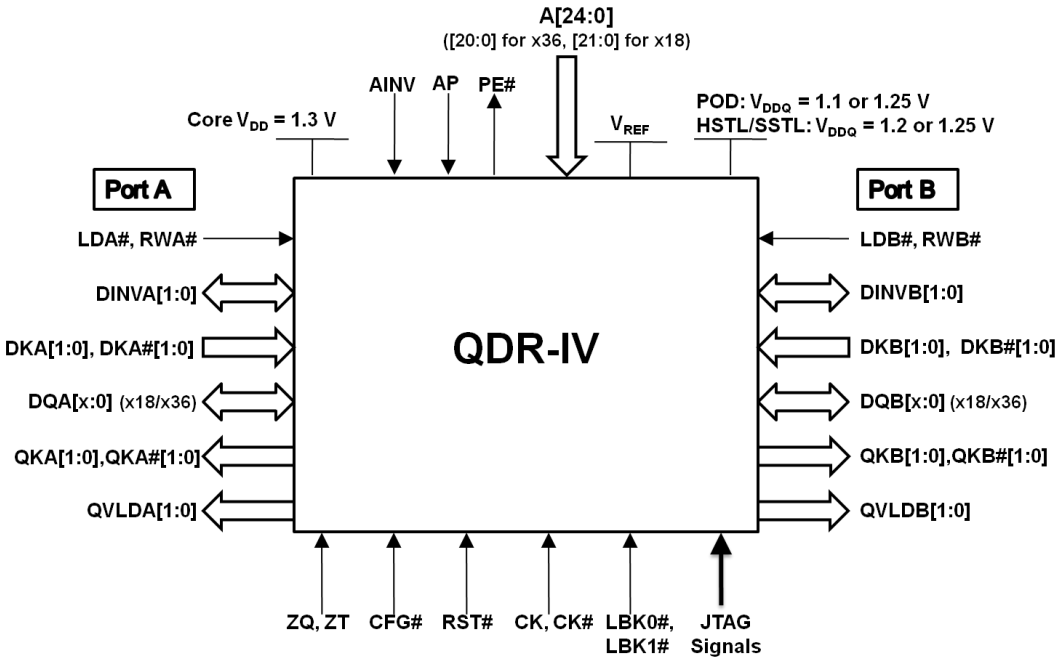
Table 1. QDR-IV Features

Feature	Description
Data Ports	QDR-IV has two independent bidirectional data ports that support simultaneous read/write transactions with a two-word burst architecture. Both data ports operate at double data rate. QDR-IV is available in either 18-bit or 36-bit I/O widths per port.
Address Port	QDR-IV contains a single address port that runs at double data rate and is used to control both data ports.
Control Signals	All the control signals in QDR-IV operate at single data rate (SDR).
Operation Modes	QDR-IV can operate in an eight-bank mode (QDR-IV XP SRAM) at up to 1066 MHz and in a non-banked mode (QDR-IV HP SRAM) at up to 667 MHz.
Clocking	QDR-IV uses three differential clocks: 1. (CK, CK#) for address and command signals 2. (DKA, DKA#, DKB, DKB#) for data input signals 3. (QKA, QKA#, QKB, QKB#) for data output signals
Bus Inversion	QDR-IV has a bus inversion feature to reduce switching noise and power. It is configurable ON/OFF for address and data.
Address Bus Parity Error Protection	QDR-IV supports configurable ON/OFF address bus-parity error protection. It provides data integrity for the address bus.
On-Die Termination (ODT)	QDR-IV offers configurable ON/OFF on-die termination (ODT) with clock, address, command, and data pins. It supports 40, 50, 60, 100, and120 Ω termination values.
Configurable Internal Registers	QDR-IV contains internal registers to configure the device. Access to these registers is only possible with a configuration mode that cannot coincide with normal memory transactions. Registers are written to during memory initialization and can be updated and read back.
Write Forwarding	QDR-IV supports write forwarding between the ports with full-data coherency.
ECC	QDR-IV introduces on-chip error correction code (ECC) to virtually eliminate the soft error rate (SER).
Training Mode	QDR-IV has the loopback operation mode for control, address, data, and clock pins for deskew training, which improves signal timing.
I/O Signaling	QDR-IV is compatible with the JESD8-24 compliant Pseudo Open Drain (POD) and with JESD8-16A compliant High-Speed Transceiver Logic/ Stub Series Terminated Logic (HSTL/SSTL) signaling. POD uses 1.1-V ±50-mV or 1.2-V ±50-mV I/O V_{DDQ} levels, while HSTL/SSTL supports 1.2-V ±50-mV or 1.25-V ±50-mV I/O V_{DDQ} levels.
Power Supply	QDR-IV requires 1.3-V ±40-mV core voltage (V_{DD}).
Package	QDR-IV is available in a 361-ball flip-chip ball-grid array (FCBGA) package that measures 21 mm × 21 mm with a 1-mm pitch.
JTAG	QDR-IV supports the JESD8-26-compliant JTAG 1149.1 Compatible Test Access Port with 1.3-V LVCMOS-compatible signaling.

Refer to the relevant datasheet for details on the timing waveforms.

Figure 2 shows a general interface diagram of QDR-IV. The interfaces are designed to be electrically compatible with POD and HSTL/SSTL-type interfaces.

Figure 2. Interface Diagram



3 Functional Description

The QDR-IV SRAM incorporates two data I/O ports designated as Port A and Port B. Because accesses to the two ports are independent, the random transaction rate is maximized for any combination of read/write accesses to the memory array.

In QDR-IV, access to each port is through a common address bus (A) running at double data rate. Addresses for Port A are latched on the rising edge of the input clock (CK), and addresses for Port B are latched on the falling edge of the CK or rising edge of the CK#. The control signals (LDA#, LDB#, RWA#, and RWB#) are running at single data rate (SDR), and they determine whether to perform a read or a write operation. Both data ports (DQA and DQB) are equipped with double data rate (DDR) interfaces. The device is offered in a 2-word burst architecture. It is available in ×18 and ×36 data bus widths.

The QDR-IV XP SRAM device has a bank-switching option. The Banking Operation section describes the use of bank switching, which enables the device to operate at much higher frequencies and RTR.

3.1 Clock Signal Description

- The CK/CK# clocks are associated with the address and control pins: An-A0, AINV, LDA#, LDB#, RWA#, and RWB#. The CK/CK# clocks are centered with address and control signals.
- The DKA/DKA# and DKB/DKB# are incoming clocks associated with the input write data. These clocks are center-aligned with respect to the input write data.

Based on the QDR-IV SRAM device's data bus width configuration, Table 2 shows the relationship of input clocks with respect to the input write data. To ensure proper timing between command and data cycles, and to enable proper data bus turnaround, the DKA/DKA# and DKB/DKB# clocks must meet the CK-to-DKx skew (t_{CKDK}), which is specified in the respective datasheet.

Table 2. Input Clocks and Write Data Relationship

Input Clocks	x18	x36
DKA0/DKA0#	Controls DQA[8:0]	Controls DQA[17:0]
DKA1/DKA1#	Controls DQA[17:9]	Controls DQA[35:18]
DKB0/DKB0#	Controls DQB[8:0]	Controls DQB[17:0]
DKB1/DKB1#	Controls DQB[17:9]	Controls DQB[35:18]

- The QKA/QKA# and QKB/QKB# are outgoing clocks associated with the read data. These clocks are edge-aligned with respect to the read output data.

  QK/QK#, the data output clock is generated from the internal PLL. It is synchronized to the CK/CK# clock and meets CK-to-QKx skew (t_{CKQK}), which is specified in the respective datasheet.

  Based on the QDR-IV SRAM device's data bus width configuration, Table 3 shows the relationship of output clocks with respect to the read data.

Table 3. Output Clocks and Read Data Relationship

Output Clocks	x18	x36
QKA0/QKA0#	Controls DQA[8:0]	Controls DQA[17:0]
QKA1/QKA1#	Controls DQA[17:9]	Controls DQA[35:18]
QKB0/QKB0#	Controls DQB[8:0]	Controls DQB[17:0]
QKB1/QKB1#	Controls DQB[17:9]	Controls DQB[35:18]

3.2 Read/Write Operation

Read and write commands are driven by the control inputs (LDA#, RWA#, LDB#, and RWB#) and the address inputs.

Port A control inputs are sampled at the rising edge of the input clock (CK). Port B control inputs are sampled at the falling edge of the input clock.

Table 4 shows the conditions for Port A and Port B Read/Write operation.

Table 4. Port A and Port B Read/Write Condition

	Read Operation	Write Operation
Port A	LDA# = 0 and RWA# =1	LDA# = 0 and RWA# =0
Port B	LDB# = 0 and RWB# =1	LDB# = 0 and RWB# =0

As Figure 3 and Figure 4 show, the Port A read data comes out of the DQA pins exactly five Read Latency (RL) clock cycles after the rising edge of CK in the case of the QDR-IV HP SRAM or eight RL clock cycles after the rising edge of CK in the case of the QDR-IV XP SRAM. The data is available after the number of RL clock cycles from the **rising** edge of the CK signal when the READ command was issued.

The Port A write data is supplied to the DQA pins exactly three Write Latency (WL) clock cycles after the rising edge of CK in the case of the QDR-IV HP SRAM or five WL clock cycles after the rising edge of CK in the case of QDR-IV XP SRAM. The data comes after the number of WL clock cycles from the **rising** edge of the CK signal when the WRITE command was issued.

The Port B read data comes out of the DQB pins exactly five RL clock cycles after the falling edge of CK in the case of the QDR-IV HP SRAM or eight RL clock cycles after the falling edge of CK in the case of the QDR-IV XP SRAM. The data is available after the number of RL clock cycles from the **falling** edge of the CK signal when the READ command was issued.

The Port B write data is supplied to DQB pins exactly three WL clock cycles after the falling edge of CK in the case of the QDR-IV HP SRAM or five WL clock cycles after the falling edge of CK in the case of the QDR-IV XP SRAM. The data comes after the number of WL clock cycles from the **falling** edge of the CK signal when the WRITE command was issued.

The QVLDA/QVLDB signals indicate valid output data at the respective port. QVLDA and QVLDB are asserted a half-clock cycle before the first data word driven on the bus and de-asserted a half-clock cycle before the last data word driven on the bus. Data outputs are tristated following the last data word.

Figure 3. Read Timing

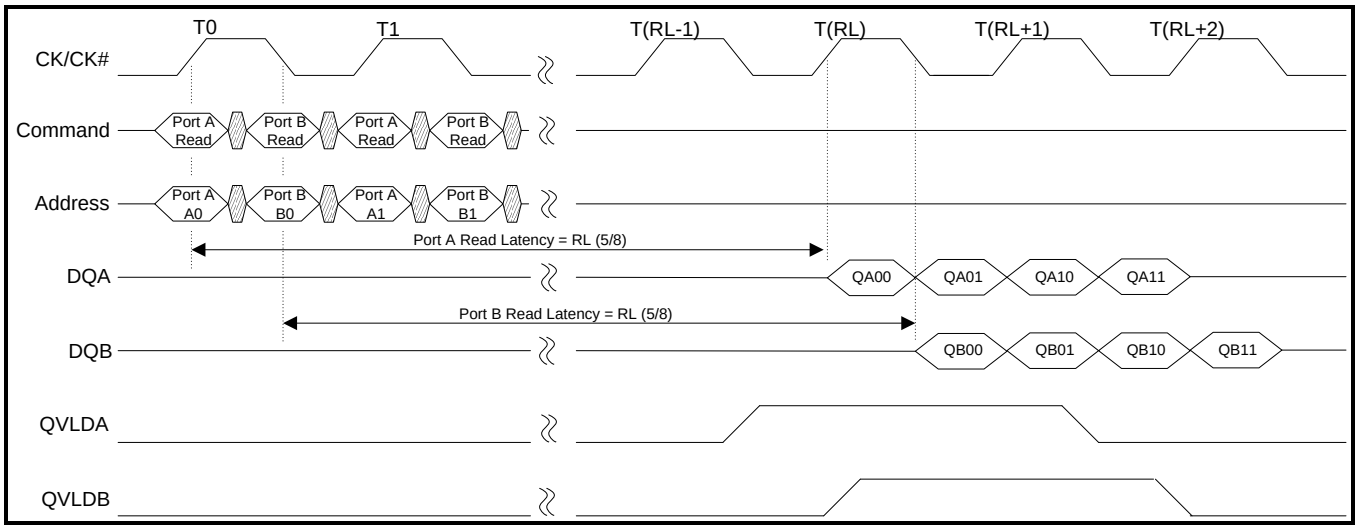
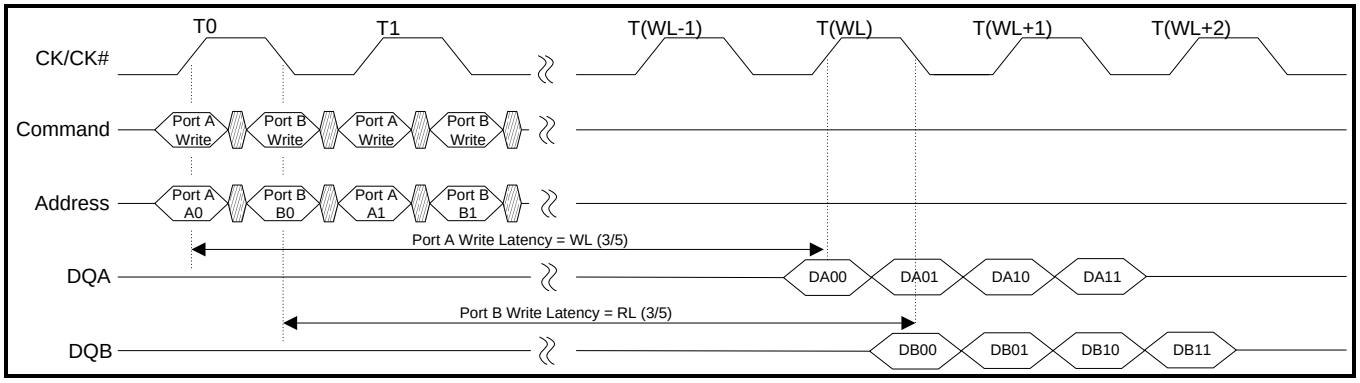


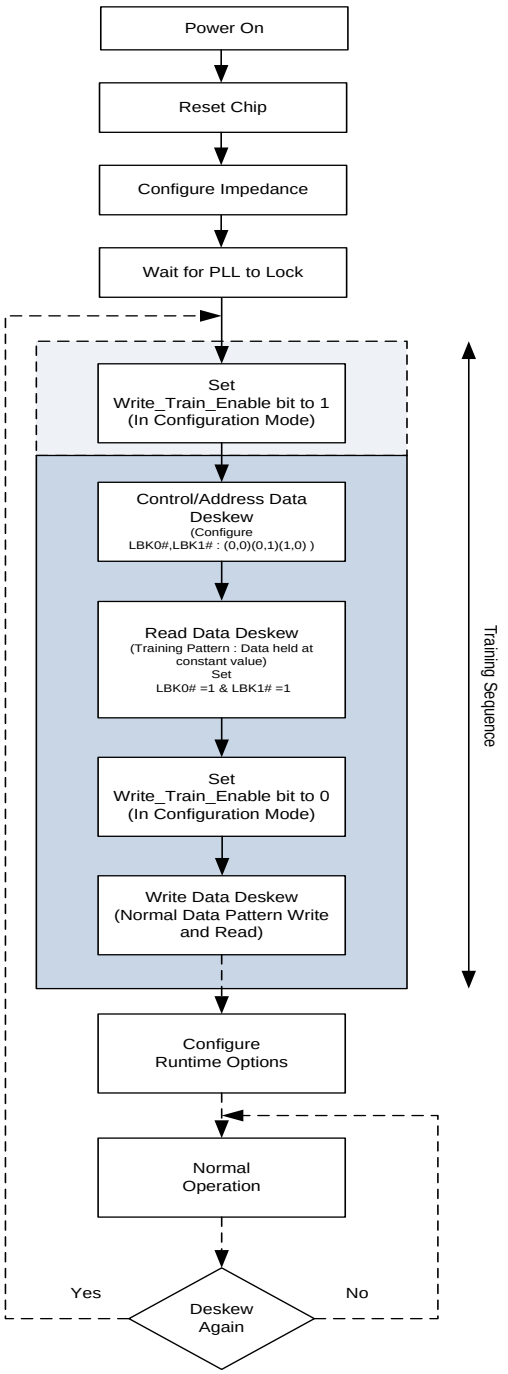
Figure 4. Write Timing



3.3 Deskew Training Sequences

The high frequency at which the memory controller and QDR IV operate means that the data valid window is very narrow. The QDR IV device supports a feature called “Deskew Training Sequence” that helps improve this data valid window period by reducing the skew between byte lanes. This results in better timing margins for the controller when reading data from the memory. This training sequence is an important part of the initialization process of Cypress’s QDR-IV SRAMs. This training sequence is usually employed by applications that do not support inbuilt deskew functionality. The training sequence is illustrated in Figure 5:

Figure 5. Deskew Training Sequence



Deskew training sequence is a part of the initialization procedure (Refer to the datasheet for initialization procedure). Immediately after the Power-Up and Reset Sequences, we need to set the Write_Train_Enable bit(Bit Location 7) in the Option Control Register during the configuration mode of operation. By doing so, we can avoid re-entering the configuration mode before the training sequence. Setting this bit does not have any influence until the Read Data Deskew training.

Deskew is achieved in three steps:

1. Control/Address Deskew

2. Read Data Deskew

3. Write Data Deskew

3.3.1 Control/Address Deskew

Set LBK0# and LBK1# to corresponding bit values depending on the signal to be deskewed. See Table 12 for loopback signal mapping. Thirty nine input signals are looped back to data pins of port A. Based on LBK0# and LBK1# status, at a time thirteen input signals are mapped to DQA0-DQA12.

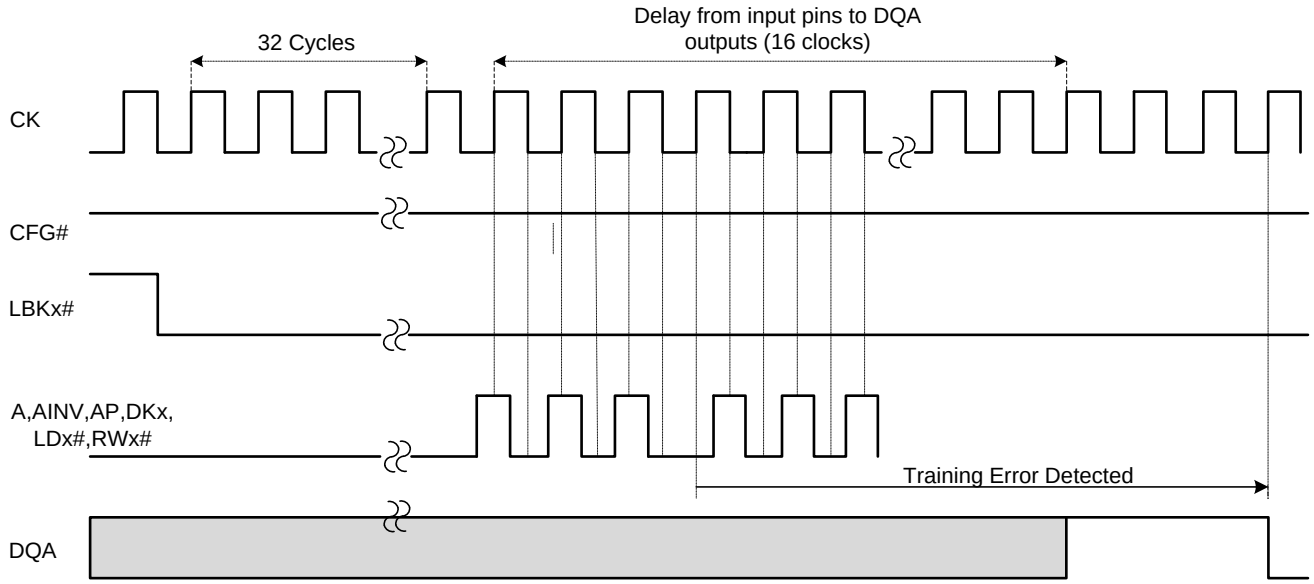
Table 5. Loopback Signal Mapping

Input Pin LBK0# = 0 LBK1# = 0	Input Pin LBK0# = 0 LBK1# = 1	Input Pin LBK0# = 1 LBK1# = 0	Output Pin
A0	A13	DKA0	DQA0
A1	A14	DKA0#	DQA1
A2	A15	DKA1	DQA2
A3	A16	DKA1#	DQA3
A4	A17	LDA#	DQA4
A5	A18	RWA#	DQA5
A6	A19	DKB0	DQA6
A7	A20	DKB0#	DQA7
A8	A21	DKB1	DQA8
A9	A22	DKB1#	DQA9
A10	A23	LDB#	DQA10
A11	A24	RWB#	DQA11
A12	AINV	AP	DQA12

The clock inputs DKA0, DKA0#, DKA1, DKA1#, DKB0, DKB0#, DKB1 and DKB#1 are free-running clock inputs and should be continuously running during the training sequence.

Each input pin is sampled on both the rising and falling edges using the input CK/CK#. The output value on the rising edge of the output QKA/QKA# will be the value that was sampled on the rising edge of the input clock. The output value on the falling edge of the output QKA/QKA# will be the inverted value of what was sampled on the falling edge of the input clock. Data inversion is not active in this mode and CFG# will be HIGH during Address/Control Loopback training.

Figure 6. Loopback Training Diagram



As Figure 6 shows, if the address/control signal is not deskewed, the signal on DQA, which should remain HIGH throughout the training period, will go LOW. This signal transition should be captured by the module driving the signals and processor/FPGA should calibrate the signal accordingly.

3.3.2 Read Data Deskew

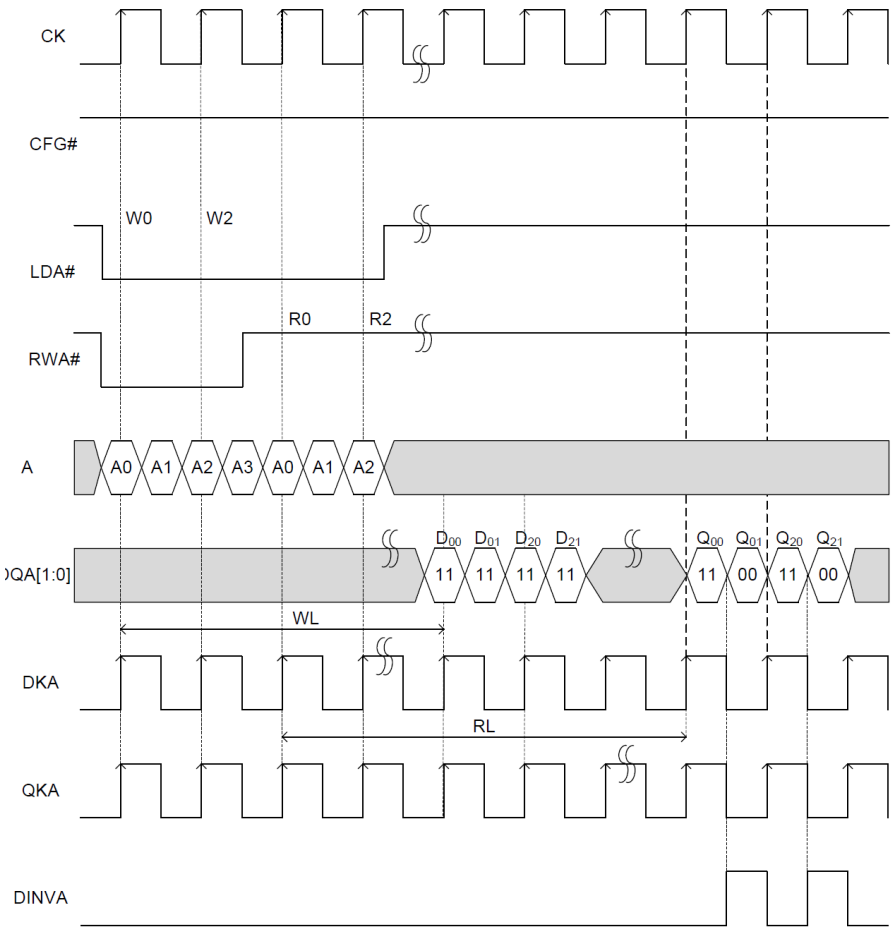
At this stage, the address, control, and data input clock are already deskewed. During the Read Data Deskew sequence, the training data pattern that is used to write into the memory is held at a constant value (D_{00}, D_{01}, D_{20}, D_{21}) as shown in the waveform diagram below. Both LBK0# and LBK1# are set to '1' during this training sequence.

Write_Train_Enable bit is set to '1' while configuring the option control registers. The first and second data burst are sampled from the same data bus, but the second data burst is complemented before writing into memory. The Write_Train_Enable bit has no effect on the read data cycles.

After the data pattern is written into the memory, standard read commands allow the memory controller to access the data and deskew with respect to QK/QK#. DINVA/DINVB will be ignored during write and always toggles during read when Write_Train_Enable = 1.

As shown in Read Data Deskew Diagram below, the data written to memory (D_{00}, D_{01}, D_{20}, D_{21}) is all 1s and the corresponding read data (Q_{00}, Q_{01}, Q_{20}, Q_{21}) toggles between '1' and '0'. The controller must capture the toggled data and verify. Otherwise, a precise calibration is required to confirm read data deskew from the controller.

Figure 7. Read Data Deskew Sequence Diagram



During Read Data Deskew sequence :

- Write_Train_Enable bit should be set to 1
- LBK0# = 1 & LBK1# = 1

WL:Write Latency

RL:Read latency

3.3.3 Write Data Deskew

By this time, the address, control, clock, and data outputs are already deskewed. Before performing the Write Data Deskew sequence, enter the configuration mode again to disable Write_Train_Enable by setting the corresponding bit to 0.

Write Data Deskew is performed using write commands to memory followed by read commands in the normal operation mode. The deskewed read data path is used to determine whether the write data was received correctly by the device. This permits the processor/FPGA to deskew with respect to DK/DK# input data clocks the following signals: DQA, DINVA, DQB, and DINVB.

3.4 Banking Operation

The QDR-IV XP SRAM is divided into eight banks to operate at a higher frequency (Maximum Operation Frequency = 1066 MHz); QDR-IV HP SRAM operates in non-banked mode at lower frequencies (Maximum Operating Frequency = 667 MHz).

The lower three address pins (A2, A1 and A0) in QDR-IV XP select the bank that will be accessed during the read or write operation. The only banking restriction is that a particular bank can be accessed only once each clock cycle. The bank access rule for QDR-IV XP SRAM necessitates that the bank address accessed on port B cannot to be same as bank address accessed on port A.

If a banking violation occurs, the read/write operation on Port A is unrestricted as it is sampled on the rising edge of the clock while that on Port B is denied. The QDR-IV HP SRAM does not have any banking restriction.

Figure 8. QDR-IV XP SRAM – Write/Read Operation

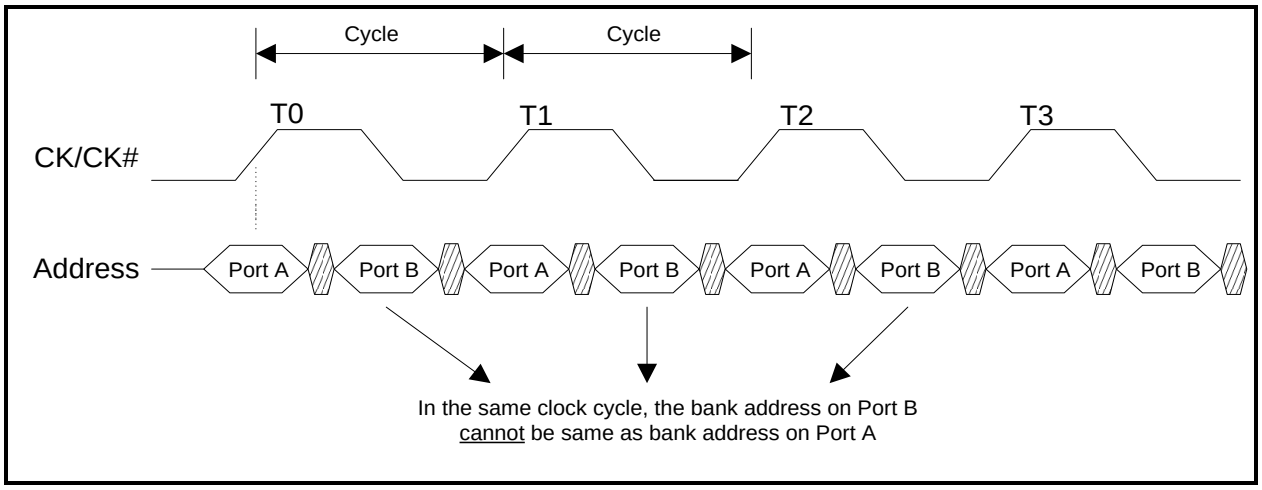
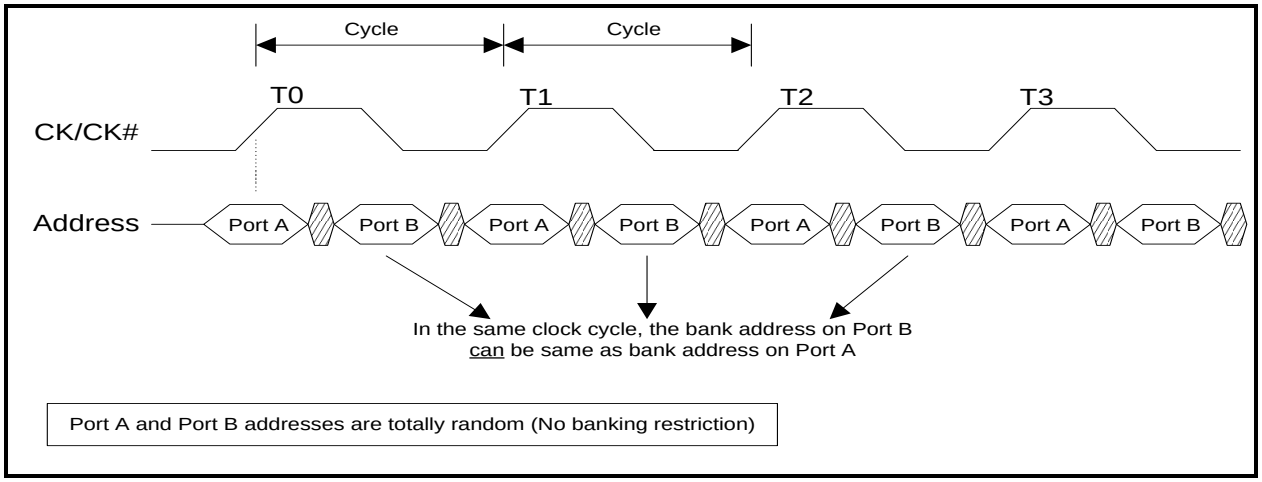


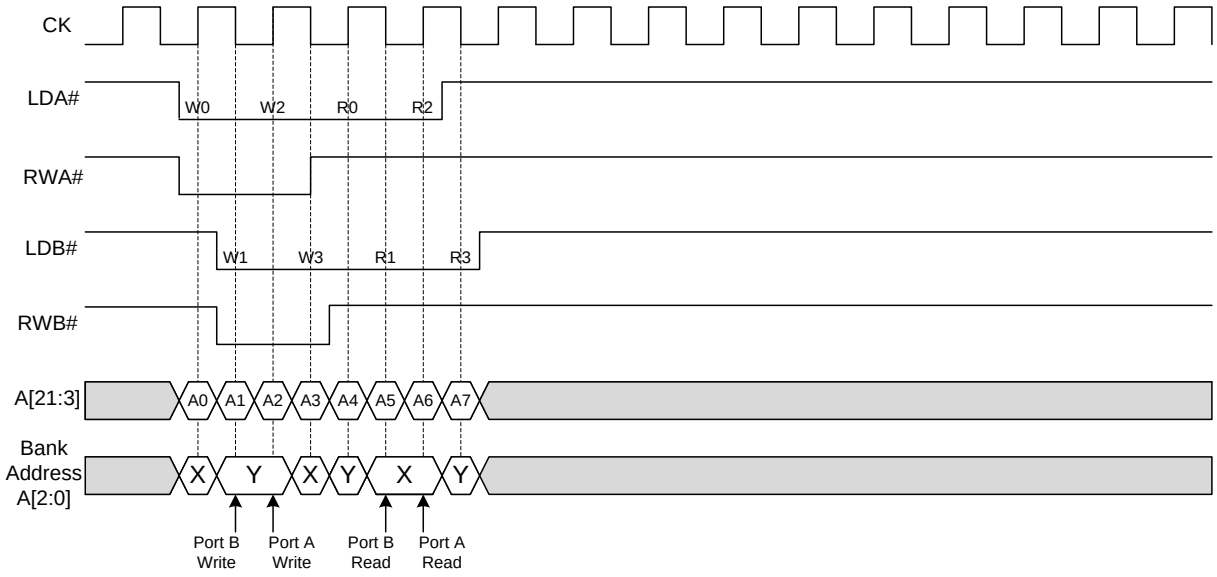
Figure 9. QDR-IV HP SRAM – Write/Read Operation



The banking restriction on QDR-IV XP SRAM may be looked upon as an advantage in applications where each bank of memory is used for different purposes and is not being accessed in the same clock cycle twice. One example could be where a network router can store different routing tables in each bank of the QDR-IV XP SRAM. If a particular routing table is not accessed more than once during the same clock cycle, it is possible to achieve high RTRs (Random Transaction Rate) offered by the QDR-IV XP SRAM. In such applications, the maximum RTR that can be achieved is 2132 MT/s with an operating frequency of 1066 MHz.

Another scenario where the banking restriction does not hinder the transaction rate is in designs with multiple ports at the physical layer with each port directed toward one of the banks in memory. These ports would be multiplexed to Port A and Port B of QDR-IV XP SRAM. In this design, no single bank can be accessed in the same cycle twice as each bank is connected to different ports at the physical layer. However, one can access the same bank again in one clock cycle period if the first access to the bank is through port B on the falling edge of the current clock cycle and the second access is through port A on the rising edge of the next clock cycle. In the diagram shown below, during the write sequence, both port B and port A access bank Y in one clock cycle period. Similarly, port B and port A access bank X during the read sequence in one clock cycle period.

Figure 10. Access To Same Memory Bank In One Clock Cycle Period



3.5 Bus Turnaround Considerations

The Bus Turnaround time plays an important role in determining, if additional interval is required between the read and write commands to avoid bus contention on the same I/O port.

Let us consider a write command followed by a read command on port A in QDR-IV HP SRAM. The write data is supplied to the DQA pins exactly three clock cycles from the rising edge of the CK signal corresponding to the cycle when the write command was initiated. The read command can be issued in the next cycle as the data would be available on DQA pins after five clock cycles from the rising edge of the CK signal corresponding to the cycle when the read command was initiated. We still have two extra cycles, which will be useful to accommodate the bus turnaround time and trace delay (from ASIC/FPGA to QDR IV memory). Therefore,, the read command can be initiated right after the write command.

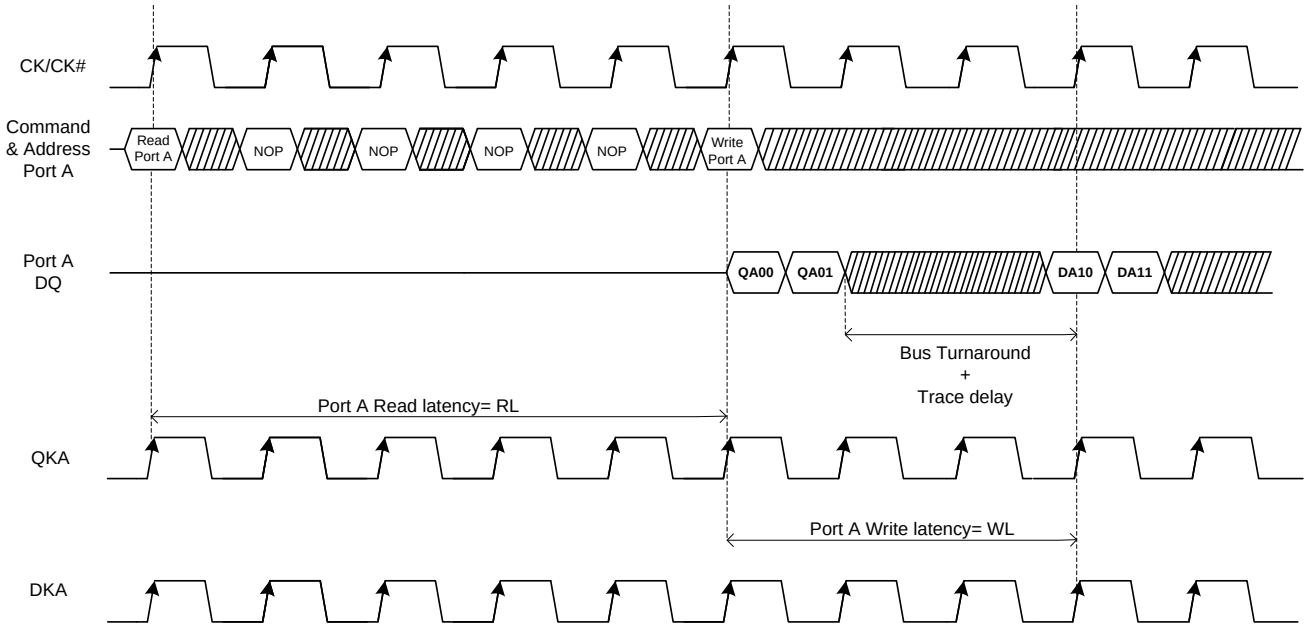
In other cases, if the write command follows the read command, the write command should be issued three clocks after the read command. This is because the read data on DQA pins would appear five clocks after the read command is sampled at the rising edge of the clock signal CK, and the write data is supplied to the DQA pins exactly three clock cycles after the write command is sampled at the rising edge of the clock signal CK. Otherwise, there will be bus contention. Therefore, the minimum clock cycles after which a write command should be issued is given by RL – WL + 1 (RL: Read latency; WL: Write latency, both measured in the number of clock cycles).The extra one cycle is to allow for the data to be captured correctly and compensate for the bus turnaround delay (usually one clock cycle).

If the trace delay is more than the bus turnaround delay, then the interval between ‘Read to Write’ commands is given by:

Time Period between “Read to Write” command = Read latency – Write latency + 1 + Trace Delay

Refer to Figure 11. The write command on port A is issued after four clock cycle from the read command. This is done to avoid bus contention due to the difference in read and write latencies,, bus turnaround time, and trace delay.

Figure 11. QDR-IV HP SRAM Timing Analysis Diagram



3.6 Bus Inversion

QDR-IV devices support the bus inversion feature to reduce the switching noise and I/O power. In a memory transaction, either the memory controller or the QDR-IV could choose to apply bus inversion.

Because the Pseudo Open Drain (POD) signaling mode in QDR-IV devices provides an option for I/O signals with high-side termination to VDDQ, signals driven to a logic HIGH state consume zero power. Therefore, if more than half of the bits in a transaction are zero, bus inversion is a good feature to use with POD I/O signaling. Note that internally QDR-IV takes care of data integrity for the inverted address and data bus.

The address and data bus inversion features can be enabled or disabled using chip-configuration registers.

3.6.1 Address Bus Inversion

The AINV is a double data rate signal and is updated for each address sent to the memory device. The AINV pin indicates whether the address bus (An – A0) and AP are inverted. AINV is an active HIGH signal. When AINV = 1, the address bus is inverted; when AINV = 0, the address bus is not inverted. The function of the AINV pin is controlled by the memory controller.

The address bus and the address parity bit are considered together as Address Group (AG). Table 6 lists the AG definitions and AINV setup conditions for x18 and x36 QDR-IV options.

Table 6. Address Bus Inversion Conditions

	x18	x36
Address Group	AG[22:0] = A[21:0],AP	AG[21:0] = A[20:0],AP
Inversion Logic	If number of logic “0” in AG[22:0] ≥12, then invert AG[22:0] by setting AINV = 1	If number of logic “0” in AG[21:0] ≥11, then invert AG[21:0] by setting AINV = 1
	If number of logic “0” in AG[22:0] <12, then keep AG[22:0] as it is and set AINV = 0	If number of logic “0” in AG[21:0] <11, then keep AG[21:0] as it is and set AINV = 0

3.6.2 Example of x36 Device

3.6.2.1 Without Address Bus Inversion:

Assume that you want to access the 22'h 000199 and 22'h 3FFCFF addresses respectively. Seventeen address pins need to switch the logic state between the first and second addresses, as shown in the following table (red cells). This increases the switching noise, I/O current, and crosstalk on the address pins.

Table 7. Address Bus Order (Without Bus Inversion)

AG[21:0]	22 Bits (Binary)																					
1st Address Group - 22'h 000199	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1
2nd Address Group - 22'h 3FFCFF	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1

3.6.2.2 With Address Bus Inversion:

According to Table 6, the 1st address group (22'h 000199) satisfies the inversion logic condition. Therefore, before the memory controller transmits the 1st address group, it will invert (22'h 000199 --> 22'h 3FFE66) the address group and set the AINV pin to 1. Because the 2nd address group does not need to be inverted, the memory controller transmits it with no change and AINV is set to 0.

The following table shows the result with address bus inversion. You can now see that only five address pins need to switch the logic (see the red cells). Therefore, the total number of switching bits is reduced to five, which results in reduced simultaneous switching output (SSO) noise, I/O current, and crosstalk. Thus, address bus inversion feature supported by QDR-IV helps reduce the effect of switching noise.

Table 8. Address Bus Order (With Bus Inversion)

AG[21:0]	22 Bits (Binary)																						AINV
1st Address Group - 22'h 3FFE66 **(Inverted)**	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	0	0	1	1	0	1
2nd Address Group - 22'h 3FFCFF **(same)**	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0

AINV pins can be left floating (unconnected) if the address inversion feature is disabled.

3.7 Data Bus Inversion

Data bus inversion performs a similar function as address bus inversion on the data lines. However, inversion bits are generated by a memory controller during a memory write operation and the inversion logic within the QDR-IV memory generates inversion bits during a memory read operation.

The DINVA and DINVB pins indicate whether the corresponding DQA and DQB pins are inverted. DINVA and DINVB are active HIGH signals. When DINV = 1, the data bus is inverted; when DINV= 0, the data bus is not inverted.

DINVA[1] and DINVA[0] are independent and control their respective DQA groups. DINVA[0] covers DQA[17:0] for the x36 configuration and DQA[8:0] for the x18 configuration, respectively. DINVA[1] covers DQA[35:18] for the x36 configuration and DQA[17:9] for the x18 configuration, respectively. Similarly, DINVB[0] covers DQB[17:0] for the x36 configuration and DQB[8:0] for the x18 configuration, respectively. DINVB[1] covers DQB[35:18] for the x36 configuration and DQB[17:9] for the x18 configuration, respectively.

Table 9 lists the DINV-bit descriptions and DINVA setup conditions for the x18 and x36 QDR-IV options.

Table 9. Data Bus Inversion Conditions

	x18	x36
DINV bits	DINVA[1] covers DQA[17:9], DINVA[0] covers DQA[8:0] DINVB[1] covers DQB[17:9], DINVB[0] covers DQB[8:0]	DINVA[1] covers DQA[35:18], DINVA[0] covers DQA[17:0] DINVB[1] covers DQB[35:18], DINVB[0] covers DQB[17:0]
Inversion Logic	If number of logic “0” in DQA[8:0] ≥5, then invert DQA[8:0] by setting DINVA[0] = 1	If number of logic “0” in DQA[17:0]≥10, then invert DQA[17:0] by setting DINVA[0] = 1
	If number of logic “0” in DQA[8:0] <5, then keep DQA[8:0] as it is and set DINVA[0] = 0	If number of logic “0” in DQA[17:0]<10, then keep DQA[17:0] as it is and set DINVA[0] = 0

Note: A similar Inversion logic can be applied to DINVA[1], DINVB[0], and DINVB[1] for their respective DQ groups.

3.7.1 Example of x18 Device

3.7.1.1 Without Data Bus Inversion:

Assume that you want to transmit 9’h 007 and 9’h 1F3 on DQA[8:0] respectively. As a result, six data pins need to switch the logic between the first and second DQA[8:0] bits, as shown in the following table (red cells). This will increase the switching noise, I/O current, and crosstalk on data pins.

Table 10. Data Bus Order (Without Bus Inversion)

DQA[8:0]	9 Bits (Binary)								
1ST DQA[8:0] - 9'h 007	0	0	0	0	0	0	1	1	1
2ND DQA[8:0] - 9'h 1F3	1	1	1	1	1	0	0	1	1

3.7.1.2 With Data Bus Inversion:

According to Table 9, the 1st DQA[8:0] satisfies the inversion logic condition. Therefore, before the memory controller transmits the 1st DQA[8:0], it will invert (9’h 007 --> 9’h 1F8) the pin and set the DINVA[0] pin to 1. Because the 2nd DQA[8:0] does not need be inverted, so the memory controller will transmit it with no change and will set DINVA[0] to 0.

Table 11 shows the result with data bus inversion. In this case, only three data pins need to switch the logic (see the red cells). Hence, the total number of switching bits is reduced to three, which results in reduced SSO noise, I/O current, and crosstalk.

Table 11. Data Bus Order (With Bus Inversion)

DQA[8:0]	9 Bits (Binary)									DINVA[0]
1st DQA[8:0] - 9'h 1F8 (Inverted)	1	1	1	1	1	1	0	0	0	1
2nd DQA[8:0] - 9'h 1F3 (same)	1	1	1	1	1	0	0	1	1	0

DINVA/DINVB pins can be left floating (unconnected) if the data bus inversion feature is disabled.

3.8 Address Parity

QDR-IV has a single address bus running at double data rate and high frequency. Therefore, the Address Parity Input (AP) and Address Parity Error Flag Output (PE#) pins provide an address parity feature in the chip to ensure the data integrity of the address bus. The Address Parity function is optional; you can enable or disable it using the configuration registers.

The AP pin is used to provide an even parity across the address pins (An to A0). The AP value is set if the total number of 1s of AP and An to A0 add up to an even number.

- For a x18 data bus-width device, set the AP so that the number of 1s in A[21:0] and AP are even.
- For a x36 data bus-width device, set the AP so that the number of 1s in A[20:0] and AP are even.

3.8.1 Example of x36 Device

Let us take two addresses, 21'h1E0000 and 21'h1F0000, for a x36 data bus-width device. Table 12 shows how to set an AP value for each address.

Table 12. Address Parity Feature

	Address, A[20:0] (x36 Device)																					AP	Number of 1s in A[20:0] and AP	
21'h1E0000	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	4	AP=0 because there is an even (four) number of 1s in A[20:0]
21'h1F0000	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	6	AP=1 because there is an odd (five) number of 1s in A[20:0]

When a parity error occurs, the complete address of the first error is recorded in configuration registers 4, 5, 6, and 7, (refer to the relevant datasheet for more information on the configuration registers) along with the Port A/B error bit and address invert bit. The Port A/B error bit indicates the port where the address parity error occurred: '0' for Port A and '1' for Port B. This information remains latched until cleared by writing a '1' to the Address Parity Error Clear bit in configuration register 3.

Two counters are used to indicate if multiple address parity errors have occurred. The Port A Error Count is a running count of the number of parity errors on Port A addresses. Similarly, the Port B Error Count is a running count of the number of parity errors on Port B addresses. They each independently count to a maximum value of 3 and then stop counting. These counters are free-running and they are both reset by writing a '1' to the Address Parity Error Clear bit in configuration register 3.

As soon as the address parity error is detected, the write operation will be ignored to prevent memory corruption. However, the read operation continues with the incoming incorrect address, and the false data will be sent out from the memory.

PE# is an active LOW signal, which indicates an address parity error. The PE# signal is set to '0' within eight cycles (in QDR-IV XP SRAMs) or five cycles (in QDR-IV HP SRAMs) after an address parity error was detected. It remains asserted until the error is cleared through configuration registers. The address parity check is completed after address inversion is processed.

As soon as PE# goes LOW, the controller must stop the memory operation, and reset PE# to HIGH using the configuration registers. In addition, the controller must rewrite data into the memory due to the earlier write operation being blocked by the device owing to the AP error detect.

AP and PE# pins can be left floating (unconnected) if the address parity feature is disabled.

4 Design Recommendations for Memory Controller

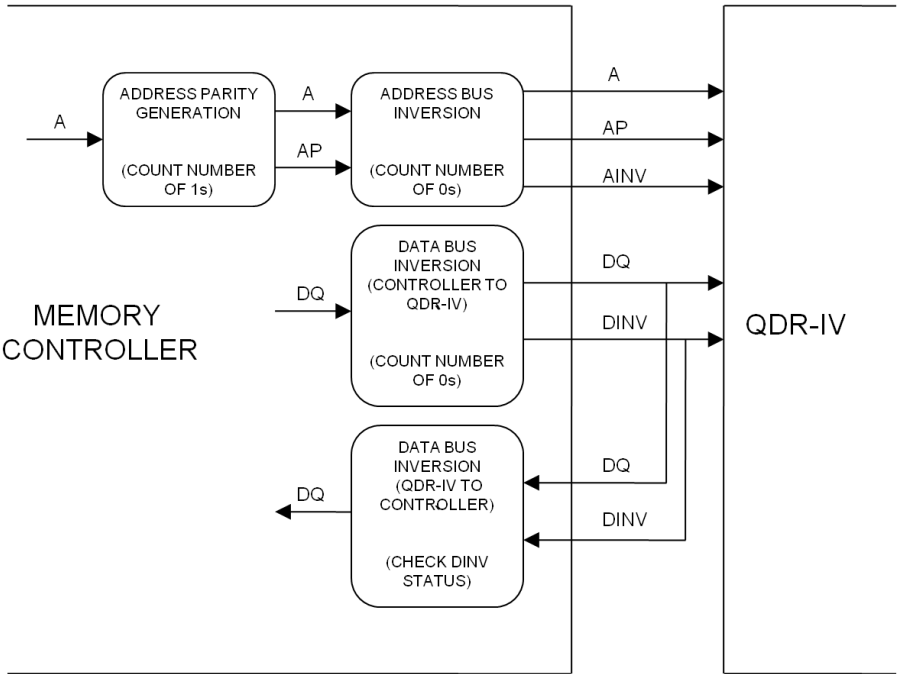
This section provides some memory controller design recommendations when address parity and bus inversion features of the QDR-IV are enabled.

The memory controller must first generate the address parity bit based on the address bus. Address inversion should be done later on the address bus and address parity bit.

For data bus inversion, the memory controller needs to count the number of logic 0s in the respective DQ bus to generate the corresponding DINV bit (based on the data bus inversion condition) before sending the data to QDR-IV.

QDR-IV uses the same logic for data bus inversion while transmitting the data to the memory controller. To identify the received data from QDR-IV, the controller only needs to check the status of the corresponding DINV bit. If the controller receives DINV = 1, then it needs to invert the relevant data bus; otherwise the received data bits must remain unchanged. Figure 12 shows the design consideration for the memory controller.

Figure 12. Design Consideration for Memory Controller



Cypress offers a reference design memory controller for Xilinx Virtex-7 FPGA to qualified QDR-IV customers. Contact qdr-iv@cypress.com for controller availability.

Contact Xilinx for QDR-IV memory controller on Ultrascale platform.

Contact Altera for QDR-IV memory controller on Arria-10 platform.

4.1 Error Correcting Code (ECC)

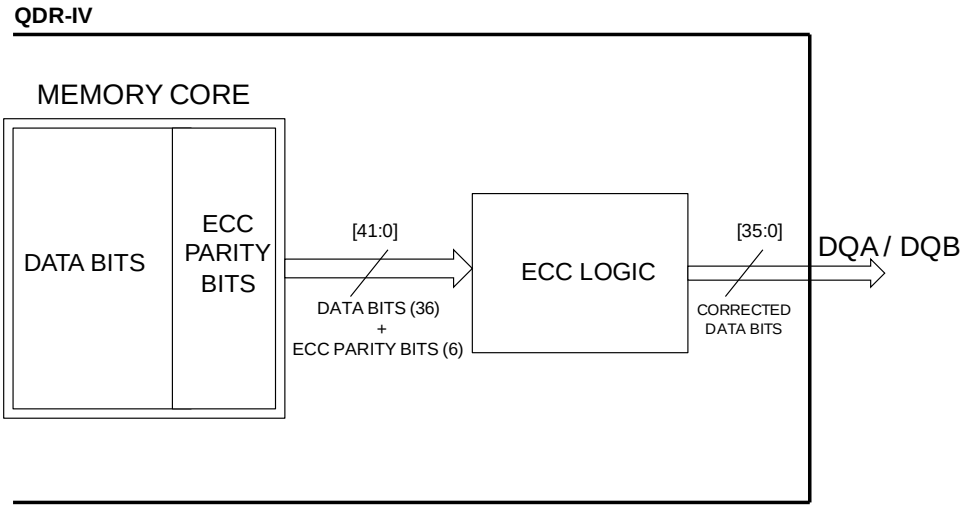
System designers have to rely on techniques such as off-chip error correction or redundancy to achieve a higher reliability. These techniques result in overheads in terms of either PCB space or additional processing time. QDR-IV offers a single-chip solution with on-chip error correcting code (ECC), reducing the board space, cost, and design complexity. It also reduces the overall soft error rate (SER) of the QDR-IV memory array. This feature covers both x18 and x36 data bus-width options and will always be enabled in the SRAM. The ECC protection provides single-bit error correction (SEC).

QDR-IV generates the ECC parity bits internally from the input data and stores them in the memory array. The memory array contains extra bits, which are required to store the ECC parity. However, these extra internal parity bits are not brought out to the external pins.

For example, Figure 13 shows the output data logic diagram for a x36 device. There are six ECC parity bits for 36 data bits; therefore, 42 bits (36 data bits + 6 ECC parity bits) arrive to the ECC logic from memory core. As a result, the ECC logic provides 36 bits of corrected output data.

QDR/DDR SRAMs without ECC typically have an SER Failure in Time (FIT) rate of 200 FIT/Mb. This number improves to 0.01 FIT/Mb with ECC, which provides an improvement of four orders of magnitude.

Figure 13. Output Data Logic (x36 Option)



5 QDR-IV Operational Modes

QDR-IV XP SRAM works at a higher frequency and has a few bank access rules, while QDR-IV HP SRAM operates at a relatively lower frequency with no bank access restrictions.

QDR-IV operates with read latency and write latency values that are determined by the speed of operation. Table 13 defines the operational modes and frequencies supported for each.

Table 13. Operational Modes

	QDR-IV HP SRAM		QDR-IV XP SRAM	
Clock Frequency	600 MHz	667 MHz	933 MHz	1066 MHz
Read Latency	5 cycles	5 cycles	8 cycles	8 cycles
	8.33 ns	7.5 ns	8.57 ns	7.5 ns
Write Latency	3 cycles	3 cycles	5 cycles	5 cycles
Banking Operation	No		Yes	
Bus Width	x18, x36			
I/O Type	1.1 V and 1.2 V POD 1.2 V and 1.25 V HSTL/SSTL			
Package	361 FCBGA			
Port configuration	Bidirectional R/W ports			
Density	144 Mb, 72 Mb			

6 Board Design Guidelines

6.1 QDR-IV Input Voltages Requirements

Table 14 shows the different input voltage requirements for QDR-IV SRAM using POD and HSTL/SSTL signaling.

Table 14. QDR-IV Input Supply Voltages

POD Interface					
Parameter	**Description**	**Min**	**Typ**	**Max**	**Unit**
V_{DD}	Core supply voltage (1.3 V ± 40 mV)	1.26	1.3	1.34	V
V_{DDQ}	I/O supply voltage (1.1 V ± 50 mV)	1.05	1.1	1.15	V
	I/O supply voltage (1.2 V ± 50 mV)	1.15	1.2	1.25	
V_{REF}	Reference voltage	V_{DDQ} × 0.69	V_{DDQ} × 0.7	V_{DDQ} × 0.71	V
HSTL/SSTL Interface					
Parameter	**Description**	**Min**	**Typ**	**Max**	**Unit**
V_{DD}	Core supply voltage (1.3 V ± 40 mV)	1.26	1.3	1.34	V
V_{DDQ}	I/O supply voltage (1.2 V ± 50 mV)	1.15	1.2	1.25	V
	I/O supply voltage (1.25 V ± 50 mV)	1.2	1.25	1.3	
V_{REF}	Reference voltage	V_{DDQ} × 0.48	V_{DDQ} × 0.5	V_{DDQ} × 0.52	V

6.1.1 V_{DD} and V_{DDQ} Generation

- Active current (I_{DD}) can be found under the respective device datasheet to design the V_{DD} power supply. Cypress recommends generating V_{DD} and V_{DDQ} from the regulator ICs.
- I/O switching current (I_{DDQ}) for V_{DDQ} can be calculated from the power calculator tool (in the Power Consumption and Junction Temperature Calculation section). If QDR-IV operates with the ODT feature, then the I/O switching power and the ODT power need to be calculated to get the total I_{DDQ}.

6.1.2 V_{REF} Generation

- V_{REF} consumes negligible amount of current because it is an input to the differential amplifier. The maximum V_{REF} current requirement for the POD signaling mode is 3 µA and for the HSTL/SSTL signaling mode is 1 µA.
- V_{REF} should track V_{DDQ} voltage. V_{REF} is equal to $V_{DDQ}/2$ for HSTL/SSTL and V_{DDQ} x 0.7 for POD interface. So, V_{REF} can be generated by using resistor divider with V_{DDQ} or by using regulator IC.

6.1.3 V_{TT} Generation for HSTL Signaling

- The board needs an extra termination voltage (V_{TT} = $V_{DDQ}/2$) supply if the input signals are terminated onboard and the ODT option is disabled in QDR-IV.
- Calculate the external termination power by using power calculator tool to estimate the V_{TT} current for V_{TT} power supply design.
- Because V_{TT} should also track V_{DDQ}, Cypress recommends generating V_{TT} by using a V_{DDQ} source or regulator, which can supply or drop the current and control the voltage.

6.2 Decoupling Capacitors Requirements

Decoupling capacitors are required to reduce the noise in the power system. The objective of these capacitors is to eliminate the effects of inductance or ground bounce on the power supply bus. The capacitor, which has a low series resistance and series inductance, decouples or “bypasses” the power supply bus from the IC.

The decoupling capacitor has the following advantages:

- Reduces the voltage swing on the power and ground pins.

- Provides a low-impedance path from the power plane to the ground plane.
- Provides a signal return path between the power and ground planes.

Refer to Figure 14. QDR-IV package (Top side) contains decoupling capacitors for V_{DD} and V_{DDQ} on it. Table 15 shows the QDR-IV package decoupling capacitors for the respective input voltages. These package decoupling capacitors can be considered in the power integrity simulation for the board decoupling capacitor scheme.

Figure 14. QDR-IV Package Outline

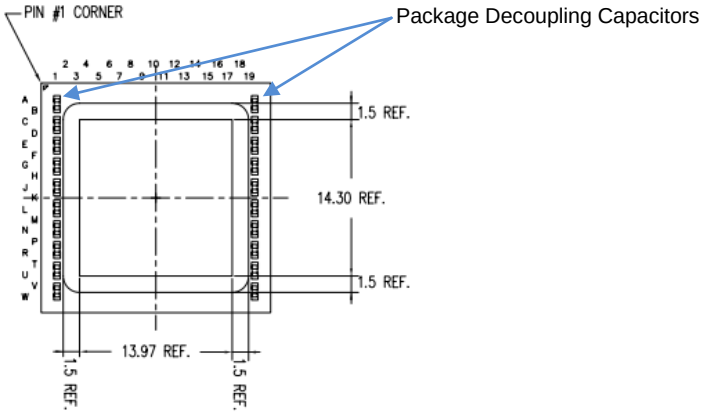


Table 15. QDR-IV Package Decoupling Capacitors

Voltage	Package Decoupling Capacitors
V_{DD}	10 x 100 nF
V_{DDQ}	10 x 100 nF

6.3 Determining Board Decoupling Capacitors

This section shows an example of how to achieve power integrity for V_{DDQ} using the QDR-IV characterization board as a reference. Cypress recommends that you perform simulations based on the target board to arrive at the target impedance.

First, find the target Impedance (Z_T) for the respective power nets. The target impedance depends on the average current (assumed to be 50% of max current) and the noise voltage tolerated as a percentage of the external supply voltage (V_{DD}, V_{DDQ}, V_{REF}, and V_{TT}).

Thus,

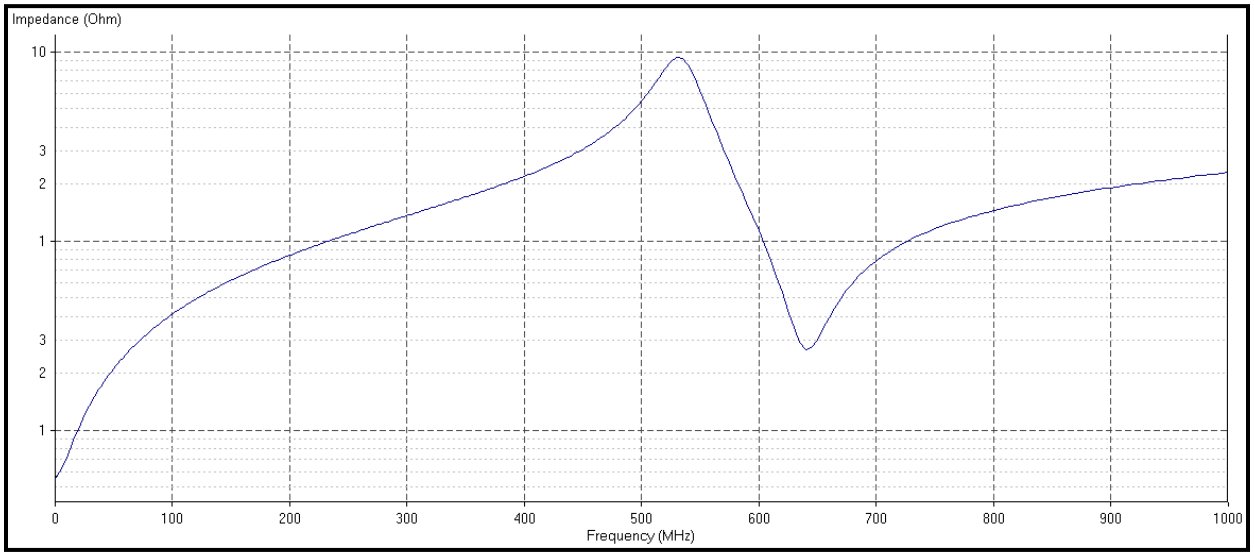
Target Impedance (Z_T) = (Voltage Supply x Noise Percent) / (50% of Maximum Transient Current) …….…… (1)

The voltage supply in the numerator depends on the supply noise specifications for V_{OH}-V_{IH} and V_{OL}-V_{IL}. This is the maximum level of supply noise that can be tolerated. The maximum current is the overshoot level of current when all outputs are switching. The assumptions are 20 mA maximum transient current per output, and 100 outputs switching. The noise level assumed is 10% of V_{DDQ} (at 1.2 V typical). The resulting target impedance for QDR-IV is 120 mΩ.

Next, simulate the voltage segment or plane. The tool (e.g. Cadence SIGRITY) should support decoupling capacitor libraries which comprehend ESR/ESL which are the lead resistance and inductance. The choice of the capacitor depends on the maximum voltage, size, cost, etc.

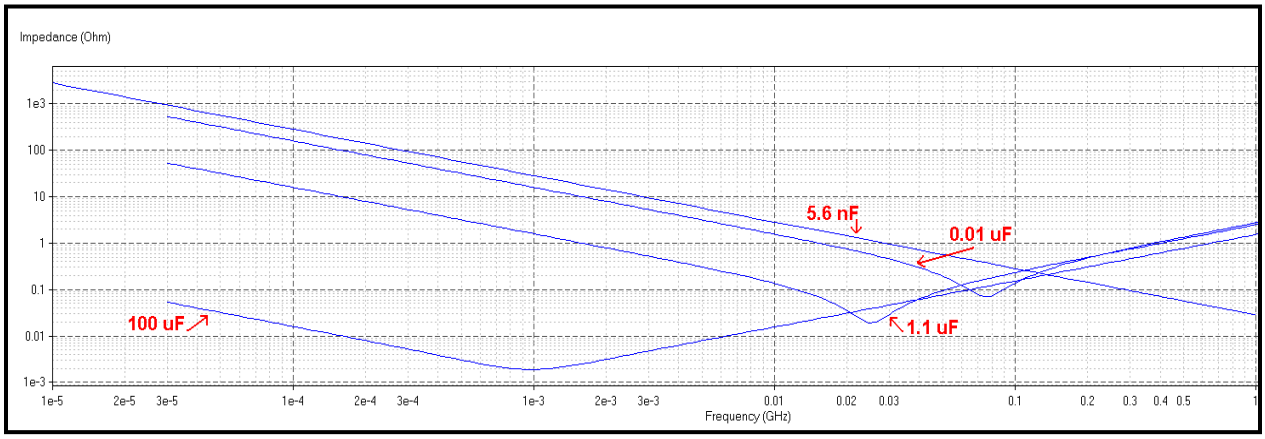
The following example simulation is done in the frequency domain. Usually a simulation without any decoupling capacitors is run to see the power impedance without any capacitors including any on-die capacitors.

Figure 15. Power Integrity for VDDQ Without Decoupling Capacitor



Then, iteratively the capacitors are loaded and turned on in the tool. The iteration involves pre-selection of capacitors, which depends on the frequency at which the impedance is high. The following figure shows a sample of the individual frequency response for some capacitors. The largest capacitors are near the Voltage Regulator Model (VRM), and progressively get smaller. The largest capacitors lower the impedance at low frequency, and vice versa, with the on-die capacitors addressing the highest frequency range. It is only necessary to run the power integrity simulation up to the maximum switching frequency. It is also recommended that a VRM be used in the simulation setup. The VRM can be a simple resistor with a very low value (e.g., 0.001 ohms). Alternatively, a spice model for the VRM can be used. The VRM reduces the DC-level impedance, which is the case on actual boards.

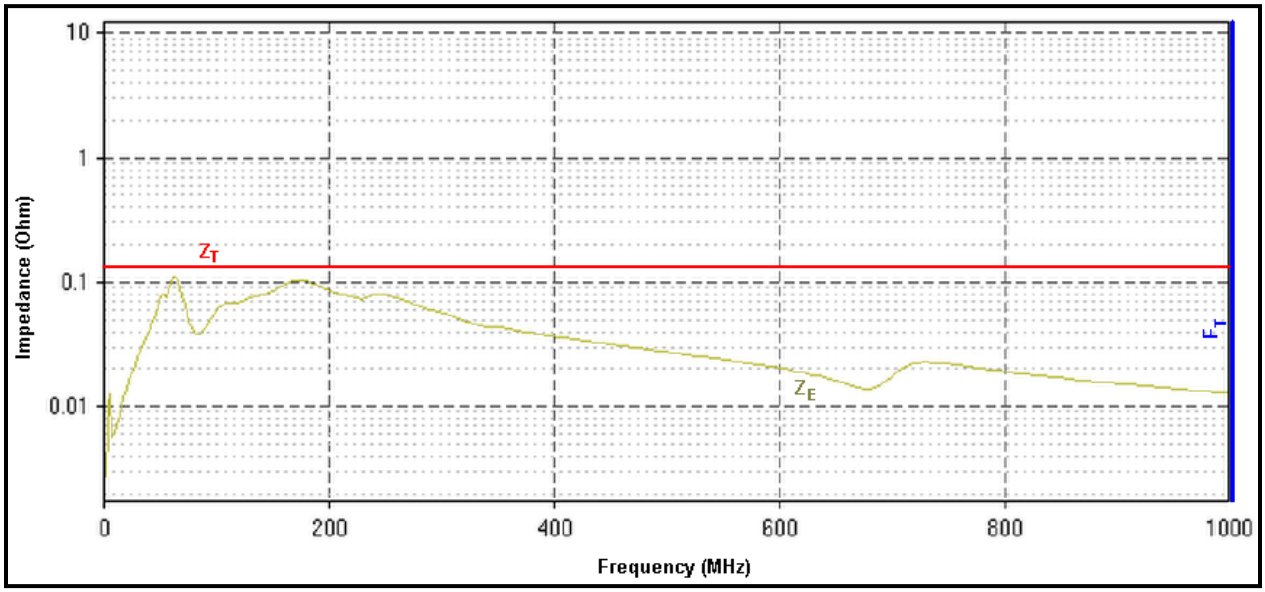
Figure 16. Power Integrity for Decoupling Capacitors



The objective is to iteratively solve for power integrity for effective impedance (Z_E) less than 120 mΩ for 1066-MHz frequency.

As shown in Figure 17, the target impedance (Z_T, red horizontal line) is 120 mΩ, the target frequency (F_T, blue vertical line) is 1000 MHz (the simulation has been performed from 0 to 1 GHz target frequency) and the effective impedance (Z_E, green line) is less than Z_T across the frequency, which shows that the combination of decoupling capacitors (Table 15) meets the target impedance for V_{DDQ}.

Figure 17. Power Integrity Simulation Results



Run a switching noise simulation to ensure that the power supply noise meets the noise target.

The decoupling capacitance for V_{DD}, V_{REF}, and V_{TT} can be identified using power integrity simulation tools. The selection of decoupling capacitors depends on board and device properties. Therefore, Cypress recommends that you perform power integrity simulation for high-speed systems before selecting the decoupling capacitor values for the respective power nets.

6.3.1 Board Design Recommendations for Decoupling Capacitors

Decoupling capacitors play a major role in SRAM performance. It is important to choose the correct value capacitor and place it on the board.

- Minimize wiring and lead inductances. In the PCB design, avoid long, narrow PCB traces because they increase inductance.
- Passing through a via is acceptable if the path has a lower inductance than an alternative longer trace.
- Keep capacitors on the same side of the board as the component if possible.
- Arrange capacitors by decreasing value such that the lowest value capacitor is as close to the power pin/power trace of the device as possible.
- Make sure that the capacitor value meets the voltage swing requirements, and that it gives a low-impedance path to ground in the intended frequency range of the application.

6.3.2 Termination Scheme Recommendation

Mismatched impedance causes signals to reflect along the transmission lines, which can cause ringing and jeopardize system reliability. The ringing reduces the dynamic range of the receiver (because of threshold shifts) and can cause false triggering. To eliminate reflections originating at the source, the source impedance must match the trace impedance.

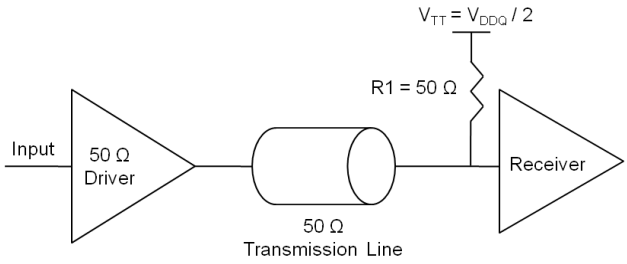
QDR-IV supports HSTL/SSTL (JESD8-16A compliant) and POD (JESD8-24 compliant) signaling with configurable on-die termination (ODT) for clock, address, command, and data inputs. Enable the ODT feature in QDR-IV to simplify board design by removing the termination resistors from the board. Designers can also disable the ODT feature and have termination resistors on the board for the input signals.

The following section discusses the recommended termination schemes for QDR-IV.

6.3.2.1 Termination for HSTL/SSTL Single-Ended Signal

QDR-IV has single-ended address and command signals. The recommended termination scheme is to use active pull-up termination to the V_{TT} voltage source at the load. Figure 18 shows an active pull-up termination scheme, where the terminating resistor (R1) is tied to a termination voltage (V_{TT}). In this scheme, the voltage (V_{TT}) is selected so that the output drivers can draw current from the high-level and low-level signals. However, this scheme requires a separate voltage source that can track V_{DDQ}, and sink and source currents to match the output transfer rates.

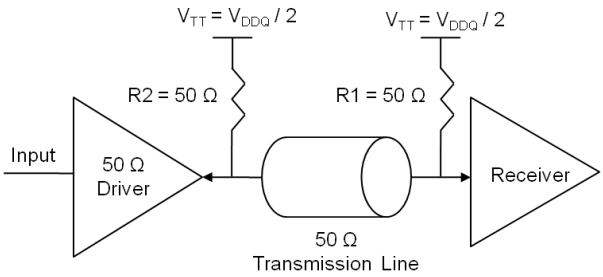
Figure 18. Active Pull-Up Termination Scheme Using 50 Ω



6.3.2.2 Termination for HSTL/SSTL Bidirectional Signal

QDR-IV has bidirectional data bus and data inversion signals. Figure 19 shows an active pull-up termination scheme, where the termination resistors (R1, R2) are tied to a termination voltage (V_{TT}). This is similar to the active pull-up termination scheme shown in Figure 18, with the only difference being the active pull-up is present on both ends. The active pull-up on the source end, shown in Figure 19, is actually load termination when the bus turns around.

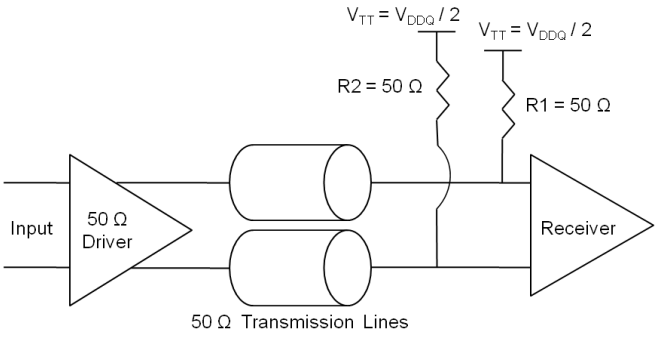
Figure 19. Active Pull-up Termination Scheme for Bidirectional I/Os Using 50 Ω



6.3.2.3 Termination for HSTL/SSTL Differential Signal

Figure 20 shows the recommended termination scheme for QDR-IV differential input clocks. It has an active pull-up termination scheme, where the termination resistors (R1, R2) are tied to a termination voltage (V_{TT}).

Figure 20. Active Pull-Up Termination Scheme for Differential Signal Using 50 Ω



6.3.2.4 Termination Requirement for POD Signaling

POD output drivers contain strong pull-down and weak pull-up strength. As a result, the POD signal needs an external pull-up termination resistor or on-die termination resistor. A weak pull-up on the driver side and pull-up termination resistor on the receiver side accomplishes the requirement of signal pull-up actions. POD signaling consumes less power than HSTL/SSTL (strong pull-up + strong pull-down) signaling.

If the output drivers are expected to demonstrate a 60-Ω pull-up drive impedance, the pull-down drivers would be expected to produce a 40-Ω pull-down drive impedance. Figure 21, Figure 22, and Figure 23 show the recommended termination schemes for POD single-ended, bidirectional, and differential signals.

Figure 21. POD Active Pull-up Termination Scheme for POD Single-Ended Signal Using 60 Ω

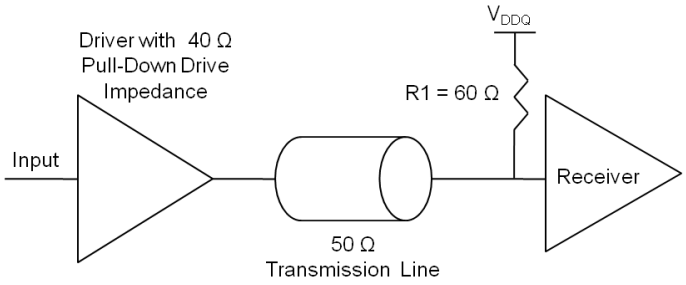


Figure 22. Active Pull-up Termination Scheme for POD Bidirectional I/Os Using 60 Ω

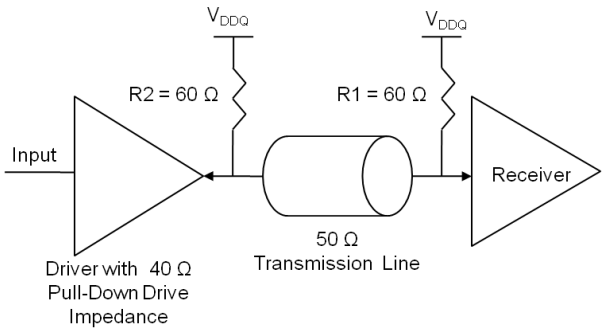
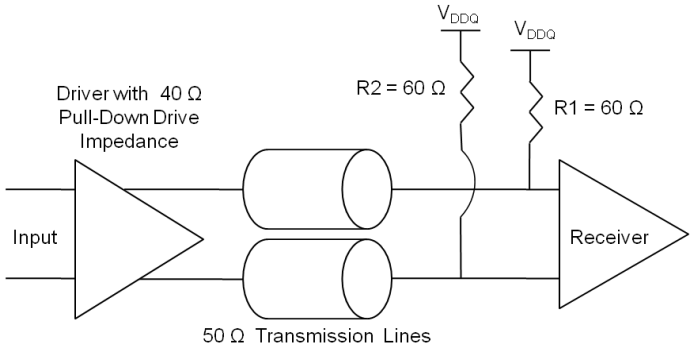


Figure 23. Active Pull-up Termination Scheme for POD Differential Signal Using 60 Ω



Always run signal integrity simulations before selecting the termination scheme and resistor values because it depends on board and device properties. In addition, place the termination resistors close to the device to reduce the stub length and, thereby, reduce reflections.

6.4 Board Layout Guidelines

To optimize performance, apply the following guidelines. Cypress recommends simulating your board implementation to get the precise delay numbers.

- Consider CK/CK# as a starting point and estimate the delay for the rest of the signals with respect to CK/CK#.
- All data, address, controls, and clock lines should be matched closely within +/- 50 ps within each bus type and +/- 50 ps between buses.
- DK_X clock should meet CK-to-DKx skew (t_{CKDK}) and address, command and data signals need to have proper setup/hold time (as per datasheet) with respect to the relevant clock.
- Cypress packages are routed to have all traces to within 5 ps of each other and they are closely matched and reflect an average length of 11.4 mm.
- All data, address, control, and clock lines should be routed to have 50 Ω +/- 10% impedance, and should have no impedance discontinuities. Traces in Cypress packages are drawn to have 50 Ω +/- 10%impedance.
- All three clocks in QDR-IV are differential clocks, so the clock traces must be routed differentially with 100 Ω differential impedance. As a result, the positive and negative clock signal traces will be identical and there should not be any skew between them.
- The DK/DK# write clocks and QK/QK# read clocks are associated with data groups based on the device organization. Therefore, route these clocks with their respective data groups on the same PCB layer to minimize the skew between them.
- Route CK/CK#, address, and command groups on the same PCB layer.
- All traces should be simulated to ensure similar and low insertion loss. Traces must be as wide as possible with adjustments to the dielectric thickness to reflect the 50-Ω impedance. Consider putting more ground vias in the proximity of signal vias to reduce insertion losses. Worst-case crosstalk victims must be simulated, ensuring that the noise levels are within specifications.

For more information on Cypress's ball grid array (BGA) packages and BGA layout guidelines, refer to the application note, AN79938- Design Guidelines for Cypress Ball Grid Array (BGA) Packaged Devices.

6.5 Output Data Valid Window

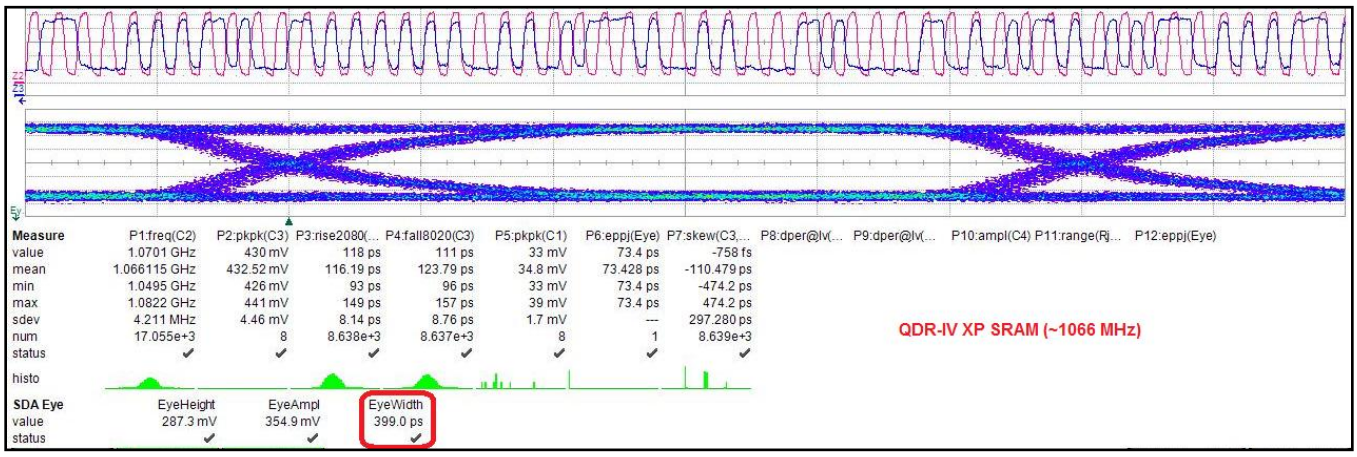
The QKx and QKx# clocks are associated with read data. The QKx and QKx# clocks are used as source-synchronous clocks for the double data rate DQx and DINVx pins, when acting as outputs for the read data.

Based on the characterization data, Cypress assures minimum 80% of data valid window with respect to half a clock cycle ($t_{CK}/2$) time for all QDR-IV devices. These values are used in the timing plan to determine the portion of the total data timing budget consumed by the QDR-IV device. Table 16 and Figure 24 show the data valid window values, measured on the characterization board for all QDR-IV SRAM devices.

Table 16. QDR-IV Data Valid Window Measurement (Characterization Board)

Device	Clock Frequency (t_{CK})	Half Clock Cycle ($t_{CK}/2$)	Measured Worst-Case Data Valid Window
QDR-IV HP SRAM	600 MHz = 1667 ps	834 ps	716 ps
	667 MHz = 1500 ps	750 ps	658 ps
QDR-IV XP SRAM	933 MHz = 1072 ps	536 ps	456 ps
	1066 MHz = 938 ps	469 ps	399 ps

Figure 24. Output Data Valid Window of x36 Device (Data Signal DQB[22])



7 Power Consumption and Junction Temperature

Calculate the junction temperature of QDR-IV based on the following equation:

$$T_J = P_d \theta_{JA} + T_A \quad \text{..... (1)}$$

Where,

θ_{JA} = Junction-to-ambient thermal resistance

T_A = Ambient temperature

P_d = Power dissipation

QDR-IV power consumption varies in the three following use cases:

- On-die termination (ODT) feature disabled
- ODT feature enabled with HSTL signaling
- ODT feature enabled with POD signaling

7.1 ODT Feature Disabled

The power consumption (P_d) is as follows:

P_d = Core Power + I/O Switching Power

$$= V_{DD} I_{DD} + \alpha f C_L V_{DDQ}^2 N \quad \text{..... (2)}$$

Where,

V_{DD} = Core voltage

I_{DD} = Active current

α = Activity factor, or the ratio of frequency at which outputs toggle to the clock frequency

= 1 for double-data-rate devices, such as QDR-IV SRAMs;

f = Operating frequency

C_L = External load capacitance

V_{DDQ} = I/O voltage

N = Number of I/Os that are switching

7.2 ODT Feature Enabled With HSTL Signaling

Enable the ODT feature with HSTL signaling by configuring the QDR-IV SRAM device. The power consumption (P_d) is as follows:

P_d = Core Power + I/O Switching Power + ODT Power (HSTL)

$$= V_{DD} I_{DD} + \alpha f C_L V_{DDQ}^2 N + (5/16) [V_{DDQ}^2 / R] N_{I/P} \quad \text{..... (3)}$$

Where,

R = Termination resistor

$N_{I/P}$ = Number of SRAM inputs with ODT

= 120, worst-case scenario for x36 data width option (Refer to)

= 84, worst-case scenario for x18 data width option (Refer to)

The following section describes the ODT power consumption for HSTL signaling.

7.2.1 ODT Power Consumption for HSTL Signaling

Figure 25 shows the HSTL signaling input termination circuit while the source is driving logic ‘0’. Figure 26 shows the HSTL signaling input termination circuit while the source is driving logic ‘1’. In either case, the power consumption is identical. The driver source impedance is represented by ’R’. The QDR-IV input ODT resistance is represented by ’2R’.This represents an impedance-matched circuit.

Figure 25. Input Termination Circuit for HSTL Signaling (Source Driving Logic ‘0’)

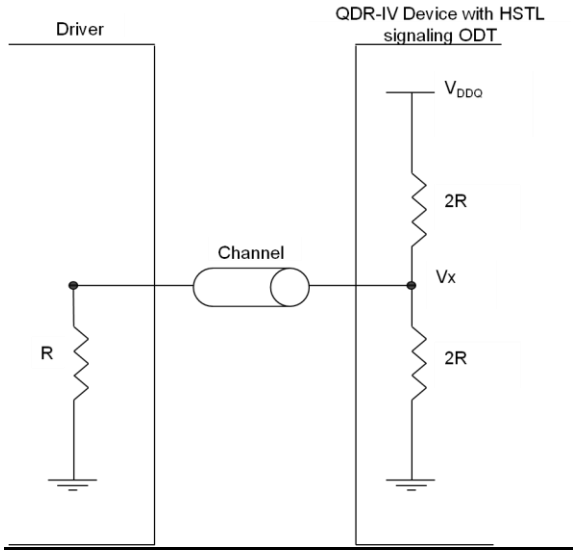
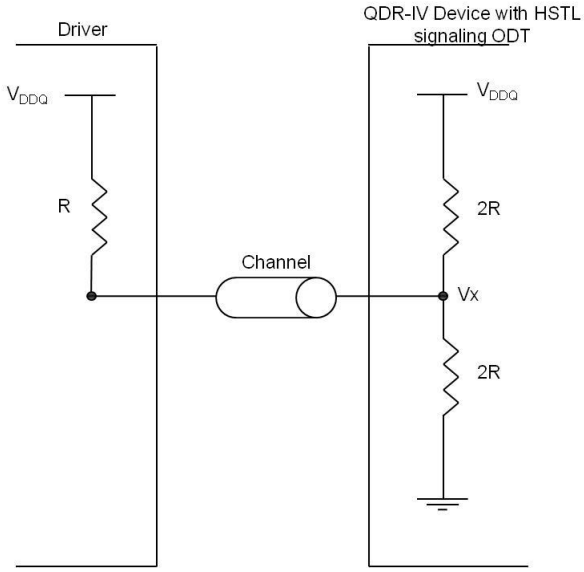


Figure 26. Input Termination Circuit for HSTL Signaling (Source Driving Logic '1')



Consider the source driving logic '1' (refer to Figure 26). The Voltage V_x is derived as follows:

$V_x = 2\ R \times V_{DDQ} / (2\ R + (R \parallel 2\ R))$

$= 2\ R \times V_{DDQ} / (2R + 2\ R/3)$

$= (3/4)\ V_{DDQ}$ …….. (4)

The power consumption in the pull-up and pull-down resistors is:

ODT Power = $\{(V_{DDQ} - V_x)^2 / 2R\} + \{(V_x)^2 / 2\ R\}$

$= 1/(32\ R) \times (V_{DDQ})^2 + (9/32\ R) \times (V_{DDQ})^2$ ……using equation (4)

$= 5/(16\ R) \times V_{DDQ}^2$

Therefore, ODT Power (HSTL)

$= 5/(16R) \times V_{DDQ}^2 \times$ (number of inputs with ODT resistors) $= (5/16)\ [V_{DDQ}^2 / R]\ N_{I/P}$ ….. (5)

7.3 ODT Feature Enabled With POD Signaling

Enable the ODT feature with POD signaling by configuring the QDR-IV SRAM device. The power consumption (P_d) is as follows:

P_d = Core Power + I/O Switching Power + ODT Power (POD)

$= V_{DD}\ I_{DD} + \alpha\ f\ C_L\ V_{DDQ}^2\ N + \beta\ [V_{DDQ}^2 / 4\ R]\ N_{I/P}$ …….. (6)

Where,

R = Termination resistor

$N_{I/P}$ = Number of SRAM inputs with ODT

= 117, worst-case scenario for the x36 data-width option (refer to)

= 81, worst-case scenario for the x18 data-width option (refer to)

β = [(Number of signals going LOW) / (Number of signals going LOW + Number of signals going HIGH)]

= 0.5, worst-case for β is 0.5 because POD is used with the Data Inversion and Address Inversion features. That means, only half the bits are driving LOW, at most. For example, if the controller tries to input 0000001111 bits without Data Inversion then β=0.6. But with data inversion, controller provides 1111110000 to QDR-IV and β=0.4.

The following section describes the ODT power consumption for POD signaling.

7.3.1 ODT Power Consumption for POD Signaling

POD works with the Data Inversion and Address Inversion feature. The advantage of POD is that it saves power when compared with HSTL.

Figure 27 shows the POD signaling input termination circuit while source is driving logic '0' and Figure 28 shows the POD signaling input termination circuit while source is driving logic '1' The input ODT resistance is represented by "R". This represents an impedance-matched circuit for POD signaling.

If the source is driving '1', then there will not be any ODT power consumption because the current cannot find the path to ground (Figure 22). If the source is driving '0' (Figure 27), then ODT power consumption will be as follows:

ODT Power (POD) = 0, when source is driving logic '1'

ODT Power (POD) = $(V_{DDQ}/2)^2 \times (1/R)$, when source is driving logic '0'

So, Average ODT Power (POD) = $\beta \times [V_{DDQ}^2/ 4R] \times$ (number of inputs with ODT resistors)

$= \boldsymbol{\beta\ [V_{DDQ}^2/\ 4\ R]\ N_{I/P}}$ ..... (7)

Figure 27. Input Termination Circuit for POD Signaling (Source Driving Logic '0')

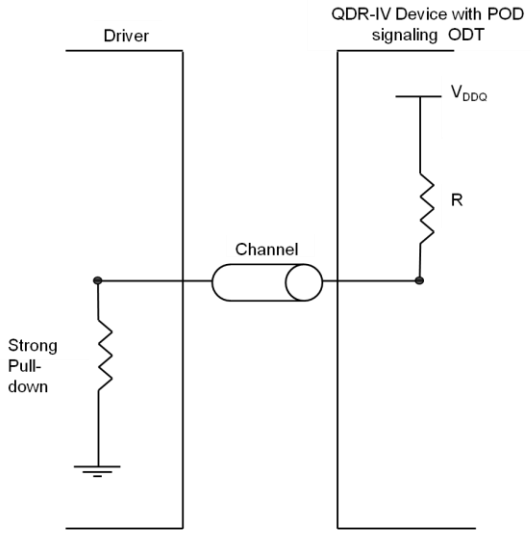
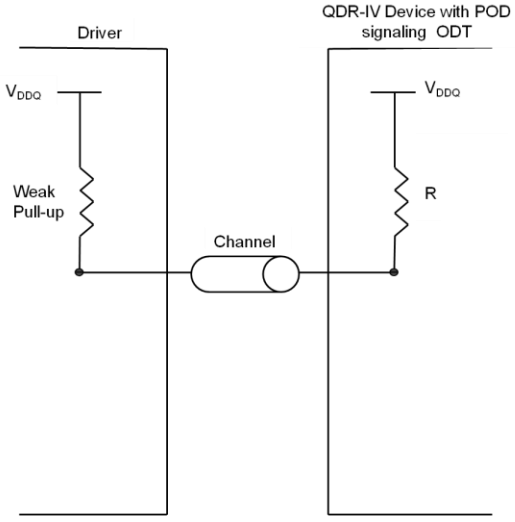


Figure 28. Input Termination Circuit for POD Signaling (Source Driving Logic '1')



7.4 Example of an x18 Device

This example uses the QDR-IV XP SRAM (Part Number CY7C4122KV13). Assuming that the device is running at 1066 MHz with a 5-pF capacitive load and all I/Os switching, the power dissipated for HSTL/SSTL signaling mode is calculated as follows:

P_d = Core Power + I/O Switching Power + ODT Power (HSTL)
Core power

$= V_{DD} \times I_{DD} = 1.3\ V \times 4100\ mA = 5.33\ W$

I/O switching power

$= \alpha\ f\ C_L\ V_{DDQ}^2\ N$

$= 1 \times 1066\ MHz \times 5\ pF \times (1.25\ V)^2 \times 36 = 0.3\ W$

ODT Power (HSTL with 50-Ω input impedance)

$= (5/16)\ [V_{DDQ}^2 / R]\ N_{I/P}$

$= (5/16) \times [(1.25\ V)^2 / 50\ \Omega] \times 84 = 0.82\ W$

Therefore, the total power dissipated under HSTL/SSTL signaling mode is 6.45 W.

The following steps calculate the power dissipated for the same device operating under POD signaling mode.

P_d = Core Power + I/O Switching Power + ODT Power (POD)
Core power

$= V_{DD} \times I_{DD} = 1.3\ V \times 4100\ mA = 5.33\ W$

I/O switching power

$= \alpha\ f\ C_L\ V_{DDQ}^2\ N$

$= 1 \times 1066\ MHz \times 5\ pF \times (1.25V)^2 \times 36 = 0.3\ W$

ODT Power (POD with 60-Ω input impedance)

$= \beta\ [V_{DDQ}^2 / 4\ R]\ N_{I/P}$

$= 0.5 \times [(1.25\ V)^2 / (4 \times 60\ \Omega)] \times 81 = 0.264\ W$

Therefore, the total power dissipated under POD signaling mode is 5.89 W.

This example verifies that the power consumed by the QDR-IV device with POD signaling mode is less than the HSTL/SSTL power consumption.

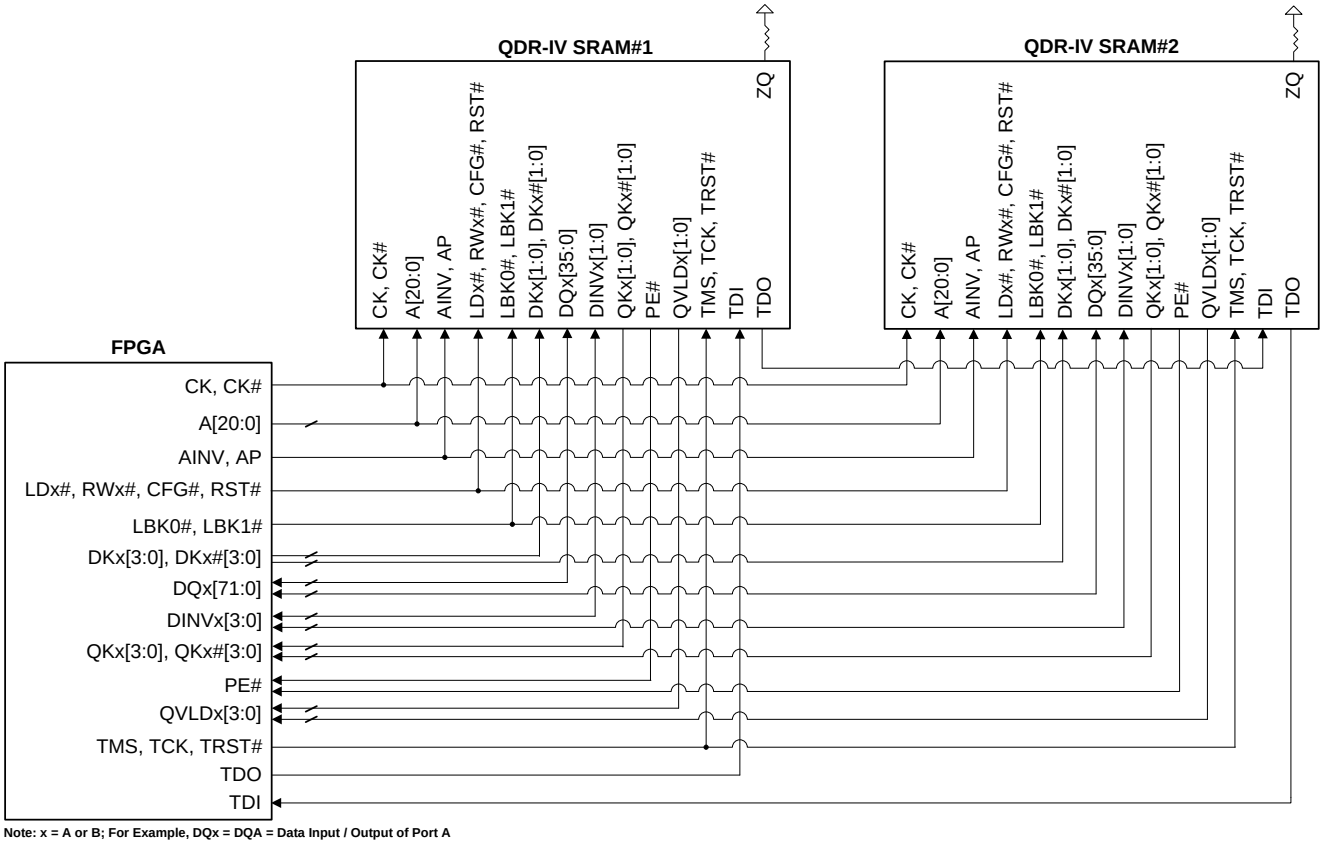
For more information, see the online tool for calculating the power consumption and junction temperature for synchronous SRAM products: http://www.cypress.com/?docID=23984

The maximum allowable junction temperature for QDR-IV SRAM is 125 °C. Use Heat Sink or Fan for QDR-IV if the junction temperature is above the maximum limit.

8 Width Expansion

QDR-IV SRAMs can be connected together to improve the memory bandwidth in the application. Figure 29 shows two QDR-IV (CY7C4142KV13) SRAMs connected in the width expansion configuration, which increases the memory bandwidth by factor of two.

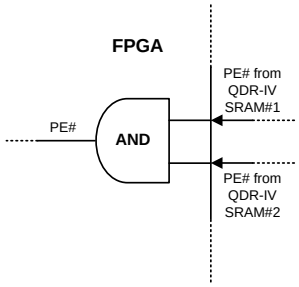
Figure 29. Width Expansion



8.1 Recommendation for Width Expansion Configuration

- All signals are shared between both QDR-IV devices excluding DK clocks, DQ, DINV, QK clocks, PE#, and QVLD.
- The PE# is an active LOW signal, which is set to zero within eight cycles (in QDR-IV XP SRAMs) or five cycles (in QDR-IV HP SRAMs) after the address parity error is detected. The memory controller can accept the PE# signal from both QDR-IV devices and perform a logic AND operation on them as shown Figure 30 to get the address parity error status.

Figure 30. PE# Configuration in Width Expansion



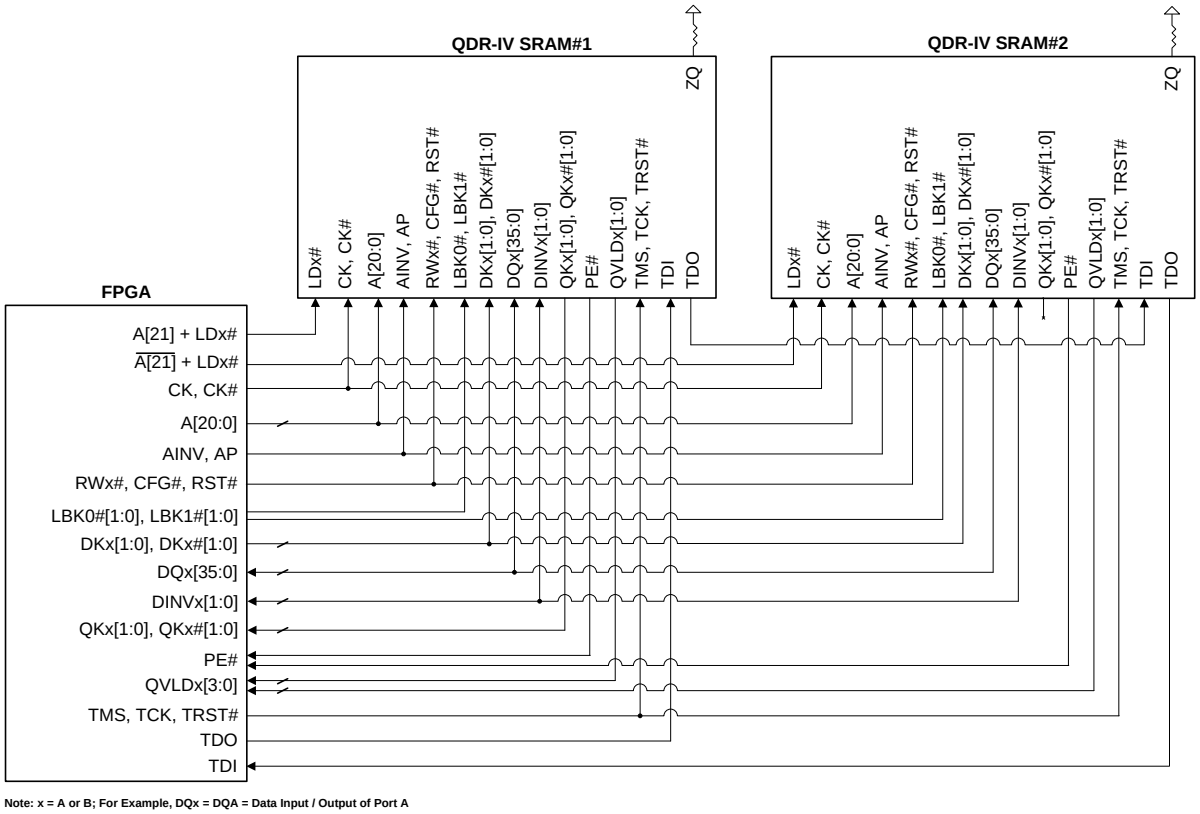
- Assuming trace impedance is 50 Ω,
  - QDR-IV input impedance should be 100 Ω for the shared input signals like CK/CK# clocks and Address. The rest of the inputs that are not shared (such as DK/DK# and DQ) should have 50-Ω input impedance.
  - QDR-IV output impedance should be 50 Ω.
  - FPGA input impedance should be 50 Ω.
  - FPGA output impedance should be 50 Ω.

- The trace length matching between two QDR-IV SRAMs to FPGA is very important for timing closure by system designers.

9 Depth Expansion

QDR-IV SRAMs can be connected together to increase the memory density in the application. Figure 31 shows two QDR-IV (CY7C4142KV13) SRAMs connected in the depth expansion configuration, which increases the memory density by factor of two.

Figure 31. Depth Expansion

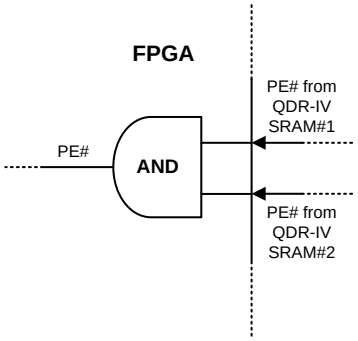


Note: x = A or B; For Example, DQx = DQA = Data Input / Output of Port A

9.1 Recommendations for Depth Expansion Configuration

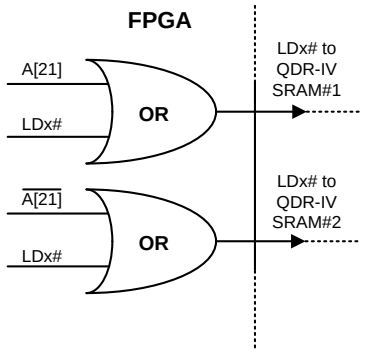
- All signals are shared between both QDR-IV devices excluding LBK0#, LBK1#, PE#, and QVLD.
  - QVLD and QK clocks are outputs that may assume HI or LO state, but would never tristate. The memory controller can use the QK clock from either memory device because QK clocks are free-running clocks.
  - The PE# is an active LOW signal, which is set to zero within eight cycles (in QDR-IV XP SRAMs) or five cycles (in QDR-IV HP SRAMs) after the address parity error is detected. In depth expansion topology, only one QDR-IV device would be active at a given point in time. Therefore, the memory controller can accept the PE# signal from both QDR-IV devices and perform a logic AND operation on them as shown in Figure 32 to get the address parity error status.

Figure 32. PE# Configuration in Depth Expansion



- In the depth expansion configuration, the extra address signal A[21] should act as a chip select to enable one device, while disabling the other. To select the single QDR-IV chip, A[21] needs to logically connected with LDx# in the memory controller as shown in Figure 33.

Figure 33. LDx# Configuration in Depth Expansion



- AP and AINV should be calculated based on A[20:0].
- Configuration and Loop back training should be performed separately for each QDR-IV SRAM device.
- Assuming trace impedance is 50 Ω,
  - QDR-IV input impedance should be 100 Ω for the shared inputs such as CK/CK# clocks and Address. The rest of the inputs that are not shared such as LDx# should have 50 Ω input impedance.
  - QDR-IV output impedance should be 50 Ω.
  - FPGA input impedance should be 100 Ω because one QDR-IV will be running at a time and it will see the input impedance from FPGA and another QDR-IV SRAM device.
  - FPGA output impedance should be 50 Ω.
- The trace length matching between two QDR-IV SRAMs to FPGA is very important for timing closure by system designers.

To simplify the layout, QDR-IV SRAM can be placed in a clamshell fashion wherein pairs of QDR-IV devices are located on opposite sides of the board.

10 QDR-IV Comparison with QDR-II+ and QDR-II+ Xtreme Devices

10.1 Architecture, Bandwidth, Power and Feature Comparison

Table 17 shows the architecture, bandwidth, RTR, power consumption, and feature comparison among QDR-II+, QDR-II+ Xtreme, and QDR-IV devices.

Table 17. QDR-IV Comparison with QDR-II+ and QDR-II+ Xtreme Devices

	Parameter	QDR-II+		QDR-II+ Xtreme		QDR-IV	
Architecture	Maximum density	144 Mb		72 Mb		144 Mb	
	Data burst length [1]	2	4	2	4	2	2b
	Banks	1		1		1	8
	Address per cycle	2	1	2	1	2	
	I/O ports	1R+1W		1R+1W		2 R/W	
	Write latency cycles	0,1		0,1		3	5
	Read latency cycles	2, 2.5		2.5		5	8
	I/O width/port	x9, x18, x36		x18, x36		x18, x36	
Bandwidth / RTR	Max clock frequency (MHz)	333	550	450	633	667	1066
	Max RTR (MT/s)	666	550	900	633	1334	2132
	Total maximum BW (Gbps)[2]	47.9	79.2	64.8	91.1	96	153.5
Power Consumption	V_{DD} (V)	1.8		1.8		1.3	
	V_{DDQ} (V)	1.8,1.5		1.8,1.5		1.1, 1.2,1.25	
	Core power consumption (W)[3]	2.1	2.7	2.6	3.0	4.2	5.9
	Total power consumption per chip (W)[4,5]	3.1	3.9	3.7	4.2	4.5	6.5
Features	I/O signaling	HSTL		HSTL		POD, HSTL/SSTL	
	On-chip ECC	No		No		Yes	
	Address parity	No		No		Yes	
	Address/Data bus inversion	No		No		Yes	
	Banking operation	No		No		No	Yes
	Package type	165-ball FBGA		165-ball FBGA		361-ball FCBGA	
	Package size (mm)	13 X 15		13 X 15		21 X 21	
	Dedicated data Input/Output clocks	No		No		Yes	
	Loopback mode for timing deskew training	No		No		Yes	

[1] With a single address, an entire series of accesses can take place in the burst operation; where Data Burst Length 2 = Burst of two data accesses with a single address, 4 = Burst of four data accesses with a single address; and 2b = Burst of two data accesses with a single address (banking operation)

[2] Maximum Bandwidth = Maximum frequency x Data Rate x Maximum Bus Width x Number of Ports

[3] Core Power = V_{DD}(Typ) x I_{DD}(Max)

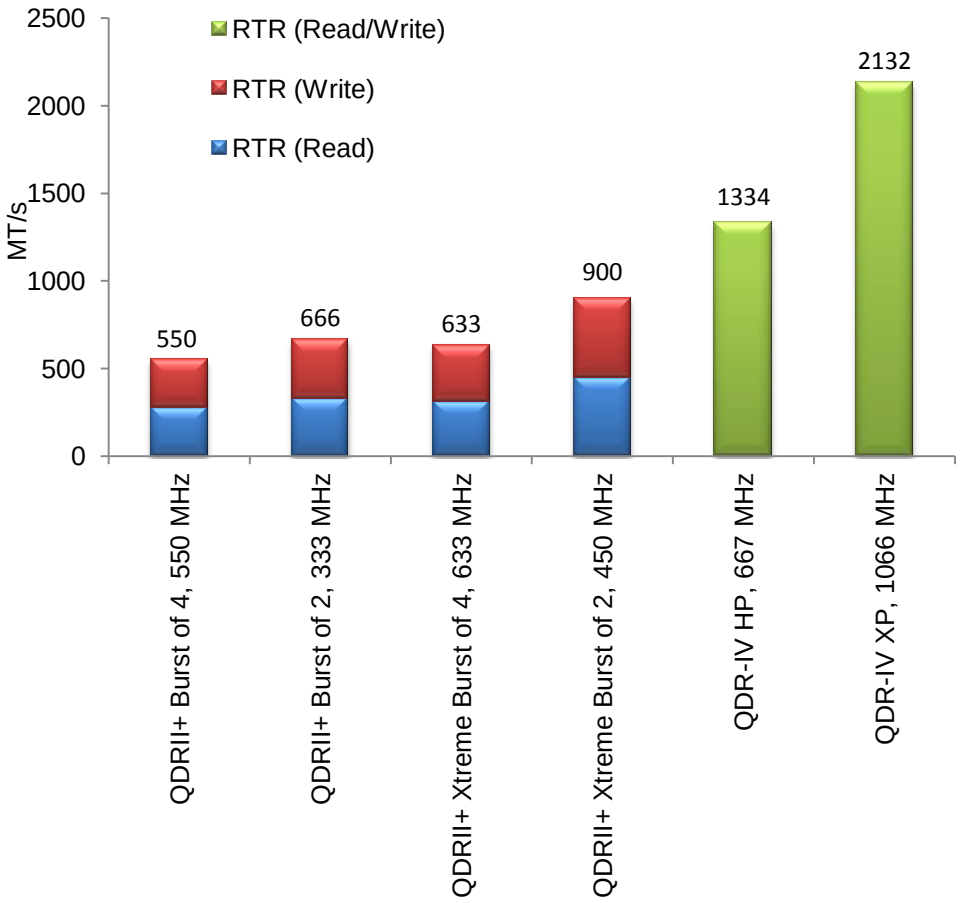
[4] Total Power Consumption = Core Power + I/O Power (Typ. V_{DDQ}, 5-pF load capacitance, all switching I/Os, and mentioned highest frequency assumptions)

[5] To calculate the total power consumed by SRAM, refer to the tool: http://www.cypress.com/?docID=23984

10.2 RTR Comparison

The banked mode operation allows QDR-IV XP SRAM to operate up to 1066 MHz, which provides an RTR of up to 2132 MT/s. Figure 34 shows the improvement in RTR from the QDR-II+ to the QDR-IV in this SRAM family.

Figure 34. Comparing RTR Among QDR SRAMs



10.3 Pin Differences with QDR®-II, QDR-II+, and QDR-IV Devices

There are very few pin differences between the QDR-II and QDR-II+ devices. However, QDR-IV introduces several new features that cause differences in pin information when compared with QDR-II and QDR-II+ devices. Table 18 compares 144M, x18, Burst of 2 QDR-II, QDR-II+, and QDR-IV devices and Table 19 compares 144M, x36, Burst of 2 QDR-II, QDR-II+ and QDR-IV devices.

Table 18. Pin Differences with x18 QDR-II, QDR-II+, and QDR-IV

QDR- II (x18)			QDR- II+ (x18)				QDR-IV (x18)			Comments for QDR-IV
Pin Name		No. of Pins	Pin Name		No. of Pins (With ODT)	No. of Pins (Without ODT)	Pin Name		No. of Pins	
Data input pins	D[x:0]	18	Data input pins	D[x:0]	18	18	Data input/output for Port A	DQA[x:0]	18	QDR-IV has two bi-directional ports
Data output pins	Q[x:0]	18	Data output pins	Q[x:0]	18	18	Data input/output for Port B	DQB[x:0]	18	
Address pins	A[x:0]	22	Address pins	A[x:0]	22	22	Address pins	A[x:0]	22	
Write port select	WPS#	1	Write port select	WPS#	1	1	Synchronous read/write input for Port A	RWA#	1	QDR-IV has synchronous read/write input for each port
Read port select	RPS#	1	Read port select	RPS#	1	1	Synchronous read/write input for Port B	RWB#	1	
Byte write select	BWS#[x:0]	2	Byte write select	BWS#[x:0]	2	2				
Input clocks	K/K#	2	Input clocks	K/K#	2	2	Address/ command input clock	CK/CK#	2	Input clock for address and commands
Input clocks for output data	C/C#	2					Data input clock	DKA[1:0], DKA#[1:0], DKB[1:0], DKB#[1:0]	8	Input clock for data input

QDR- II (x18)			QDR- II+ (x18)				QDR-IV (x18)			Comments for QDR-IV
Pin Name		No. of Pins	Pin Name		No. of Pins (With ODT)	No. of Pins (Without ODT)	Pin Name		No. of Pins	
Echo Clocks	CQ/CQ#	2	Echo clocks	CQ/CQ#	2	2	Data output clock	QKA[1:0], QKA#[1:0], QKB[1:0], QKB#[1:0]	8	Output clock for data output
Output impedance matching input	ZQ	1	Output impedance matching input	ZQ	1	1	Output impedance matching input	ZQ/ZT	1	
PLL turn off	DOFF#	1	PLL turn off	DOFF#	1	1				
JTAG pin	TDI	1	JTAG pin	TDI	1	1	JTAG pin	TDI	1	
JTAG pin	TDO	1	JTAG pin	TDO	1	1	JTAG pin	TDO	1	
JTAG pin	TMS	1	JTAG pin	TMS	1	1	JTAG pin	TMS	1	
JTAG pin	TCK	1	JTAG pin	TCK	1	1	JTAG pin	TCK	1	
							JTAG pin	TRST#	1	QDR-IV has TRST# pin as a reset pin for JTAG and TRST# is not optional for QDR-IV
No Connection pins	NC	38	No Connection pins	NC	38	39	Do Not Use pins	DNU	40	DNU is same as NC pins in QDR-II and QDR-II+
Reference voltage input	V_{REF}	2	Reference voltage input	V_{REF}	2	2	Reference voltage input	V_{REF}	6	
Core power supply pins	V_{DD}	10	Core power supply pins	V_{DD}	10	10	Core power supply pins	V_{DD}	44	

QDR- II (x18)			QDR- II+ (x18)				QDR-IV (x18)			Comments for QDR-IV
Pin Name		No. of Pins	Pin Name		No. of Pins (With ODT)	No. of Pins (Without ODT)	Pin Name		No. of Pins	
Power supply inputs for the outputs of the device	V_{DDQ}	16	Power supply inputs for the outputs of the device	V_{DDQ}	16	16	Power supply inputs for the outputs of the device	V_{DDQ}	64	
Ground pins	V_{SS}	25	Ground pins	V_{SS}	25	25	Ground pins	V_{SS}	106	
			Valid output indicator	QVLD	1	1	Valid output indicator	QVLDA[1:0], QVLDB[1:0]	4	
			ODT input pin	ODT	1					
							Address parity input	AP	1	AP is used to provide even parity across the address pins of QDR-IV. The PE# pin indicates an address parity error has occurred. Address parity function is optional and can be enabled or disabled in the configuration registers.
							Address parity error flag	PE#	1	
							Address inversion state for address bus	AINV	1	Address Inversion feature is optional in QDR-IV. It is configurable through configuration registers in the memory.
							Data inversion state for DQ data bus	DINVA[1:0], DINVB[1:0]	4	Data inversion feature is optional in QDR-IV. It is configurable through configuration registers in the memory.

QDR- II (x18)			QDR- II+ (x18)				QDR-IV (x18)			Comments for QDR-IV
Pin Name		No. of Pins	Pin Name		No. of Pins (With ODT)	No. of Pins (Without ODT)	Pin Name		No. of Pins	
							Synchronous load input	LDA#, LDB#	2	LDA# enables commands for data port A, and LDB# enables commands for data port B. When the command is disabled, new commands are ignored, but internal operations continue.
							Configuration bit	CFG#	1	This pin is used to configure different mode registers of QDR-IV
							Active LOW asynchronous RST	RST#	1	RST# pin to reset the QDR-IV
							Loopback mode	LBK0#, LBK1#	2	Loopback mode for control and address/command/clock deskewing
Total number of active pins (signals)		74			74	73			101	
Total number of power and Ground pins		53			53	53			220	
NC/DNU		38			38	39			40	
Total number of pins		165			165	165			361	

Not Applicable

Table 19. Pin Differences Between x36 QDR-II, QDR-II+, and QDR-IV

QDR- II (x36)			QDR- II+ (x36)				QDR-IV (x36)			Comments for QDR-IV
Pin Name		No. of Pins	Pin Name		No. of Pins (With ODT)	No. of Pins (Without ODT)	Pin Name		No. of Pins	
Data input pins	D[x:0]	36	Data input pins	D[x:0]	36	36	Data input/output for Port A	DQA[x:0]	36	QDR-IV has two bi-directional ports
Data output pins	Q[x:0]	36	Data output pins	Q[x:0]	36	36	Data input/output for Port B	DQB[x:0]	36	
Address pins	A[x:0]	21	Address pins	A[x:0]	21	21	Address pins	A[x:0]	21	
Write port select	WPS#	1	Write port select	WPS#	1	1	Synchronous read/write input for Port A	RWA#	1	QDR-IV has synchronous read/write input for each port
Read port select	RPS#	1	Read port select	RPS#	1	1	Synchronous read/write input for Port B	RWB#	1	
Byte write select	BWS#[x:0]	4	Byte write select	BWS#[x:0]	4	4				
Input clocks	K/K#	2	Input clocks	K/K#	2	2	Address/ command input Clock	CK/CK#	2	Input clock for address and commands
Input clocks for output data	C/C#	2					Data input clock	DKA[1:0], DKA#[1:0], DKB[1:0], DKB#[1:0]	8	Input clock for data input
Echo clocks	CQ/CQ#	2	Echo clocks	CQ/CQ#	2	2	Data output clock	QKA[1:0], QKA#[1:0], QKB[1:0], QKB#[1:0]	8	Output clock for data output
Output impedance matching input	ZQ	1	Output impedance matching input	ZQ	1	1	Output impedance matching input	ZQ/ZT	1	

QDR- II (x36)			QDR- II+ (x36)				QDR-IV (x36)			Comments for QDR-IV
Pin Name		No. of Pins	Pin Name		No. of Pins (With ODT)	No. of Pins (Without ODT)	Pin Name		No. of Pins	
PLL turn off	DOFF#	1	PLL turn off	DOFF#	1	1				
JTAG pin	TDI	1	JTAG pin	TDI	1	1	JTAG pin	TDI	1	
JTAG pin	TDO	1	JTAG pin	TDO	1	1	JTAG pin	TDO	1	
JTAG pin	TMS	1	JTAG pin	TMS	1	1	JTAG pin	TMS	1	
JTAG pin	TCK	1	JTAG pin	TCK	1	1	JTAG pin	TCK	1	
							JTAG pin	TRST#	1	QDR-IV has TRST# pin as a reset pin for JTAG and TRST# is not optional for QDR-IV
No Connection pins	NC	1	No Connection pins	NC	1	2	Do Not Use pins	DNU	5	DNU is same as NC pins in QDR-II and QDR-II+
Reference voltage input	V_{REF}	2	Reference voltage input	V_{REF}	2	2	Reference voltage input	V_{REF}	6	
Core power supply pins	V_{DD}	10	Core power supply pins	V_{DD}	10	10	Core power supply pins	V_{DD}	44	
Power supply inputs for the outputs of the device	V_{DDQ}	16	Power supply inputs for the outputs of the device	V_{DDQ}	16	16	Power supply inputs for the outputs of the device	V_{DDQ}	64	
Ground pins	V_{SS}	25	Ground pins	V_{SS}	25	25	Ground pins	V_{SS}	106	

QDR- II (x36)			QDR- II+ (x36)				QDR-IV (x36)			Comments for QDR-IV
Pin Name		No. of Pins	Pin Name		No. of Pins (With ODT)	No. of Pins (Without ODT)	Pin Name		No. of Pins	
			Valid output indicator	QVLD	1	1	Valid output indicator	QVLDA[1:0], QVLDB[1:0]	4	
			ODT input pin	ODT	1					
							Address parity input	AP	1	AP is used to provide even parity across the address pins of QDR-IV. The PE# pin indicates an address parity error has occurred. Address parity function is optional and can be enabled or disabled in the configuration registers.
							Address parity error flag	PE#	1	
							Address inversion state for address bus	AINV	1	Address Inversion feature is optional in QDR-IV. It is configurable through configuration registers in the memory.

QDR- II (x36)			QDR- II+ (x36)				QDR-IV (x36)			Comments for QDR-IV
Pin Name		No. of Pins	Pin Name		No. of Pins (With ODT)	No. of Pins (Without ODT)	Pin Name		No. of Pins	
							Data inversion state for DQ data bus	DINVA[1:0], DINVB[1:0]	4	Data Inversion feature is optional in QDR-IV. It is configurable through configuration registers in the memory.
							Synchronous load input	LDA#, LDB#	2	LDA# enables commands for data port A, and LDB# enables commands for data port B. When the command is disabled, new commands are ignored, but internal operations continue.
							Configuration bit	CFG#	1	This pin is used to configure different mode registers of QDR-IV
							Active LOW asynchronous RST	RST#	1	RST# pin to Reset the QDR-IV

QDR- II (x36)			QDR- II+ (x36)				QDR-IV (x36)			Comments for QDR-IV
Pin Name		No. of Pins	Pin Name		No. of Pins (With ODT)	No. of Pins (Without ODT)	Pin Name		No. of Pins	
							Loopback mode	LBK0#, LBK1#	2	Loopback mode for control and address/ command/ clock deskewing
Total number of active pins (signals)		111			111	110			136	
Total number of power pins		53			53	53			220	
NC/DNU		1			1	2			5	
Total number of pins		165			165	165			361	

Not Applicable

11 Summary

This design guide provided an overview of the QDR-IV SRAM family, covering:

- QDR-IV operation
- Recommendations for QDR-IV board design
- Power and junction temperature calculation
- Comparison between the QDR-IV, QDR-II+, and QDR-II family of devices

12 References

1. QDR®-IV: The Next Generation of the Highest-Performance Memory Standard for Leading-Edge Networking Systems
2. AN4065 - QDR®-II, QDR-II+, DDR-II, and DDR-II+ Design Guide
3. AN79938 - Design Guidelines for Cypress Ball Grid Array (BGA) Packaged Devices

A Appendix

The following table shows the number of pins that have on-die termination (ODT) in QDR-IV SRAM devices.

Pin Names	Number of Pins (x36 Device)	Number of Pins (x18 Device)	Group Name
CK, CK#	2	2	Clock Input Group
A[x:0]	25	25	Address/Command Input Group
AP	1	1	Address/Command Input Group
AINV	1	1	Address/Command Input Group
DKA[1:0], DKA#[1:0], DKB[1:0], DKB#[1:0]	8	8	Clock Input Group
DQA[x:0], DQB[x:0]	72	36	Data Input Group
DINVA[1:0], DINVB[1:0]	4	4	Data Input Group
LDA#, LDB#	2	2	Address/Command Input Group
RWA#, RWB#	2	2	Address/Command Input Group
CFG#	1	1	Address/Command Input Group
LBK0#, LBK1#	2	2	Address/Command Input Group
TOTAL[6]	**120**	**84**	

[6] If the pin is driving HIGH under POD signaling, then the ODT circuit does not consume any power. Therefore, the total number of ODT pins ($N_{I/P}$) is 117 (x36 option) and 81 (x18 option) for POD signaling because LBKx# and CFG# pins are always HIGH during normal operation.

Document History

Document Title: AN84060 - QDR®-IV Design Guide

Document Number: 001-84060

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4053300	PRIT	07/08/2013	New Specification
*A	4271623	PRIT	02/06/2014	Changed Title to QDR-IV Design Guide Changed MPNs from CY7C4*2*KV12, CY7C4*4*KV12 to CY7C4*2*KV13, CY7C4*4*KV13 Changed QDR-IV GT SRAM name to QDR-IV XP SRAM Changed non-banked QDR-IV SRAM name to QDR-IV HP SRAM Modified Introduction Added Figure 1 Modified Interface Diagram Modified Read and Write Timing Diagram Modified QDR-IV HP and QDR-IV XP SRAM Write/Read Operation Diagram Added Board Design Guidelines section Added Power Consumption and Junction Temperature Calculation Modified Comparing RTR among QDR SRAMs figure
*B	4316406	PRIT	03/21/2014	Post to web.
*C	4546293	DEVM	11/05/2014	Added the Deskew Training Sequences section Updated the Banking Operation section Added a footnote added for RTR Added the Bus Turnaround Considerations section Removed Table-15
*D	5021894	PRIT	12/01/2015	Added sections: Width Expansion and Depth Expansion Updated the References section Updated template
*E	5416184	PRIT	08/26/2016	Updated Design Recommendations for Memory Controller section with QDR-IV controller availability Updated Decoupling Capacitors Requirements and included Figure 14 to show package decoupling capacitors on the chip Appendix: Categorized input pin in the group Updated template
*F	5705813	AESATMP9	04/21/2017	Updated logo and copyright.

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