Design guidelines for Infineon quad flat no-lead (QFN) packaged devices

About this document

Scope and purpose

AN72845 offers guidelines for the design, manufacturing, and handling of Infineon quad flat no-lead (QFN) packages on printed circuit boards (PCBs) and flexible printed circuits (FPC).

Intended audience

This document is intended for engineers who design and develop surface mount technology (SMT) printed circuit boards (PCBs) or flexible printed circuits (FPCs), with QFN-packaged devices.

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1 Introduction

This application note presents guidelines that document best practices for QFN assembly and PCB/FPC design, to ensure strong manufacturing yield and reliable performance. Because many factors influence manufacturing, performance, and reliability of the final electronic product, you should validate these guidelines using your own product development and qualification process. These are the major influencing factors:

- PCB/FPC and solder/flux material selection
- Manufacturing equipment
- Application specification requirements

2 Why choose QFN over leaded packages?

Infineon QFN-packaged devices offer a near chip-sized footprint with a high I/O count compared with standard leaded IC packages, such as small outline package (SOP) or quad flat package (QFP) devices.

For example, the footprint of a 32-lead thin quad flat pack (TQFP) is 81 mm^2 (7.0 mm × 7.0 mm body with a 9.0 mm × 9.0 mm footprint, including package leads). The equivalent QFN with 32 leads (**Figure 1**) is only 25 mm^2 (5.0 mm × 5.0 mm body with no extended leads). As a result, you can reduce the footprint of the PCB by 70 percent.

QFN packages are designed to be soldered directly onto PCB or FPC substrates. Because of the exposed metal pad on the bottom of the package, QFN-packaged devices offer better thermal dissipation. In addition, QFN packages offer excellent electrical performance because their leads are shorter than those of extended lead packages.

Infineon QFN-packaged devices have a contact pitch of 0.5 mm, 0.4 mm, or 0.35 mm and a thickness of 1.0 mm, 0.6 mm, or 0.4 mm, depending on the product.

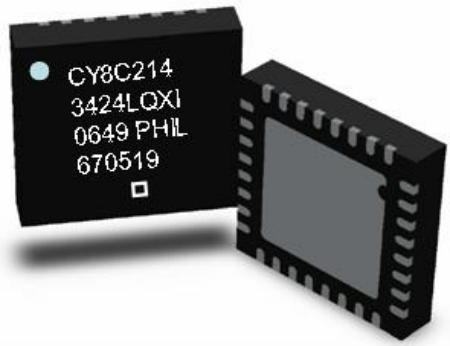


Figure 1 Example of a Infineon QFN product

Note: Infineon QFN-packaged devices are 100 percent green and are Pb-free, in compliance with RoHS.

3 Thermal considerations

Thermal design historically has meant finding out which components in the system generate the most heat and coupling them to a heat sink. However, with power systems shrinking and becoming more cost-sensitive, heat sinks have become a less attractive option. You need to use the PCB as a heat sink. As with other heat sinks, heat is transferred through the PCB in the form of conduction, convection, and radiation.

A QFN package has an integrated thermal pad on the bottom that offers a low resistance path to conduct heat out of the device. The heat is conducted to whatever structure is attached to this pad. Typically, the pad connects to a copper landing on the PCB through a solder joint, effectively turning the PCB into a heat sink. In a QFN component, this thermal pad is also electrically connected to power ground. (Refer to a device data sheet for details on electrical specifications.)

To optimize performance and system reliability, ensure that the device is both thermally and electrically coupled to the PCB. Not only does the heat need to conduct through the PCB, it also must effectively transfer into the surroundings and away from the device. Therefore, this step is critical to ensuring a robust thermal pad and PCB design.

3.1 Thermal system

The QFN device and the surrounding PCB area under it together make up the “thermal system”, which optimizes heat conduction, as **Figure 2** shows.

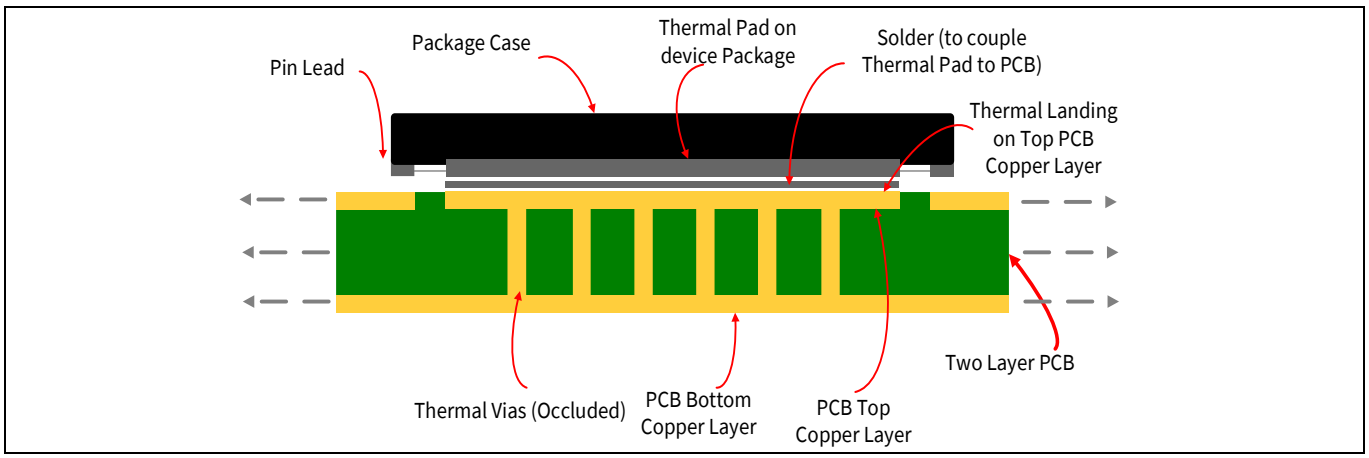


Figure 2 Thermal system cross-sectional view

The thermal system consists of:

- The exposed thermal pad integrated on the bottom of the QFN package
- A thermal landing on the PCB top layer
- An array of vias designed to transfer heat from the top to the bottom layer of the PCB
- A layer of solder paste (interface material) used to couple the pad to the landing.

Heat flow paths can be considered as lumped heat flow paths, as **Figure 3** shows. Although this model is not accurate for heat flow, it emphasizes that most of the heat is conducted through the via array into the PCB.

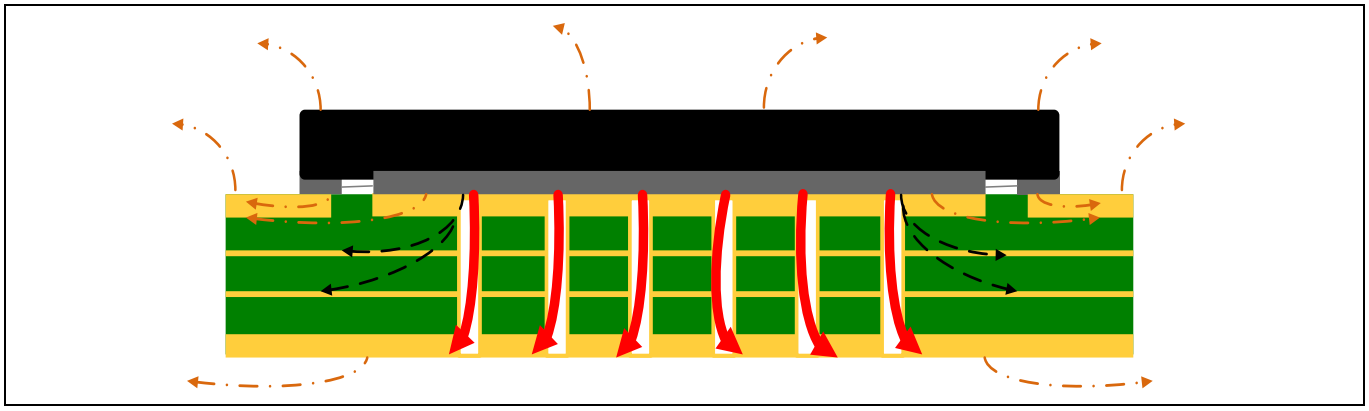


Figure 3 Heat flow paths

3.2 Optimizing heat flow paths

The goal of a good thermal design is to optimize several heat flow paths:

- Through the thermal vias
- Through the PCB area surrounding the device
- Into the ambient or system enclosure

3.2.1 Heat flow through thermal vias

Lay out the thermal landing carefully, because it is part of the most critical path for heat conduction. Here is an example of a recommended thermal landing layout using a 6.10 mm × 6.10 mm QFN exposed pad as a reference.

The thermal landing on top layer of the PCB should be slightly smaller than the QFN exposed pad (6.05 mm × 6.05 mm in this example). A similar copper pour should also be on the bottom layer, which should ideally extend into a large copper plane without any cuts or breaks.

The recommended optimum number of vias is 36. Use a 6 × 6 via array, as **Figure 4** shows.

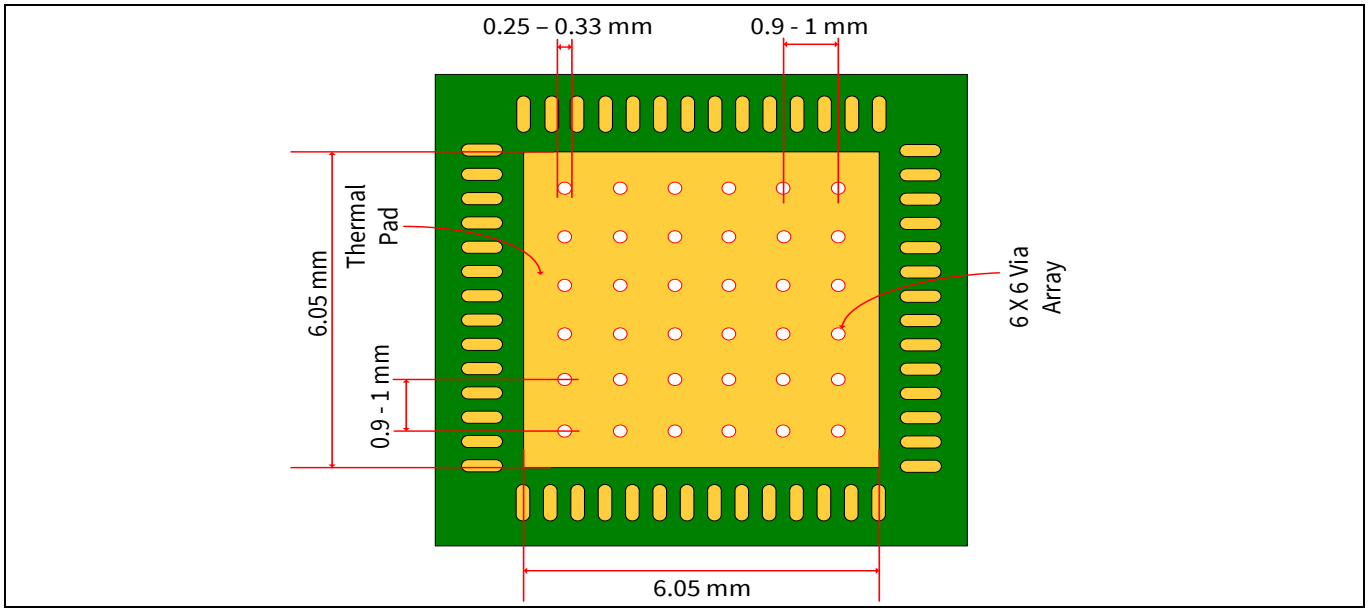


Figure 4 QFN landing pattern with 6 x 6 via array

There is no thermal relief (web or spoke connections) on vias. There should be a continuous copper ring around the vias, as **Figure 5** shows.

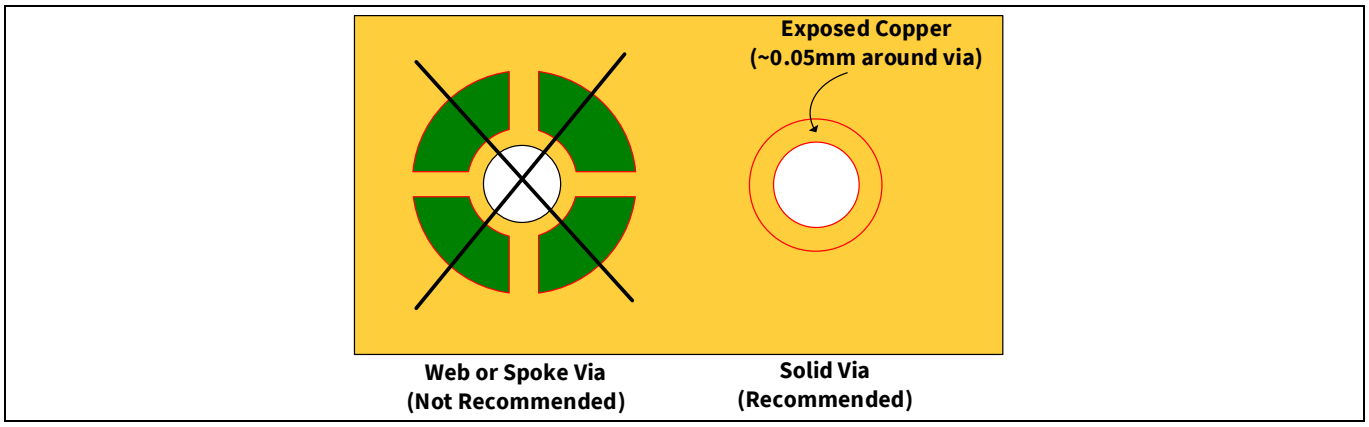


Figure 5 Thermal via

Do not completely cover vias with solder mask because it can lead to excessive voiding.

To avoid wicking, vias should be internally plated with copper and filled with solder. They may be filled with thermally conductive materials such as copper or silver epoxy to further improve thermal conductivity.

3.2.2 Heat flow through PCB area surrounding the device

Signal routing degrades heat conduction through the top copper plane. Improve thermal conductivity of the plane by filling unused PCB areas surrounding the device with copper. Note that copper pours should connect to appropriate electrical connections.

Connect the thermal landing on the top layer of the PCB to power ground copper pours to improve heat conductivity and satisfy device electrical specifications. The power ground copper pour connections must be made to all inner and outer layers to maximize heat conduction through the PCB.

For additional thermal and QFN considerations for PSoC™ devices, see **AN61290 - PSoC™ 3 and PSoC™ 5LP hardware design considerations**, and **AN88619 - PSoC™ 4 MCU hardware design considerations**.

4 QFN PCB guidelines

Details of package outlines for Infineon QFN products are available in the product datasheets.

4.1 Land pattern recommendations

Infineon QFN packages use two kinds of contact designs, as **Figure 6** shows. One is standard, in which the side metal and bottom leads meet at the package edges. The other uses pull-back leads, in which the side metal and bottom metal are etched, resulting in leads that are shorter by 0.1 mm.

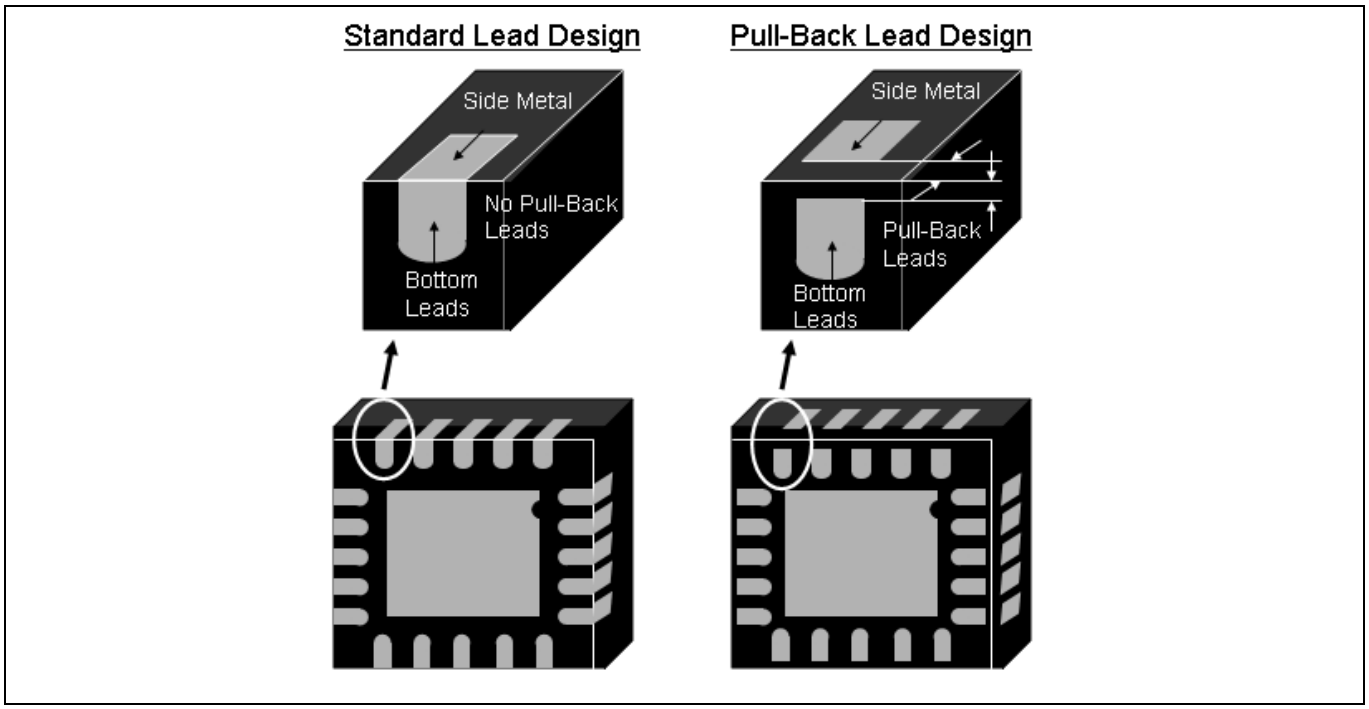


Figure 6 QFN package contact design options

Standard leads (without pull-backs) are the most common for Infineon QFN products. The longer leads maximize the solder joint area between the leads and the PCB pads. Because the lead and solder extend to the edge of the package, you can visually inspect the solder joint.

Peripheral solder pads on the mating board should be slightly larger than the package leads and similar in shape. **Figure 7** shows a typical PCB land pattern. Ensure that land patterns follow industry standard practices, such as those documented in IPC-SM-782.

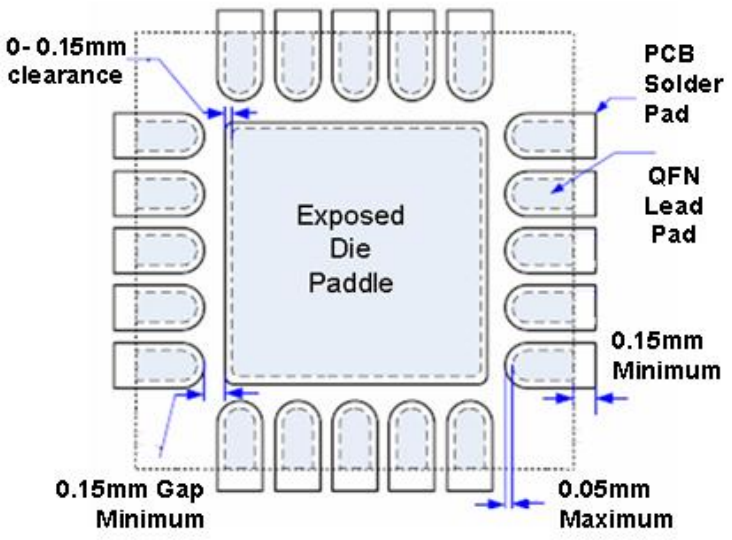


Figure 7 Solder pad design on PCB

PCB fabrication for surface mount assemblies uses one of the following types of pads/land patterns (**Figure 8**):

- Non-solder mask defined (NSMD) – The metal pad is smaller than the solder mask opening
- Solder mask defined (SMD) – The solder mask opening is smaller than the metal pad

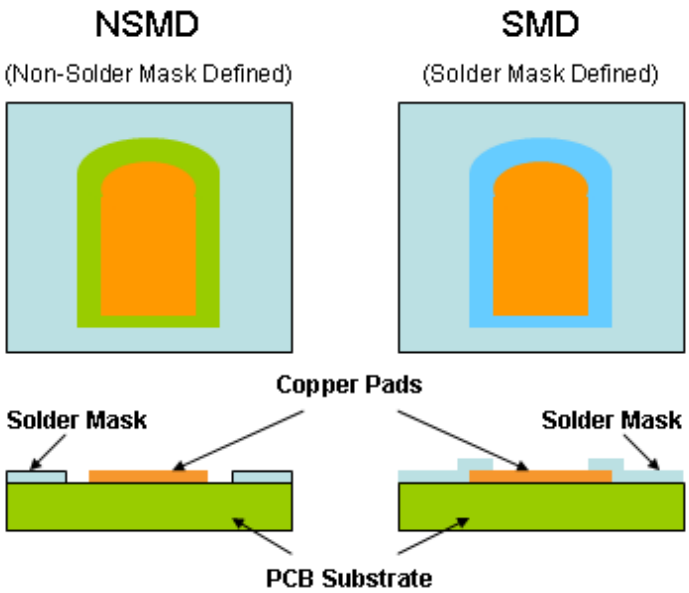


Figure 8 NSMD and SMD land patterns

You must choose between NSMD and SMD for your PCB depending on the overall product reliability and manufacturing requirement. Typically, NSMD land patterns are more reliable for board-level mechanical performance; however, the NSMD pad is prone to peeling off during rework processing.

4.2 Placement of PCB traces

Avoid placing traces close to the device. Doing so increases the thermal resistance and restricts the heat flow away from the device.

Also, avoid having traces on a layer that is used as a thermal plane for heat removal. If you must route on a thermal plane, consider the following options shown in **Figure 9**:

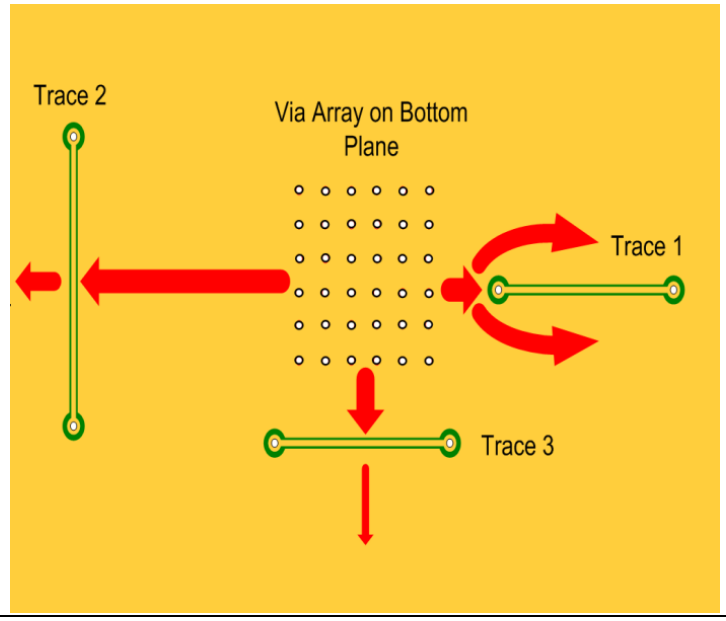


Figure 9 PCB trace placement

Trace 3 runs parallel to and close to the device. The trace significantly restricts heat flow (shown by red arrows) because it cuts the copper plane along the device periphery.

Trace 2, which is far from the device, has a lower impact on heat flow.

Trace 1 is the best option, because it is perpendicular to the device. The impact on heat flow is minimal.

Note:

1. *Although Trace 1 is the best routing option, placing multiple instances of Trace 1 in parallel does affect heat flow.*
2. *Avoid routing traces on the thermal layer. If unavoidable, use Trace 1 as an example for routing.*
3. *Maximize the length and/or width of traces to promote heat transfer away from the device.*

4.3 Placement of other components

Similar to traces, placing components close to the QFN device also restricts heat flow. If the other components emit heat, hot spots may be created and the QFN device may no longer be the focus of the thermal design.

In some cases, components must be placed close to the QFN device due to electrical considerations. For example, to optimize the high current loops in a DC-DC converter system, the fly-back diode and inductor must be placed close to the QFN device.

In these cases, one solution is to thermally – but not necessarily electrically – couple the thermal pad of the QFN device to heat sinks used for the other components.

4.4 Additional thermal vias

Thermal vias, similar to the ones used for the thermal landing, can connect internal or external thermal planes, or both, whenever electrically possible. That action helps to maximize the continuous copper plane area for heat conduction. Whenever possible, maximize the overlap between planes, as **Figure 10** shows.

Note: Too many vias can hurt thermal performance because they deplete the continuous plane and may cause mechanical instability.

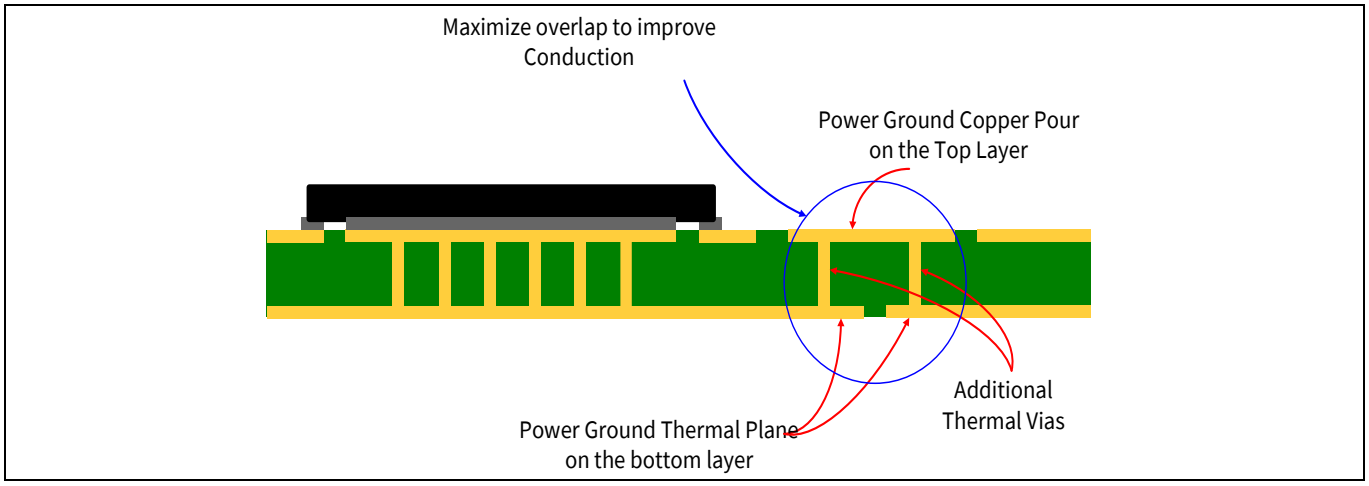


Figure 10 Additional thermal vias

4.5 Use of thermal isolation cuts

Sometimes, you can improve the overall performance of the PCB by carefully placing isolation cuts to segregate components that run at higher temperatures. A component that transfers a lot of heat into the PCB can be isolated so that its heat does not affect other components.

Note: Also consider air flow across the PCB. Place heat-generating components downstream from other components.

4.6 Board considerations

This section lists considerations when designing a board for QFN devices.

Standard glass or epoxy printed circuit boards are compatible with Infineon QFN devices.

4.6.1 Number of PCB layers

Increasing the number of copper layers in a PCB improves thermal conductivity. You can achieve as much as a 20°C reduction in $T_{junction}$ (junction temperature of the device) when you increase the number of layers from two to four. See **Figure 11**.

Recommendation: For systems with total power dissipation (PD) greater than 5 watts, use four layers. If four layers is not an option, explore other cooling techniques.

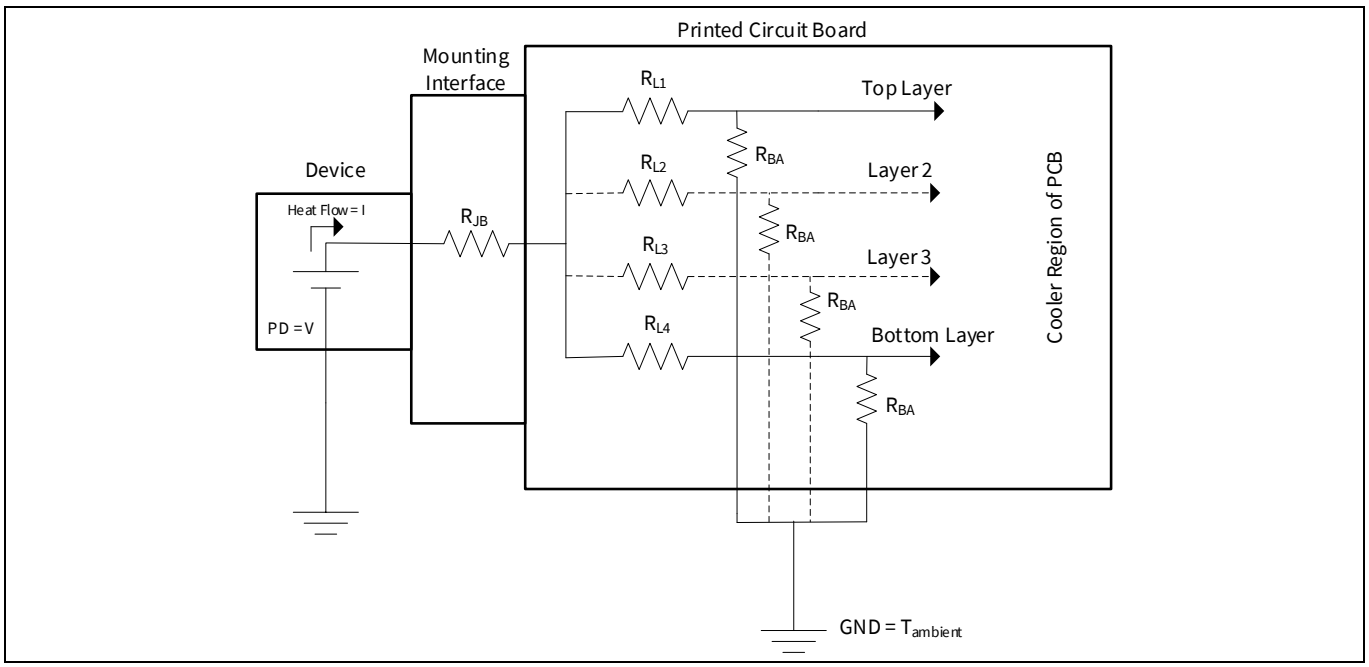


Figure 11 Electrical analogy for a thermal system

4.6.2 Copper thickness

Increasing the copper thickness lowers the thermal resistance. For cost-sensitive designs, increasing the copper thickness In PCB layers may be a good alternative to increasing the number of layers to optimize thermal performance.

Recommendation: Use 2-ounce copper plating for outer layers in designs with total PD greater than 3 W.

4.6.3 PCB size

Large boards have greater thermal mass. Heat travels from the device to the PCB and then laterally conducts through PCB surfaces. We can estimate a first-pass lateral conductivity for a given PCB size by performing some simple calculations based on the following assumptions:

- A 2 inch × 2 inch (50.8 mm × 50.8 mm) board
- Two layers with 100 percent copper coverage
- 2 ounces of copper per layer (layer thickness 0.071 mm)
- Both layers are at the same temperature
- The majority of the heat transfer is in the form of conduction
- Conductivity of copper is 0.386 W/(mm-°C)
- Conductivity of epoxy material is 0.00025 W/(mm-°C)
- Board thickness of 1.52 mm gives epoxy thickness of 1.38 mm
- T_{board} (PCB temperature at a point on the top PCB layer below the QFN component) is 85 °C
- The required $T_{ambient}$ (ambient temperature of the system) is 60°C.

Thermal conduction is along the PCB surface, as **Figure 12** shows.

Using one-dimensional (1D) equations for conduction:

$$\theta_{PCB} = \left(\frac{\ell}{k_{eff} A} \right)$$ Equation 1

Where:

- θ_{PCB} denotes the lumped 1D lateral thermal resistance of the PCB surfaces.
- k_{eff} denotes the effective thermal conductivity of the medium (the PCB in this case).
- “A” denotes the surface area of the medium to the direction of heat transfer. In this case, it is the product of length and PCB thickness.
- ℓ denotes the thickness of the medium.

Assuming heat flow through the PCB as one-dimensional and disregarding heat flow from the side surfaces (shown in **Figure 12**), the effective thermal conductivity, k_{eff}, can be calculated as follows:

$$k_{eff} = \frac{(kt)_{epoxy} + (kt)_{top\_plane} + (kt)_{bottom\_plane}}{t_{PCB}}$$ Equation 2

Where:

- k_{epoxy}, $k_{top\_plane,}$ and k_{bottom_plane} denote thermal conductivity for epoxy and copper planes.
- t_{epoxy}, $t_{top\_plane,}$ and t_{bottom_plane} denote thickness for epoxy and copper planes.
- t_{PCB} denotes overall thickness of the PCB.

Therefore, k_{eff} = 0.036 W/(mm-°C)

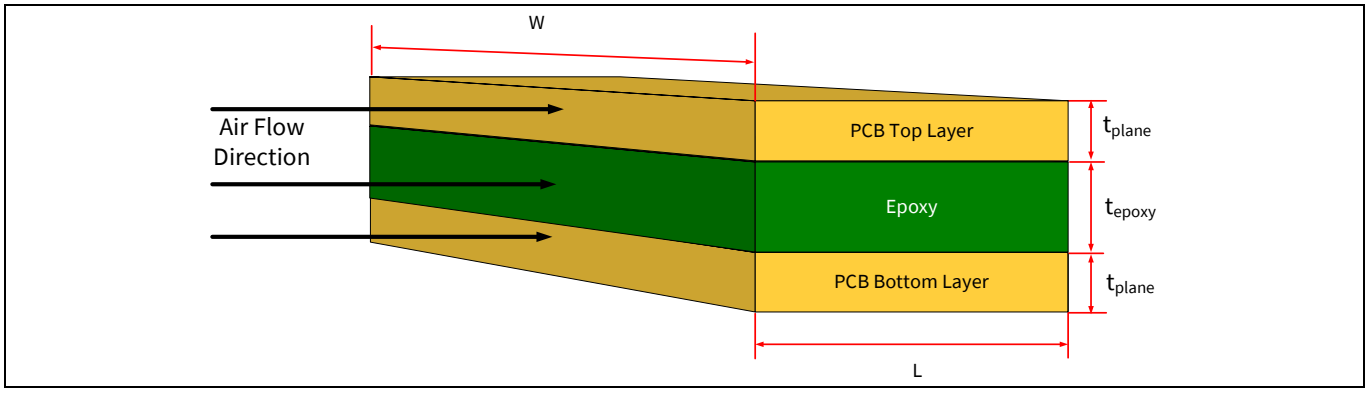


Figure 12 Heat conduction through PCB surface

Now we can calculate θ_{PCB} as follows:

$$\theta_{PCB} = \left(\frac{L}{k_{eff} * t_{PCB} * W} \right)$$ Equation 3

Therefore, θ_{PCB} = 18.30°C/W

Using Equation 4, with a board temperature of 85 °C and ambient temperature of 60 °C, the 2 inch × 2 inch board can dissipate 1.37 W of power:

$$T_{board} = T_{ambient} + PD * (\theta_{BA})$$ Equation 4

Note: Assumptions made in this example are highly simplified. This calculation is used to get a first-pass estimation of conductive cooling that a particular board size can provide for a given temperature increase. You can modify the equations depending on the amount of copper (percentage of copper) for each board layer. If accurate modeling is required (considering the effects of traces and breaks in a continuous plane), then simulate the system's thermal behavior using one of the many available computational fluid dynamics (CFD) thermal analysis tools.

Recommendation: Perform a first-pass PCB thermal estimation in the initial design.

Multiple factors influence FPC material selection and design: Polyimide material and thickness, copper thickness, via and trace dimensions, and stiffener material and thickness (**Figure 13**).

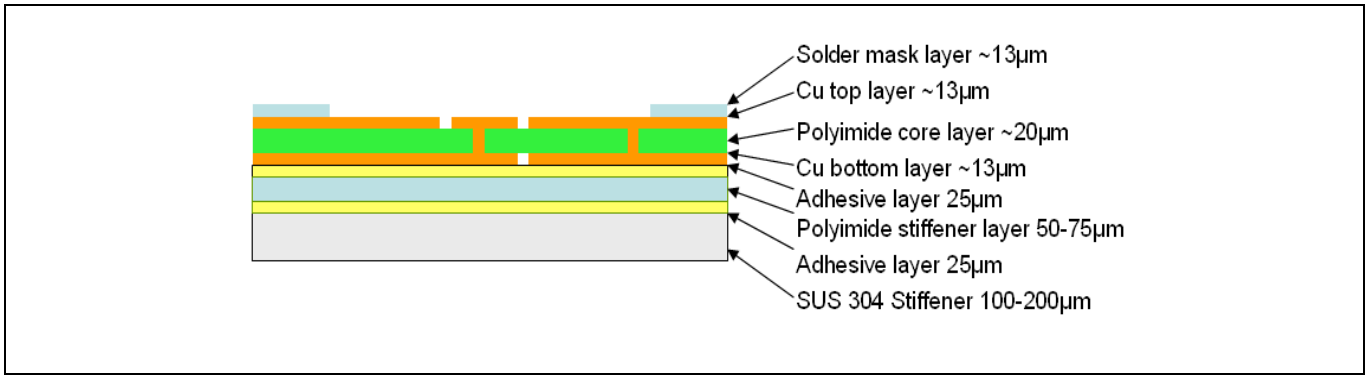


Figure 13 Typical flex printed circuit (FPC) structure

4.6.4 Board geometry and aspect ratio

Generally, board geometries and aspect ratios are governed by system-level and structural constraints. However, uniform geometries and aspect ratios enable effective electrical and thermal layouts, which optimize component placement. For example, a 4 inch × 4 inch square PCB has better thermal performance than a 1 inch × 16 inch PCB with the same surface area, assuming the heat source is at the center of the board.

Recommendation: Use uniform geometries and aspect ratios whenever possible.

4.6.5 Flex printed circuit (FPC) stiffener

SUS304 (stainless steel) is a recommended stiffener to enhance the thermal and mechanical strength of QFN packages in FPC applications. However, you must evaluate the reflow process to determine whether a SUS304 stiffener will hurt solder joint quality due to warpage. When you use a metallic stiffener in capacitive sensing applications, consider the additional parasitic capacitance of the stiffener.

Contact **Infineon support** for FPC layout design rules and review.

5 QFN SMT guidelines

Before component placement, you can start QFN board assembly by screen-printing solder paste on the board. For all QFN applications, it is important to complete the following steps:

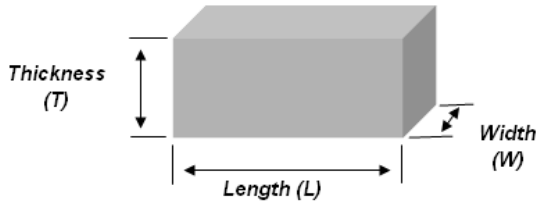
- Stencil design
- Solder paste
- Package placement
- Reflow
- Inspection
- SMT rework

The following sections describe each step.

5.1 Stencil design guidelines

Follow the IPC-7525 stencil design guidelines standard for all assemblies. You must use high-quality stencils to achieve quality solder-paste printing. The thickness of the stencil determines the amount of solder paste deposited onto the PCB land pattern. Because of the fine pitch and small terminal geometries used for QFN packages, take care when printing the solder paste onto the PCB. Too much paste causes solder bridging during reflow, and too little paste results in poor or open connections. You can achieve better solder stencil performance by using laser cut or electroformed stencils, instead of chemically etched stencils.

To prevent unbalanced solder height, the solder stencil openings should be identical for all solder pads in the QFN perimeter. For optimum reliability, the solder joints on the perimeter pads should have a standoff height of about 0.002-0.003 inch (0.051-0.076 mm). To achieve good standoff height for the perimeter pads, start with the stencil design. The stencil aperture opening should be designed to release as much paste as possible. To accomplish that, use the following aspect and area ratios (**Figure 14**).



Aspect Ratio = W/T . . . . . ≥1.5
Area Ratio = LW/2T(L+W) . . . . . ≥0.6

Figure 14 Stencil aperture aspect and area ratio

To remove heat from the package and optimize electrical performance, solder the exposed die paddle to the thermal pad with minimal voids. However, eliminating voids is not always possible because of the presence of thermal vias and the large size of the thermal pad. Reducing the stencil aperture opening to about 50 percent to 80 percent of the total thermal pad area ensures good coverage of the thermal pad area without the risk of bridging to the perimeter pads.

In addition to reducing the aperture size, you can use a slotted thermal pad stencil. That design allows adequate room for outgassing of the paste during reflow, thus minimizing voids.

Figure 15 shows examples of stencils with about 68 percent and 81 percent solder coverage. The stencil area matches the thermal pad area. Take X-rays of a few boards to ensure the manufacturing process results in minimum voids at the interface junction between the thermal pad and the PCB.

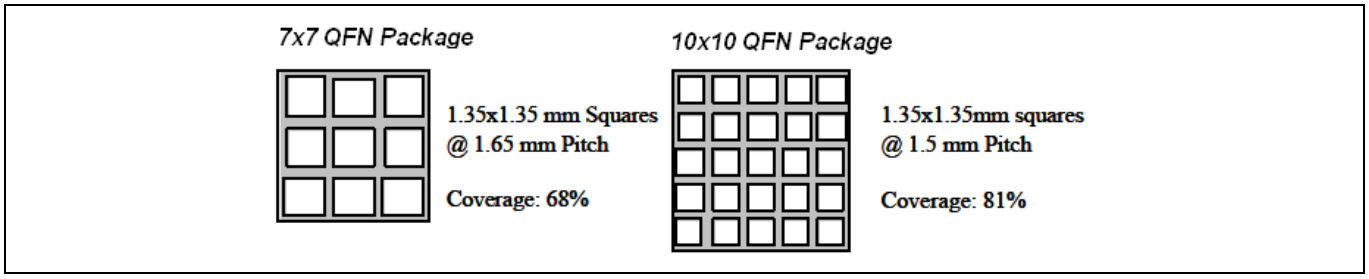


Figure 15 Example of slotted thermal pad stencil design

5.2 Solder paste

The solder paste printing process requires you to transfer solder paste (typical industry standard Pb-free solder paste containing Sn-Ag-Cu) by squeezing it over the stencil. The best board-level reliability is achieved when maximum device standoffs exist under the QFN, which are obtained by using the maximum allowable solder paste volume. Solder paste volume is the best predictor of the finished board quality. Perform a thorough inspection to ensure solder volume uniformity.

Do not use solder paste with active or acid-based flux. Due to the low clearance under a mounted QFN package, the residue from these fluxes is difficult to remove and can degrade the solder joints over time.

When soldering QFN devices for CAPSENSE™ or PSoC™ Multitouch touchscreen applications, the overall cleanliness of the final assembly is critical. Leakage resistance in the megaohm range may distort or otherwise compromise the results of the measurements. For these applications, even no-clean solders may still require a cleaning step to ensure proper operation.

5.3 Package placement

Good process and setup control are strongly recommended for pick-and-place machines used with QFN devices, to avoid damage to the thin structures of the device. Typical surface mount placement equipment can place QFN devices onto PCB or FPC substrates when the equipment is optimized for QFN parts.

To avoid overdriving the device into the solder paste, you should manage the placement height (Z) of the device on the pick-and-place equipment. Optimally, the Z height should be set at one-half the printed solder paste height. Maintaining board flatness (coplanarity) is important in keeping the Z height under control. Thin board technologies, such as FPC, require more caution.

Because of the relatively small size of the QFN package, use a pick-and-place machine with a visions-alignment system for proper centering on the PCB or FPC.

5.4 Reflow

All Infineon QFN-packaged devices are 100 percent Pb-free (Ni-Pd-Au, Ni-Pd-Au/Ag, or pure Sn plate). Therefore, Pb-free solder paste with a Pb-free reflow profile is recommended. If an application requires non–Pb-free solder paste, contact Infineon Customer Support (www.Infineon.com/support) for technical consulting.

When soldering QFN-packaged devices to substrates, remember the following tips:

- The reflow furnace should have nitrogen purge.
- Actual reflow temperatures are determined by the end user, based on thermal loading effect measurements within the furnace, including the complexity of the components on the board and the board size and thickness.
- QFN packages are sensitive to moisture-induced stress. To avoid damage during assembly solder reflow attachment, follow the guidelines in IPC/JEDEC J-STD-020D.1.
- Contact your solder manufacturer for its recommended reflow profile parameters.
- All Infineon QFN devices are qualified at 260 °C reflow with Moisture Sensitivity Level 3. **Figure 16** and **Table 1** show a typical temperature profile for Pb-free (Sn-Ag-Cu or Sn-Ag) solder and the corresponding critical reflow parameters.

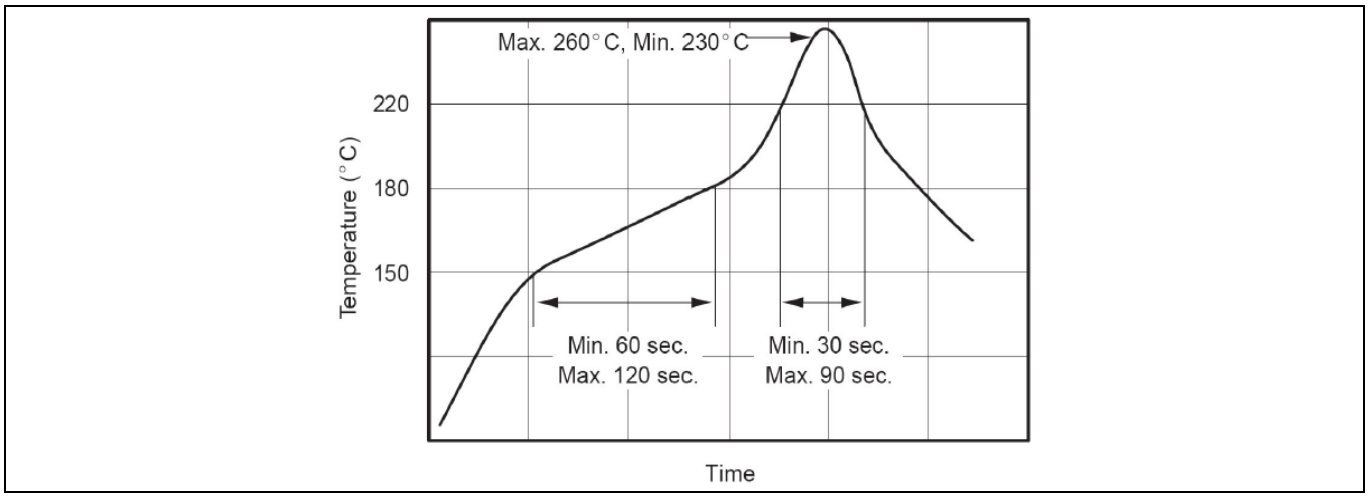


Figure 16 Typical reflow temperature profile for Pb-free paste

- For Pb-free (Sn-Ag-Cu or Sn-Ag) solder, the reflow profile is critical. Sn-Ag-Cu solder melts at ~217 °C. The reflow peak temperature, measured at the solder joint, should be 15 °C to 20 °C higher than the melting temperature.
- Higher reflow temperatures than the Infineon-qualified temperature can cause delamination within the package.

Table 1 Typical reflow parameters for Pb-free paste

Process step	Pb-free paste
Ramp rate	3°C/second
Pre-heat	150°C to 180°C, 60 to 120 seconds
Time above Liquidus, 217°C	30 to 90 seconds
Peak temperature	255°C, ±5°C
Time within 5°C of peak temperature	10 to 20 seconds
Ramp down rate	6°C/second (max)

5.5 Inspection

Because the plating of the lead frame is done prior to package singulation, the exposed sides of the leads are not plated and have a bare copper surface. Because copper oxidizes readily in an uncontrolled environment, the package falls into the category of “Bottom Only Termination,” according to IPC/EIA J-STD-001C. Due to factors beyond our control, Infineon does not guarantee the fillet formation on the sides of the package during board assembly.

Optical inspection should be performed in accordance with IPC-A-610. **Figure 17** and **Figure 18** show solder fillet formation from an optimized surface mount process for standard lead design (non pull-back design) QFN packages.

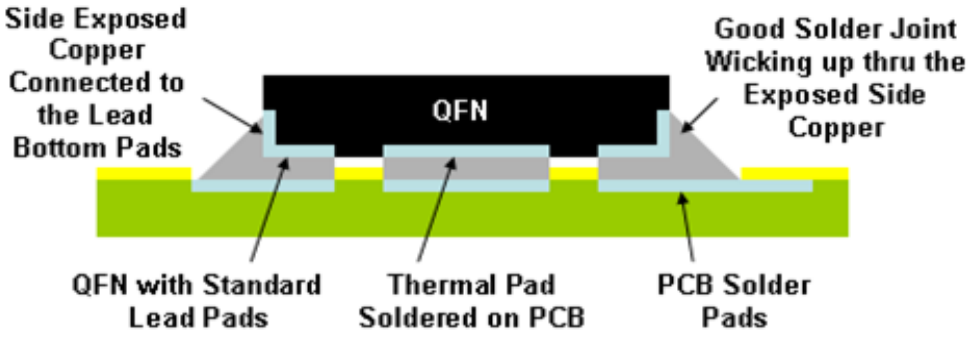


Figure 17 Cross-section view of solder joint on standard QFN without pull-back sesign (optimal solder joint)

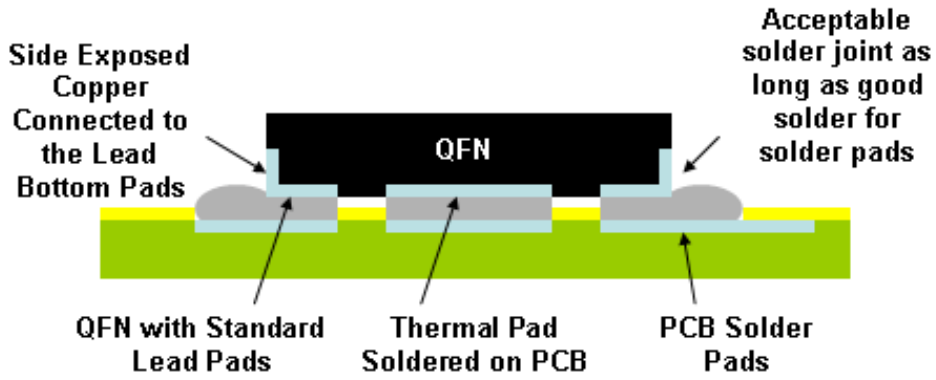


Figure 18 Cross-section view of solder joint on standard QFN without pull-back design (acceptable solder joint)

QFN packages with a pull-back design are soldered to the PCB through the QFN leads on the bottom of the package. These leads connect only to the PCB solder/land pads under the QFN body; for this reason, the solder joints cannot be inspected optically. Use X-ray inspection to confirm the quality of solder joints under mounted QFN packages. **Figure 19** shows the expected solder joint formation from an optimized surface mount process for pull-back design QFN packages.

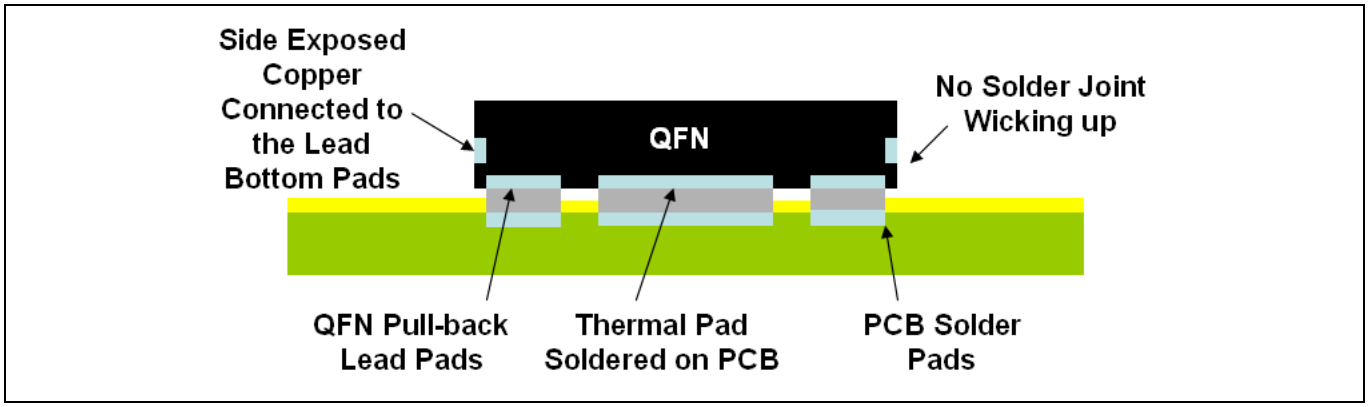


Figure 19 Cross-section view of solder joint on the QFN with pull-back design

5.6 SMT rework

Use a controlled and qualified process when you rework QFN devices to avoid mechanical and ESD damage to the device.

Prior to attempting any rework, you must ensure that the assembly is free of moisture, which could damage the board or other components. Under-board preheating is required at 150 °C to 200 °C for Pb-free solder. If you intend to reuse the device, perform a dry bake (125 °C for a minimum of 24 hours) to remove any moisture that the package may have absorbed.

To remove QFN-packaged devices for rework, focused infrared technology is preferred over traditional hot-gas. Focused IR allows more accurate removal and replacement of QFN devices without heating the adjacent components on a PCB or FPC.

If the component must be reused, a three-stage (ramp up, hold, ramp down) reflow profile is required to remove the component. Otherwise, you can use a direct ramp-up for faster device removal. The peak temperature should be in the range of 240 °C – 250 °C for as long as 90 seconds for Pb-free solder.

The temperature delta across the QFN solder joints should be less than 10 °C. The board temperature around the perimeter of the component undergoing rework should be less than 150 °C. The component top temperature should be less than 260 °C for Pb-free devices. Flux is not recommended for device removal because it adds a process step and cost.

Air velocity should be as low as possible to avoid component skew (for example, 500 cubic feet per hour (CFH) for top heater, 100 CFH for bottom heater). A nitrogen atmosphere is recommended for better heat distribution and to limit oxidation of the solder pad surfaces. A zero-force vacuum pick-up is required during the transition to cool down to avoid bridging of reflowed solder.

5.7 Component replacement

Clean the rework site with a solvent before component replacement to remove any surface contamination. For solder paste/flux application, use a mini-stencil with a squeegee as wide as the stencil. Align the apertures with the solder pads under 50x to 100x magnification. The placement machine should allow fine adjustment in the X, Y, and rotation axes.

Follow the paste manufacturer’s recommendation for reflow profile, and make sure that the maximum temperature does not exceed the package qualification level. Reflow profiles developed for initial placement or rework also can be used. A three-stage (ramp up, hold, ramp down) profile may result in smaller temperature distribution across the site.

6 Infineon QFN reliability test data

6.1 Component level reliability test

Infineon qualification procedures and requirements comply with various industry standards including JEDEC/IPC and MIL-STD-883.

Stress tests for component-level reliability are listed in **Table 2**.

Table 2 QFN qualification stress tests

Test method	Test conditions	MSL	Duration
Temp cycles cond C	-65°C to +150°C	MSL 3	500 cycles
HAST	130°C / 85% RH	MSL 3	128 hours
Pressure cook test	121°C /100% RH	MSL 3	168 hours
High temperature storage	150°C	NA	1000 hours

Detailed qualification reports for specific Infineon QFN products are available at **www.Infineon.com**.

6.2 Board-level reliability test

Board-level reliability of QFN devices can be heavily affected by the board's material, design parameters, and thickness.

Typically, QFN-packaged devices are highly reliable when assembled on rigid PCBs when the bottom thermal pad of the QFN package is soldered to the board. When the thermal pad is soldered onto the PCB, the life of the solder joint is extended by 60 percent. For this reason, soldering the thermal pad onto the board is crucial to the reliability of the solder joints on PCBs.

Because chip-on-lead (COL) QFN products (see **Figure 22**) do not have a bottom thermal pad, they perform worse on board-level reliability tests. A non-conductive epoxy coating around the solder joints on the board enhances mechanical strength.

The volume of solder paste dispensed when mounting a QFN package onto a PCB is critical for the proper package standoff height and for acceptable fillets on the perimeter of the QFN package. This improves board-level reliability.

The reliability of QFN products on FPC is not well known in the industry. However, optimizing the FPC structure and SMT process results in sufficient performance to meet requirements for typical handheld products. Use a SUS304 stainless steel stiffener to improve mechanical strength of QFN products mounted on an FPC.

Contact your local Infineon sales representative for more detailed information.

6.3 Package thermal resistance

Infineon lists the thermal resistance of each QFN product in the associated device datasheet.

Typical simulation conditions for thermal resistance require you to mount the device to either a two-layer or four-layer PCB, depending on the application of the product.

Θ_{JA} (Theta Ja, thermal resistance of junction-to-ambient) specifies the thermal resistance between a die in its package and the ambient air surrounding the packaged part when mounted to a PCB or FPC, according to JEDEC EIA/JESD51-2.

7 QFN handling during packing, shipping, and SMT

Infineon recommends that QFN-packaged programmable devices be ordered preprogrammed by Infineon to remove off-board programming from the product manufacturing flow. Alternatively, use on-board programming to prevent damage to the devices in programmer sockets during mechanical handling.

If you require reprogramming or electrical test of QFN-packaged devices, take special care during loading of the devices into the test/programming socket(s) from tape-and-reel. Infineon recommends using automated pick-and-place machines to prevent damage during mechanical handling that may affect functionality and reliability.

The moisture sensitivity level (MSL) of a component indicates its floor life and storage conditions after the original container has been opened. All Infineon QFN products are classified as MSL3 and support a 260°C reflow peak temperature, according to JEDEC standard J-STD-020.

8 Appendix A - Infineon QFN construction

Figure 20 shows a QFN package mounted on a PCB with its exposed center pad soldered to the PCB.

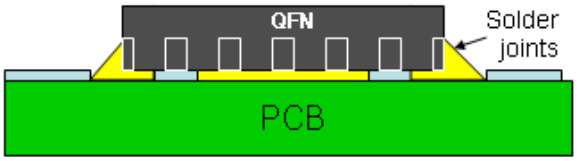


Figure 20 QFN package mounted on a PCB

Figure 21 and **Figure 22** show more details of QFN internal construction with silicon chips.

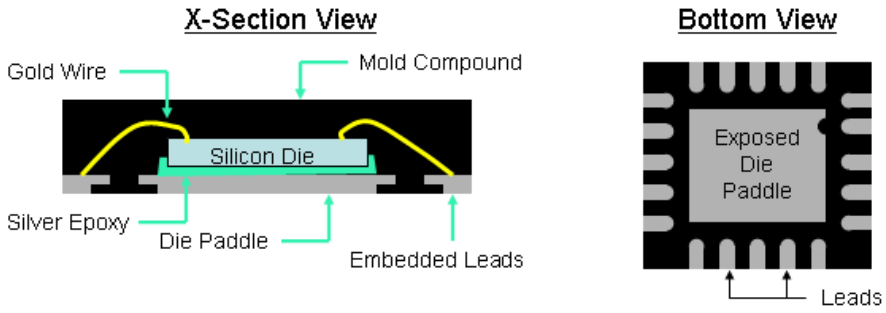


Figure 21 Standard saw-singulated QFN with exposed die paddle

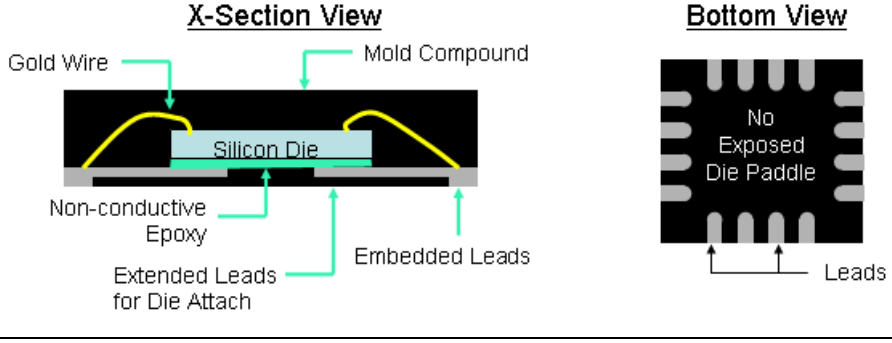


Figure 22 Chip on leads (COL) QFN without exposed die paddle

Infineon's QFN packages use a copper lead frame plated with either nickel-palladium-gold (Ni-Pd-Au), nickel-palladium-gold/silver (Ni-Pd-Au/Ag), or pure tin (Sn).

References

[1] **AN61290 - PSoC™ 3 and PSoC™ 5LP hardware design considerations**

[2] **AN88619 - PSoC™ 4 MCU hardware design considerations**

[3] Application Note: *Board Level Assembly and Reliability Considerations for QFN Type Packages* – Amkor Technology, September 2008 **http://www.amkor.com/go/packaging/all-packages/microleadframeandreg**

[4] Chapter 17: Printed Circuits Handbook (McGraw Hill Handbooks) – Sixth Edition, Darwin Edwards, Clyde F. Coombs, Jr., 2008

Revision history

Document version	Date of release	Description of changes
**	2011-12-12	New application note
*A	2015-01-29	Added note to see device datasheet for information on leaded packages Replaced reference to obsolete AN53741 with references to AN61290 and AN88619 Moved QFN construction section to Appendix A. Reformatting and minor edits throughout Updated template Sunset review
*B	2017-04-19	Updated logo and copyright
*C	2022-08-29	Migrated to Infineon template

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