

# AN72382

# Using PSoC<sup>®</sup> 3 and PSoC 5LP GPIO Pins

Author: Greg Reynolds Associated Part Family: All PSoC<sup>®</sup> 3 and PSoC 5LP parts Software Version: PSoC Creator™ 2.1 SP1 and higher Related Application Notes: For a complete list of related application notes, click here.

AN72382 shows you how to use GPIO pins effectively in PSoC® 3 and PSoC 5LP. Major topics include GPIO basics, configuration, mixed-signal use, registers, interrupts, and low-power behavior.

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#### 1 Introduction

The any-signal-to-any-pin routing available with PSoC® 3 and PSoC 5LP GPIOs helps to optimize PCB layout, shorten design time, and allow a large degree of solderless rework. However, with this freedom comes a steeper learning curve than with a traditional microcontroller. This application note introduces you to PSoC 3 and PSoC 5LP GPIO basics and demonstrates techniques for their effective use in a design.

It is assumed that you are familiar with PSoC Creator™ and the PSoC 3 and PSoC 5LP family device architecture. If you are new to PSoC, see the introductions in AN54181 - Getting Started with PSoC 3 and AN77759 - Getting Started with PSoC 5LP. If you are new to PSoC Creator, see the PSoC Creator home page.

For a list of related PSoC design resources, see the Related Application Notes section.



# 2 GPIO Pin Basics

In PSoC 3 and PSoC 5LP devices, the GPIO, SIO, and USB pins are similar. Unlike GPIO pins, though, the SIO and USB pins have different drive strengths and application-specific features. Some GPIO pins also have secondary dedicated functions, such as opamp inputs and outputs, programming and debugging interfaces, or DAC outputs. When they are not being used for special functions, all GPIO pins behave the same. Depending on the package type, PSoC devices can have as many as 62 GPIO pins.

## 2.1 Physical Structure of GPIO Pins

GPIO pins have eight drive modes to support the many analog and digital I/O capabilities that PSoC offers. A detailed block diagram of the GPIO structure appears in the PSoC 3 Architecture Technical Reference Manual (TRM), as well as in the PSoC 3 and PSoC 5LP family datasheets. Figure 1 shows a simplified version.





The various drive modes and their custom settings are described in detail in the Pins Component datasheet, which is available as part of PSoC Creator or as a separate download from the Cypress website.

## 2.2 Digital System Interconnect Overview

The PSoC 3 and PSoC 5LP digital subsystem has a programmable interconnect that allows connections between the built-in peripherals, custom logic functions (universal digital blocks, or UDBs), and any I/O pin. The digital system interconnect (DSI) routing interface allows GPIO pins to connect to any digital resource in the chip, as Figure 2 illustrates.



Figure 2. DSI Block Diagram



All digital resources are routed to the DSI for connection to each other or to the system core. For more details about the DSI operation, see the "UDB Array and Digital System Interconnect" section of the TRM.

## 2.3 Analog Routing Overview

The GPIO pins are connected to analog resources, or to each other, through a series of analog routing buses joined by switches and muxes. The two primary analog routing buses are the analog global (AG) bus and the analog mux (AMUX) bus. The AG bus is divided into four quadrants (AGL0-4, AGL4-7, AGR0-4, and AGR4-7), and the AMUX bus is divided into two halves (AMUXL and AMUXR). Figure 3 shows a portion of the analog routing diagram from the TRM.





Each AGx can connect to two of the pins on an associated port in each quadrant, while each AMUX can connect to every pin on its half of the chip. The analog buses also connect to the inputs and/or outputs of various analog resources, such as comparators, DACs, and ADCs. In addition, switches allow the left and right buses to be connected to each other.

An in-depth description of the analog routing system in the PSoC 3 and PSoC 5LP devices is included in the "Analog Routing" section of the TRM. Application notes AN58304 and AN58827 discuss analog routing and pin selection in detail.

## 2.4 GPIO Power Structure and Limits

In general, GPIO pins can source 4 mA and sink 8 mA. They can be ganged together (shorted) to allow more current to be sourced or sunk than that which a single pin can provide, but you need to consider additional power limitations.

PSoC 3 and PSoC 5LP devices provide as many as four individual I/O voltage domains through the  $V_{DDIO}$  pins. In the PSoC 3 and PSoC 5LP datasheets, the  $V_{DDIO}$  pin that supplies power to a particular set of pins is indicated by solid lines drawn on the pinout diagrams. Figure 4 shows a 48-pin PSoC 3 device with the  $V_{DDIO}$  quadrant indicators highlighted in red.





Figure 4. Example V<sub>DDIO</sub> Quadrants Highlighted in Red

The VDDIO pins are often tied to the same power rail as VDD. Little thought is given to how much current any individual VDDIO quadrant is sourcing and sinking, but there are limitations. Table 1 shows the limits according to PSoC family and package type.

Table 1.	V <sub>DDIO</sub>	Quadrant	Current	Limits
----------	-------------------	----------	---------	--------

Family	Package	Source	Sink		
PSoC 3	100-pin 68-pin	100 mA per V <sub>DDIO</sub>	100 mA per V <sub>DDIO</sub>		
PSoC 5LP	48-pin	100 mA V <sub>DDI00</sub> +V <sub>DDI02</sub> 100 mA V <sub>DDI01</sub> +V <sub>DDI03</sub>	100 mA $V_{DDIO0}$ + $V_{DDIO2}$ 100 mA $V_{DDIO1}$ + $V_{DDIO3}$		
	100-pin 68-pin	20 mA per $V_{DDIO}$	20 mA per $V_{DDIO}$		
PSoC 5	48-pin	20 mA V <sub>DDI00</sub> +V <sub>DDI02</sub> 20 mA V <sub>DDI01</sub> +V <sub>DDI03</sub>	20 mA V <sub>DDI00</sub> +V <sub>DDI02</sub> 20 mA V <sub>DDI01</sub> +V <sub>DDI03</sub>		
Note: Total source+sink current should not exceed 100 mA for any V <sub>DDIO</sub> quadrant (or V <sub>DDIO</sub> pair for the 48-pin packages).					

In applications for which the typical current sourced and sunk by the GPIO pins is expected to exceed 80 percent of the limit, make sure that no single quadrant of GPIO pins exceeds its maximum under the worst operating conditions. Doing so may mean that the design needs to use pins in separate VDDIO quadrants to spread out the current.

## 2.5 Relative Voltages of V<sub>DDA</sub>, V<sub>DDD</sub>, and V<sub>DDIO</sub>

 $V_{DDA}$  must be at the highest voltage present on the PSoC 3 or PSoC 5LP device. All other power supply pins must be less than or equal to  $V_{DDA}$ . The  $V_{DDD}$  and  $V_{DDIO}$  pins may be less than, greater than, or equal to each other.

The **System** tab of the Design-Wide Resources file includes a voltage configuration section that lets you define the voltage at which each power domain will operate. The values entered in these fields, shown in Figure 5, are used by PSoC Creator if a Component or feature is dependent on the voltage at which it is running.



> Reset   ਸਿ∓ Expand   → Collapse							
Option Type		Value					
	🗄 - Configuration						
⊕ Programming\	.Debuggir	Ig					
- Voltage Configuration							
- Vddd	FLOAT	5.0					
- Vdda	FLOAT	5.0					
- Vddio0	FLOAT	5.0					
- Vddio1	FLOAT	2.7					
Vddio2	FLOAT	1.8					
Vddio3 FLOAT 3.3							
Input value indicates the input voltage on Vddio3 pin.							
terrupts 🖁 DN	1A 📝	System 🔛 Directiv 4 🕨					

Figure 5. Voltage Configuration in Design-Wide Resources

Proper voltage configuration in PSoC Creator is recommended in all cases, regardless of which Components or features are used.

## 2.6 Startup and Low-Power Behavior

Out of the box, all GPIO pins start up in an Analog HI-Z state, where they remain until reset is released. The initial operating configuration of each pin is loaded during boot and takes effect at that time. You can change the reset behavior of GPIOs using the PRTxRDM fields of the nonvolatile latch array, which are written when the PSoC device is programmed.

In all low-power modes, GPIO pins retain their state until the part is reset or awakened. The port interrupt logic continues to function in all low-power modes so that pins can be used as wakeup sources.

**Note** UDB-based Components, such as control registers, are typically not active during sleep or hibernate. They can glitch when the PSoC device enters or exits these modes. The glitch could cause a GPIO to be set at an unwanted state. To avoid that, set the pins explicitly to a HIGH or LOW logic state before the PSoC device enters a low-power mode.

## 2.7 DMA Access to GPIO Pins

PSoC devices have a DMA controller that connects to different internal peripherals, including the I/O interface. Because GPIO registers are memory-addressed, DMA transfers can be used to configure GPIO pins and write data to the digital output path without requiring any action by the CPU.

DMA configuration and data transfer are too complex to be covered in this application note. Several other application notes and code examples are available, including AN52705 – PSoC 3 and PSoC 5LP – Getting Started with DMA.

## 2.8 Port Interrupt Control Unit

PSoC 3 and PSoC 5LP have a port interrupt control unit (PICU) that manages I/O interrupts. Each GPIO pin can generate an interrupt on a rising edge, falling edge, or either edge condition. Level-sensitive interrupts are implemented by tying a cy\_isr Component to the interrupt terminal of a Pins Component.

When a GPIO interrupt is triggered, the corresponding bit in that GPIO's status register is set to '1'. The bit will remain at '1' until the register is read or a chip reset occurs. The API provided by PSoC Creator manages GPIO interrupt configuration and reporting.

The individual GPIO interrupt signals within a port are ORed together, and a single PICU request is sent to the interrupt controller. The port interrupt requests are daisy-chained together to generate a single wakeup signal, which is sent to the PSoC power manager. The PICU remains active in all low-power modes, but the individual GPIO interrupts must still be managed after wakeup.





# 3 GPIO Pins in PSoC Creator

This section describes how to use PSoC Creator to configure and manipulate GPIO pins. PSoC Creator combines text and graphical editing interfaces so that designers can set their hardware configuration and write firmware at the same time.

## 3.1 **PSoC Creator APIs**

Cypress provides a set of APIs that you can use to dynamically control GPIOs through firmware. The APIs for the Pins Component enable access on both a component-wide and per-pin basis.

The cy\_boot Component also provides functions to access chip resources. The functions in cy\_boot are not part of the individual component libraries, but the libraries can use them. The per-pin APIs, which are provided as part of cy\_boot in the *cypins.h* file, are documented in the "Pins" section of the PSoC Creator System Reference Guide. You can use these APIs to control the configuration registers for each physical pin.

For a summary and a simple code example for the APIs related to GPIOs, see GPIO API and Register Reference.

## 3.2 Pins Component Symbols and Macros

The cy\_pins Component is the recommended way for internal PSoC resources to connect to a physical pin. It allows PSoC Creator to automatically place and route the signals within the PSoC device based on the chosen configuration of the pin. The standard Cypress component catalog contains four types of predefined GPIO configurations (macros) in the Ports and Pins class of symbols: analog, digital bidirectional, digital input, and digital output. Drag one of these component macros to the schematic to add a pin to the project, as Figure 6 shows.



Figure 6. Pins Component Symbol Types in PSoC Creator

You are not confined to one type of pin configuration based on which macro symbol you choose. After you place the pin symbol on the schematic, you can configure its behavior using the component customizer options described in this document.

## 3.3 Pins Component Interrupts

You can enable interrupts in Pins Components with the cy\_pins configuration dialog in PSoC Creator, as Figure 7 shows. Double-click on the Pins Component to open it.



Configure 'cy_pins'		? 💌
Name: Interrupt		
Pins Mapping Bui	lt-in	4 Þ
Number of Pins: 1	★ 🗣 🔹 🕅 💥	
[All Pins] └──⊠ Interrupt_0	Type General Input Output Threshold: CMOS   Hysteresis Interrupt: Rising Edge Rising Edge Faling Edge Both Edges W #put Synceromized	
Datasheet	ОК Арріу С	ancel

Figure 7. Interrupt Configuration in PSoC Creator

The Pins Component symbol changes when interrupts are enabled, as Figure 8 shows. The IRQ signal of the Pins Component will toggle when a pin interrupt is triggered. You do not need to connect the irq terminal to an isr Component to enable a pin interrupt.

Figure 8. Pins Component Symbol Changes with Interrupts Enabled

ļ		Ň	í A		nterrunt	4[0]		ł	ł		
			Υ.	- 1	incertupt		I.,				
				Ξī.	ntorrunt						
				1	ntenupt						
÷					Dinc				÷		
					FIIIS						
					5[0]	_					
					•						
					irq 🗆 🗤 🗤						
											1

If interrupts are enabled, you can use only one Pins Component with each physical GPIO port. The reason for this limitation is that all pin interrupts in a port are ORed together, so only one IRQ signal can be shown on the schematic.

For example, consider two Pins Components with interrupts enabled, as Figure 9 shows. These Components cannot be mapped to pins in the same physical port because there are now two separate IRQ signals in the PSoC Creator schematic, but there is really only one physical PICU interrupt generated for the entire port.

Figure 9. Two Pins Components with Interrupts.



PSoC Creator will give an error if you try to assign these two Components to the same port. The accepted method is to assign multiple pins to the same Component, as Figure 10 shows. This ensures that there is only one IRQ signal in the schematic for that physical port. You can still assign each pin its own interrupt edge type. The only limitation is that the pins must be contiguous.



Figure 10. Pin Selection with Different Interrupt Edge Types.



You can also use the PICUx\_INTTYPEy registers to enable or change interrupts on any GPIO pin, regardless of Component settings. See the appendixes for more information on these registers.

## 3.4 External Terminals

The cy\_pins configuration dialog offers an option to show an external terminal. This allows you to add Off-Chip Components to your schematic and show their connections to the Pin. Figure 11 shows an example of a Pins Component driving an off-chip LED.

Figure 11. Off-Chip Component Connection Example



## 3.5 Manual Pin Assignments

A Pins Component is assigned to a physical pin through the **Pins** tab of the Design-Wide Resources interface (*cydwr*). PSoC Creator automatically assigns pins if none are chosen by the user, but this may lead to pin placement that is more difficult to route on a PCB. Also, some GPIO pins are directly connected to analog or digital resources.

Figure 12 shows three assigned pins. The pins highlighted in gray were manually assigned, and the pin highlighted in yellow was automatically assigned. Selecting the **Lock** option prevents the pin from being reassigned by PSoC Creator.



Figure 12. Pin Assignment in cydwr Window

PSoC Creator makes it simple to reassign pins as needed, but designers should consider pin selection before boards are designed. The "Analog Interconnect" diagrams in the TRM, AN58304, and AN58827 are valuable resources to help determine the optimal analog pin selection.



# 4 GPIO Examples, Tips, and Tricks

This section provides practical examples of how to use GPIO pins. The examples were generated for PSoC 3 devices, but the same techniques apply to PSoC 5LP. Both basic examples and more advanced techniques are included.

## 4.1 The GPIO "Hello World" Project

The simplest use of a GPIO is to set the output state of a pin HIGH or LOW. This example demonstrates how to set the output using the Pins Component API.

- 1. Place a Digital Output Pins Component, configured to Strong drive mode, in the project schematic, as Figure 13 shows.
- 2. Name the Component "MyPin" and assign it to P6[2].

Figure 13. Hello World Example Schematic



3. In *main.c*, use the Component API to toggle the output, as follows:

```
for(;;)
{
    /* Set MyPin output state to HIGH */
    MyPin_Write(1);
    /* Delay for 500 ms */
    CyDelay(500);
    /* Set MyPin output state to LOW */
    MyPin_Write(0);
    /* Delay for 500 ms */
    CyDelay(500);
}
```

4. Build the project and program the PSoC device.

The result is an output that toggles high/low every 500 ms.

## 4.2 Read an Input and Write to an Output

This example demonstrates how to read and write to a GPIO pin with the Component APIs. The output pin will drive the inverse of the input pin state.

1. Place two pins in the project schematic—one digital input pin and one digital output pin—as Figure 14 shows.

Figure 14. Input and Output Example Schematic



2. Use the Component APIs to set the state of OutputPin based on InputPin as follows:

```
for(;;)
{
    /* Set OutputPin state to the
    inverse of the InputPin state */
```



```
OutputPin_Write( ~InputPin_Read() );
}
```

The result is that OutputPin is always at the opposite state of InputPin.

## 4.3 Add Multiple GPIO Pins as a Logical Port

In PSoC Creator, you can organize a group of as many as 64 pins into a logical port, which can then be referenced in code by the port's defined name. All the pins may be part of the same physical port, or they may be from separate physical ports.

1. Place a single pin symbol, as Figure 15 shows.

Figure 15. Single Pin Symbol Placed in a Schematic



- 2. Double-click on the pin symbol to open the pin customizer window.
- 3. Type the number of pins in the **Number of Pins** field in the configuration window.

The pins will appear in the list below the field. Select an individual pin in the list to allow it to be customized independently of the others. Select **[All Pins]** to affect every pin in the port.

4. For this example, set three of the pins as digital output pins. Set the last as a digital input, as shown in Figure 16.

Figure 16. One of Four Pins Configured as a Digital Input

Configure 'cy_pins'			? X
Configure 'cy_pins'          Name:       MyPins         Pins       Mapping         Re       Number of Pins: 4         [All Pins]       MyPins_0         MyPins_1       MyPins_2         MyPins_3       MyPins_3	set Built-in X Ø ♠ ♥ 8 × 1 Type General Inp Analog Ø Digital Input Ø HW Connection Digital Output Ø HW Connection Output Enable Bidirectional	ut Output Preview:	
Data Sheet	ок	Apply	Cancel

5. Click **OK** to apply the changes.

After you define the number of pins and their types, the schematic symbol will resemble Figure 17.

Figure 17. Pins Component in Port Configuration



6. (Optional) Select **Display as Bus** in the **Mapping** tab of the pin configuration window to display the port as a bus symbol, as Figure 18 and Figure 19 show.



Figure 18. Display as Bus Option

Configure 'o	y_pins'	?	X
Name:	MyPins		
Pins	Mapping Reset Built-in	٩	Þ
Display	/ as Bus		1
Selects The bu compo all eithe	whether to display individual terminals for each pin or a single wide terminal (by s options is only valid when pins are homogeneous, which means that all pins i nent have the same pin type, output/input HW connections, SIO grouping, and r use or don't use the SIO Vref.	us). n the .d they	
Contig	uous		
Forces Port-lev APIs w	placement in adjacent physical pins. rel APIs will only be generated for this instance if it is set to be Contiguous. Per ill be globally available either way.	pin	
✓ Spann	ing		
Allows Note: S case in	placement in multiple physical ports. panning is currently configured based on the Contiguous setting. This will not I the future.	be the	
Data :	Sheet OK Apply Ca	ncel	

This feature does not affect the behavior of the port. **Note** All pins must be of the same type for them to be displayed as a bus.

Figure 19. Four Pins Displayed as a Port Bus Symbol



7. (Optional) Select **Contiguous** in the **Mapping** tab to force the pins to be physically adjacent, as Figure 20 shows.

Figure 20. Contiguous Pin Placement Option

onfigure 'c	y_pins'	X
Name:	MyPins	
Pins	Mapping Reset Built-in	4 ۵
Display	r as Bus	-
Selects The bu compor all eithe	whether to display individual terminals for each pin or a single wide terminal (bus), s options is only valid when pins are homogeneous, which means that all pins in the rent have the same pin type, output/input HW connections, SIO grouping, and the r use or don't use the SIO Vref.	e ey
Contigu	SUOL	=
Forces Port-lev APIs wi	placement in adjacent physical pins. rel APIs will only be generated for this instance if it is set to be Contiguous. Per-pin II be globally available either way.	
Spanni	ng	
Allows   Note: S case in	placement in multiple physical ports. panning is currently configured based on the Contiguous setting. This will not be th the future.	e
Data S	iheet OK Apply Cancel	

When you select **Contiguous**, PSoC Creator will modify the list of available pinout options to match the port's configuration, as Figure 21 shows.



Figure 21. Pin Placement of Contiguous Port Pins



These features are described in more detail in the pin configuration window and the Pins Component datasheet.

## 4.4 Configure GPIO Output Enable Logic

This example demonstrates how to configure and use the output enable logic of a GPIO pin.

- 1. Place two digital output pins in the project schematic.
- 2. Open the configuration dialog for each pin and check the **Output Enable** box, as Figure 22 shows.

Configure 'cy_pins'	Output2		? <mark>X</mark>
Name: Output1			
Pins Mapping Re	eset Built-in		4 ۵
Number of Pins: 1	X 🗗 🕈 🕈 🕅	8	
[All Pins]	Type General	Input Output	
····· Output1_0	Analog	Preview:	
	Digital Input     HW Connection     Digital Output     HW Connection     Output Enable     Bidirectional		
Data Sheet	ок	Apply Car	ncel

Figure 22. Output Enable Selection

- 3. Place a control register in the schematic.
- 4. Configure the control register for two outputs, as Figure 23 shows.



Figure 23.	<b>Control Register</b>	Configured with	Two	Outputs
------------	-------------------------	-----------------	-----	---------

Configure '	CyControlReg'	MuC	Wher Si	Inmail	? X
Name:	ControlReg				
Con	ifigure Built-i	n			4 ۵
	Outputs 2 Set All Direc ModeMask/ Bit Bit0Mode Bit1Mode	tMode BtValue Mode DirectMode DirectMode	External Res Clear All Bit Value Bit Value 0 0 0 0	et ]	
Data	Sheet		ок	Apply	Cancel

- 5. Add two Clock Components, configured in any way.
- 6. Connect the clocks to the pins, as Figure 24 shows.

Figure 24. Control Register Driving Pins' Output Enable



7. Add the following code to the *main.c* file:

```
for(;;)
{
    for( i=0; i<=3; i++ )
    {
        ControlReg_Write(i);
        CyDelay(500);
    }
}</pre>
```

8. Compile and program the PSoC 3 or PSoC 5LP device.

The result is the output of the two pins gated by the state of ControlReg.

This same method can be used for the creation of a bi-directional data bus. Place as many pins as required for the data bus and check the **Output Enable** box in each Pin Component. Connect all the output enable signals to a single Control Register output. When Output Enable is enabled the GPIO pins are strongly driven out. When the Output Enable is disabled the GPIO pin input logic state can be read.

## 4.5 Enable the Configurable XRES Feature

This example demonstrates how to enable the configurable XRES feature. You can configure Pin P1[2] as an optional XRES pin to support an external reset for small packages. The feature is also available in the larger packages.

1. Open the System tab in the Design-Wide Resources file, as shown in Figure 25.



2. Select the **Use Optional XRES** option to enable the optional XRES logic. If this box is selected, P1[2] stops functioning as a GPIO pin and is configured as an active LOW input with an internal pull-up.

-						
Programming\Debugging						
Debug Port Select (DPS) ENUM Debug ports disabled						
Enable BOOL						
Require XRES Pin	BOOL					
Use Optional XRES BOOL						
⊡ Voltage Configuration						
f enabled, a GPIO will be configured	to be an	external reset (XRES) pin				

Figure 25. Optional XRES Pin Enable

- 3. Program the PSoC device to write the setting to the nonvolatile array. It will take effect after the next power on.
- 4. Deselect the Use Optional XRES option and reprogram the PSoC device to restore normal GPIO functionality.

Note that all PSoC 3 and PSoC 5LP devices come from the factory with the optional XRES feature disabled. Using the configurable XRES pin does not change the functionality of a dedicated XRES pin.

## 4.6 Disable Debug Logic on GPIO Pins

This example demonstrates how to disable the debug logic associated with the port 1 pins. If the debug port feature is enabled, the PSoC device will enter debug mode if it detects activity on these pins at boot time.

- 1. Open the Design-Wide Resources file and click the **System** tab.
- 2. Select **Debug ports disabled** from the drop-down menu, as Figure 26 shows.

			arcrage roppesignicysci ina	inc d						
	_	_	Seset   È⊕ Expand   È Collapse							
Pro	-	$\leq$	Option	Туре	Value					
4. To		ş	En Configuration							
		Irce								
		8	- Debug Port Select (DPS)	ENUM	Debug ports disabled 🛛 🔻					
	H	mpoi	- Enable	BOOL	5-wire JTAG 4-wire JTAG					
		Tents	Require XRES Pin	BOOL	SWD (serial wire debug)					
e		2	Use Optional XRES	BOOL						
	_	esul	• Voltage Configuration							
		ŝ								

#### Figure 26. Debug Ports Disabled

3. Compile and program the PSoC 3 or PSoC 5LP device.

Note that the debug port must be manually enabled again if debugging is needed. Disabling the debug interface does not affect the ability to program the device.

## 4.7 Toggle GPIOs Faster with Data Registers

This example demonstrates how to use port data registers and masks to quickly toggle pins. While the Component API is the easiest way to control GPIO pins, the number of processor cycles needed to update the pin can affect how fast a toggle can occur. The register definitions and masks in the *<pin\_name>.h* file that is created for each Component can be used to more quickly update pins.

- 1. Place a digital output pin in the schematic and name it "MyPin" for convenience.
- Configure the Component with no hardware connection and assign it to a physical pin (this example uses P6[0]), as Figure 27 shows.



Figure 27. Pin Placed in Schematic



3. Add the following code to the *main.c* file:

```
for(;;)
{
    // These are API functions
    MyPin_Write(1); //set MyPin output
    MyPin_Write(0); //clear MyPin output
}
```

4. Observe the output of P6[0] using the API, as Figure 28 shows.

Figure 28. Pin Toggle Using API Switch Method



5. Replace the previous code in *main.c* with this code:

```
for(;;)
{
    MyPin_DR |= MyPin_MASK; //Set MyPin
    MyPin_DR &= ~MyPin_MASK; //Clear
}
```

6. Observe the output of P6[0] using the fast switching method, as Figure 29 shows.

Figure 29. Pin Toggle Using Fast Switching Method





A pin can toggle almost four times faster using the fast switching method rather than the API functions. This code also has the advantage of being portable. If the pin assignment is changed during development, you do not have to write to a specific physical pin's registers.

## 4.8 Use 8051 Special Function Registers

The 8051 in PSoC 3 has a set of special function registers (SFRs) that allow faster access to a limited set of PSoC registers. You can use two of those registers to quickly toggle GPIO pins.

- 1. Place a Digital Output Pins Component in the project schematic and assign it to a physical pin, just as you did in the previous example. This example also uses P6[0].
- 2. Add the following code to the main.c file:

```
/* Enable SFR access for P6[0]. */
/* Only done once in the beginning. */
SFRPRT6SEL |= 0x01;
/* Toggle GPIO pin. */
for(;;)
{
    /* Switch on P6[0] */
    SFRPRT6DR |= 0x01;
    /* Switch off P6[0] */
    SFRPRT6DR &= ~0x01;
}
```

3. Alternatively, use this method:

```
for(;;)
{
    /* Toggle P6[0] */
    SFRPRT6DR ^= 0x01;
}
```

Either method will result in very fast pin toggles. For more information on the SFRs, see the PSoC 3 Architecture TRM.

## 4.9 Use Both Analog and Digital on a GPIO

This example demonstrates how to configure and use a pin for both analog and digital functions. Assume that a GPIO pin needs to output a 10-kHz clock signal for a short time, switch to a reference voltage for a short time, and then switch back to the 10-kHz signal.

- 1. Place an analog pin, a  $V_{REF}$ , and a clock in the schematic.
- 2. Assign the Pins Component to a physical pin (this example uses P3[6]), as Figure 30 shows.

Figure 30. Basic Components Placed in the Schematic

Vdda/2 Vref	-									-	
· · · · · · · · · <del>· · · ·</del> · · ·											
MvE	Din	Ĵ.	2161	ı.							
IVIYE		Į.	slol	5		Ļ					
Clock 1											
		÷.					÷.	÷.	÷.	÷.	

3. Configure the pin with both analog and digital output settings, as Figure 31 shows.



Configure 'cy_pins'	-	<u>ନ୍ଥ</u> ×
Name: MyPin		
Pins Mapping R	eset Built-in	4 Þ
Number of Pins: 1	X 🗗 🕈 関 🕺	
[All Pins]	Type General Inp	ut Output
····⊠ MyPin_0	Analog	Preview:
	<ul> <li>Digital Input</li> <li>HW Connection</li> <li>Digital Output</li> <li>HW Connection</li> <li>Output Enable</li> <li>Bidirectional</li> </ul>	
Data Sheet	ОК	Apply Cancel

Figure 31. MyPin Configured as Both Analog and Digital

4. Connect the clock to the digital terminal and the V<sub>REF</sub> to the analog terminal, as Figure 32 shows.

Figure 32. PSoC Creator Schematic of Analog and Digital Switching Scheme



- 5. Compile the project to create the API necessary to determine the analog routing that PSoC Creator uses.
- 6. Open the *cyfitter\_cfg.c* file and look for either CYREG\_PRT3\_AG (the analog global enable) or CYREG\_PRT3\_AMUX (the analog mux bus enable). In this case, the routing tool has chosen to use the AG bus for Port 0, as follows.

CY SET REG8(CYREG PRT3 AG, 0x40);

Note that the analog routing may change whenever the project is rebuilt. If any changes are made to the project, you must check the routing.

7. Add the following code to the *main.c* file:

```
for(;;)
{
   /* Set pin to Analog */
   // Set P3[6] to Analog HI-Z
   CyPins SetPinDriveMode (CYREG PRT3 PC6, PIN DM ALG HIZ);
   // Make AG connection for P3[6]
   CY SET REG8(CYREG PRT3 AG, CY GET REG8(CYREG PRT3 AG) | 0x40);
   // Wait for 100 ms while driving signal
   CyDelay(100);
   /* Set pin to digital */
   // Break AG connection for P3[6]
   CY SET REG8(CYREG PRT3 AG, CY GET REG8(CYREG PRT3 AG) & 0xBF);
   //Set P3[6] to Strong Drive mode
   CyPins SetPinDriveMode (CYREG PRT3 PC6, PIN DM STRONG);
   // Wait for 100 ms while driving signal
   CyDelay(100);
}
```



8. Compile and program the PSoC 3 or PSoC 5LP device.

The result is an output that alternates every 100 ms between the clock signal and the reference voltage.

## 4.10 Control Analog Switching with Hardware

This example shows how an external signal is used to gate the output of an analog pin without CPU intervention.

1. Place a digital input pin (Ext\_Gate in this example), an analog pin (Analog\_Out), and an analog source (VDAC8) in the project schematic, as Figure 33 shows.

Figure 33. Components for Hardware-Controlled Gate



2. Configure the Analog\_Out pin with both analog and digital properties, as Figure 34 shows.

Configure 'cy_pins'		? 🔀
Name: Analog_Out		
Pins Mapping Re	set Built-in	4 ۵
Number of Pins: 1	< 🗗 🕈 🗍 🖉 🐇	
[Al Fins]_ └─ ⊠ Analog_Out_0	Type     General     Input       ✓     Analog     Digital Input       ✓     HW Connection       ✓     Digital Output       ✓     HW Connection       ✓     HW Connection       Øutput Enable	Output Preview:
Data Sheet	Bidirectional	Apply Cancel

Figure 34. Analog\_Out Pin Configuration

3. Configure the drive mode of the Analog\_Out pin as "Open Drain Drives Low," as Figure 35 shows.

Figure 35. Analog\_Out Pin Drive Mode

Configure 'cy_pins'		? 🔀
Name: Analog_Out		
Pins Mapping R	eset Built-in	4 ۵
Number of Pins: 1	X 🗗 🕈 🗍 🐰	
(All Pins)	Type General Input	Output
Analog_Out_0	Drive Mode	Initial State:
	Open Drain, Drives Low	🗙 Low (0)
		Minimum Supply Voltage:
Data Sheet	ОК	Apply Cancel



4. Connect the Components, as Figure 36 shows.



5. Add the following line of code to the *main.c* file. In this example, it sets the bidirectional bit for pin 0 in the Port 0 configuration registers:

// Set P0[0] to bidirectional mode
CY\_SET\_REG8(CYDEV\_IO\_PRT\_PRT0\_BIE, 0x01);

- 6. Assign the Analog\_Out pin to P0[0] to match the previous code.
- 7. Compile and program the PSoC 3 or PSoC 5LP device.

Figure 37, which is taken from the detailed GPIO block diagram in the PSoC 3 and PSoC 5LP datasheets, shows how the GPIO control logic is used to implement this technique.

Figure 37. Highlighted GPIO Block Diagram from PSoC 3 and PSoC 5LP Datasheets



The Ext\_Gate signal is routed through the DSI to the digital portion of the Analog\_Out pin. The signal from the DSI (red) is routed to the analog switches because the port bidirectional bit and the analog global select bit are set (yellow). The VDAC output (blue) is switched on or off depending on the logic state of the Ext\_Gate signal.

For more details on the analog switching available in PSoC 3 and PSoC 5LP devices, see the "Analog Routing" section of the TRM. Another good resource is the application note AN58827 – PSoC 3 and PSoC 5LP Internal Analog Routing Considerations.



## 4.11 Use the DSI as a Clock Source

This example demonstrates how to use a digital signal routed through the DSI as a clock source. As many as eight digital and four analog clocks can be created from an arbitrary DSI signal. Also, the PSoC device can use an arbitrary digital signal as an input source for the PLL.

1. Place a digital input pin, a digital output pin, and a clock in the schematic, as Figure 38 shows.

Figure 38. Basic Components for DSI Clock Example



2. Open the configuration dialog for Signal\_In and deselect the **Input Synchronized** option in the pin configuration window, as Figure 39 shows. This is necessary to prevent the signal from trying to sync to itself.

onfigure 'c	y_pins'	maye	? <mark>×</mark>
Name:	Signal_In		
Pins	Mapping Re	eset Built-in	4 Þ
Number	of Pins: 1	× 🛛 🕈	♣ X X
[All Pins]		Туре	General Input Output
- 🖂 Isi	gnal_in_0	Threshold:	CMOS   Hysteresis
		Interrupt:	None 🔹
			Hot Swap
			Input Buffer Enabled
			Input Synchronized
		, 	
Data S	Sheet	(	OK Apply Cancel

Figure 39. Input Synchronized Setting Disabled

- 3. Connect the clock to Signal\_Out with the wire tool.
- 4. Use the wire tool to create a signal for the DSI source that is connected only to Signal\_In. Start away from the terminal of Signal\_In to create the wire, as shown in Figure 40.

Figure 40. DSI Clock Source Signal

Signal_In @				
Clock_1 Signal_ 24 MHz	_(	D C	ut	t

- 5. Right-click on the wire and select Edit Name And Width from the pop-up menu that appears.
- 6. Deselect the **Use computed name and width** option and type a unique name ("MySignal" in this example) in the **Signal Name** field, as Figure 41 shows.



Figure 41. Signal Name Configuration Window

Signal Name				
Specify Full	Name			
MySignal				
Indices				
None				
⊚ Bit	Index	0 .		
Bus	Left Index	0	Right Index	0

After these configurations have been set, the schematic will resemble Figure 42.

Figure 42. Modified Components for DSI Clock Example



- 7. Open the project's Design-Wide Resources file (*<Project Name>.cydwr*) and select the **Clocks** tab.
- 8. Double-click on any of the system clocks to open the Configure Systems Clocks window.
- 9. Select the **Digital Signal** option and click the "..." button to open the **Select Input Signal** window.
- 10. Select "MySignal" and enter the signal frequency (3 MHz in this example) and accuracy, as Figure 43 shows.

Figure 43. Digital Signal Configuration Window

Select Input Signal	-	ingen in	-		? ×
Signal Frequency:	3.000 MHz	Accuracy: -	0%	+ 0%	`- ȱ
<sup>®</sup> La MySignal					
Show un-name	ed signals				
			ОК		ancel

Note that PSoC Creator uses this information to perform calculations needed to configure the system clocks. Make sure that the signal information is accurate.

11. Set the input source for the internal main oscillator (IMO) and PLL to "Digital Signal," as Figure 44 shows.



		<u> १</u> ×
→ 🔽	IMO	Digital Signal
Osc	12.000 MHz	Name: MySignal
XTAL	<ul> <li>Digital Signal</li> </ul>	Freq: 3.000 MHz
	1†.	
	PLL	Master Clock
	Input: Digital Signal (3.000 MI 👻	PLL_OUT (24.000 MHz)
	Desired: 24 MHz V	Freq  Divider
5 V	Actual: 24.000 MHz	1
OM OM	, .	· · · · ·
	USB	Bus Clock
Click head	er to enable the	Freq Oivider
03	BCIOCK	1

Figure 44. DSI Signal as the Source for the IMO and PLL

The PLL uses the 3-MHz input to generate a 24-MHz output, which is routed to the Master and Bus clocks to generate the Signal\_Out clock.

For more details on the DSI system clocking, see the datasheet, TRM, and application note AN60631 – PSoC 3 and PSoC 5LP Clocking Resources.

## 4.12 Change PICU Settings with Firmware

Dynamic configuration of the PICU is done through a write to bits [1:0] of the PICUx\_INTTYPEy register, where "x" corresponds to the port number and "y" corresponds to the pin number (see Table 2). You can change the configuration at any time to enable or disable pin interrupts.

Bits 1:0	Name	Description	
00	Disable	Interrupts disabled	
01	Rising Edge	Trigger on rising edge	
10	Falling Edge	Trigger on falling edge	
11	Change Mode	Trigger on any edge	

Table 2. PICU Interrupt Types and Bit Settings

In this example, pin P6[0] is configured as a rising-edge interrupt, and P6[1] is configured as a falling-edge interrupt.

- 1. Place two digital input pins in the project schematic.
- 2. Assign the pins to P6[0] and P6[1].
- 3. Configure P6[0] as a resistive pull-down pin, or add an external pull-down.
- 4. Configure P6[1] as a resistive pull-up pin, or add an external pull-up.
- 5. Add the following code to the *main.c* file:

```
//Set P6[0] to PICU rising-edge trigger
CY_SET_REG8(CYREG_PICU6_INTTYPE0, 0x01);
//Set P6[1] to PICU falling-edge trigger
CY_SET_REG8(CYREG_PICU6_INTTYPE1, 0x02);
//Sleep and wait for PICU interrupt
//Sleep again if not P6[1] PICU wakeup
do
{
```



}

//Save clocks and enter sleep CyPmSaveClocks(); CyPmSleep(PM SLEEP TIME NONE, PM SLEEP SRC PICU); CyPmRestoreClocks(); //Stay awake for two seconds CyDelay(2000); while (!(CY GET REG8(CYREG PICU6 INTSTAT) & 0x02)); //Disable P6[1] PICU trigger CY SET REG8(CYREG PICU6 INTTYPE1, 0x00);

### 6. Compile and program the PSoC 3 or PSoC 5LP device.

The PSoC device will wake from sleep on any PICU interrupt, but it will return to sleep again unless P6[1] was the trigger. You are not required to disable the interrupts after wakeup. They can be used during normal operation like any other interrupt source.

The PSoC 3 or PSoC 5LP TRM contains further information about the PICU, including block diagrams and functional descriptions. Another good resource is the application note AN54460 - PSoC 3 and PSoC 5LP Interrupts.

#### 4.13 Gang Pins for More Drive/Sink Current

To increase the total source/sink capabilities of the circuit, GPIO pins can be ganged (shorted together). The limitations of V<sub>DDIO</sub> quadrants still apply. This example demonstrates driving a PWM signal with four GPIO pins.

- 1. Place and configure a PWM and a Clock Component.
- Place a single Digital Output Pins Component and connect it to the PWM output terminal, as Figure 45 shows. 2.



Figure 45. Single Pin Placed in Schematic

Open the Pins configuration dialog and set the number of pins accordingly, as Figure 46 shows. This example 3. uses four GPIO pins.

Configure 'cy_pins'		8 ×
Name: MyGang		4.5
Number of Pins: 4		
[All Pins] — ⊠ MyGang_0 — ⊠ MyGang_1 — ⊠ MyGang_2 — ⊠ MyGang_3	Type     General     Input       Analog     Digital Input     Input       Ugital Input     Input     Input       Upital Output     Input     Input       Upital Output     Input     Input       Upital Output     Input     Input       Input     Input     Input<	Output Preview:
Data Sheet	ОК Ар	ply Cancel

Figure 46. Configure Multiple Pins in the Component

Optionally, set the pin mapping to **Contiguous** for easier PCB routing, as Figure 47 shows. 4.



Figure 47. Enable Contiguous Mapping

Configure 'cy_pins'	2	х
Name: MyGang		
Pins Mapping Reset Built-in	٩	⊳
Display as Bus		*
Selects whether to display individual terminals for each pin or a single wide terminal The bus options is only valid when pins are homogeneous, which means that all pin component have the same pin type, output/input HW connections, SIO grouping, all either use or don't use the SIO Vref.	(bus). is in the and they	
Forces placement in adjacent physical pins. Forces placement in adjacent physical pins. Port-level APIs will only be generated for this instance if it is set to be Contiguous. Per-pin APIs will be globally available either way.		
Spanning		
Allows placement in multiple physical ports. Note: Spanning is currently configured based on the Contiguous setting. This will no case in the future.	ot be the	•
Data Sheet OK Apply	Cancel	

- 5. Assign the Pins Component to physical pins.
- 6. Connect the signal source (PWM in this example) to each of the pin terminals in the Component, as shown in Figure 48.



7. Compile and program the PSoC 3 or PSoC 5LP device.

The output of the PWM will be driven on all four GPIOs. The pins can be shorted externally on the PCB and connected to the external circuit as needed.

### 4.14 Level-Shift Signals

The GPIO pins can be used for level-shifting of signals by powering the  $V_{DDIO}$  pins at different voltages. The only limitation is that no  $V_{DDIO}$  quadrant may be at a higher voltage than  $V_{DDA}$ . This example demonstrates how to create a simple 5-V/1.8-V level shifting configuration in the PSoC 3 or PSoC 5LP device.

- 1. Place two High-Z digital input pins and two Strong Drive digital output pins in the project schematic.
- 2. Connect one of the inputs to one of the outputs. Connect the remaining input to the remaining output.
- 3. For convenience, give the pin symbols meaningful names similar to the ones shown in Figure 49.

Figure 49. Level-Shifting with GPIO Pins

In_High 1209	

- Assign the 5-V signals to pins in one V<sub>DDIO</sub> quadrant, and the 1.8-V signals to pins in another quadrant. For this example, V<sub>DDIO</sub>3 (5.0 V P12[1:0]) and V<sub>DDIO</sub>0 (1.8 V P4[1:0]) were chosen. See the device datasheet for V<sub>DDIO</sub> distributions.
- 5. On the development board, connect V<sub>DDD</sub>, V<sub>DDA</sub>, V<sub>DDI0</sub>1, V<sub>DDI0</sub>2, and V<sub>DDI0</sub>3 to a 5-V supply.



- 6. Connect  $V_{DDIO}0$  to a 1.8-V supply.
- 7. Compile and program the PSoC 3 or PSoC 5LP device.

Any 5-V signal applied to the high-side input will appear at 1.8 V on the low-side output. Likewise, any 1.8-V signal applied to the low-side input will appear at 5 V on the high-side output, as Figure 50 shows.



In addition to shifting the voltage of the signal, the PSoC device can read and manipulate the data as it passes through. Remember that all GPIO pins in a  $V_{DDIO}$  quadrant will be at the same voltage.

# 5 Related Application Notes

- AN54181 Getting Started with PSoC 3
- AN77759 Getting Started with PSoC 5LP
- AN60631 PSoC 3 and PSoC 5LP Clocking Resources
- AN58304 PSoC 3 and PSoC 5LP Pin Selection for Analog Designs
- AN58827 PSoC 3 and PSoC 5LP Internal Analog Routing Considerations
- AN54460 PSoC 3 and PSoC 5LP Interrupts
- AN60580 SIO Tips and Tricks in PSoC 3/PSoC 5LP
- AN77900 PSoC 3 and PSoC 5LP Low-power Modes and Power Reduction Techniques
- AN52705 PSoC 3 and PSoC 5LP Getting Started with DMA

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Greg Reynolds has been with Cypress in several roles for more than a decade.



# Appendix A. GPIO API and Register Reference

## A.1 Component API

The Pins Component API is used to access all physical pins associated with a Component. The instance name of the Component, either assigned by the user or generated by PSoC Creator, is used as the prefix for the function name. The Component APIs are documented in detail in the Pins Component datasheet. Table 3 lists the Component functions.

API	Description	Example (using a Component name of MyPin)
<pin_name>_Read</pin_name>	Returns the current value for all pins in the Component.	<pre>myVar = MyPin_Read();</pre>
<pin_name>_Write</pin_name>	Writes the value to the Component pins.	<pre>MyPin_Write(1);</pre>
<pin_name>_ReadDataReg</pin_name>	Returns the current value for all pins in the Component.	<pre>myVar = MyPin_ReadDataReg();</pre>
<pin_name>_SetDriveMode</pin_name>	Sets the drive mode for each of the Component's pins.	MyPin_SetDriveMode(MyPin_DM_ALG_HIZ);
<pin_name>_ClearInterrupt</pin_name>	Clears any active interrupts on the port into which the Component is mapped. Returns the value of interrupt status register.	<pre>myVar = MyPin_ClearInterrupt();</pre>

### Table 3. Component API Reference

## A.2 Per-Pin API

You can access individual physical pins by using the global per-pin API macros. The physical pins do not need to be associated with a Pins Component because the macros directly access the pin configuration registers. Using per-pin APIs can result in undefined behavior in any physical pin associated with a Pins Component due to conflicts with the Component configuration. The per-pin APIs are documented in detail in the PSoC Creator System Reference Guide. Table 4 lists the per-pin functions.

API	Description	Example (using P1[2])
CyPins_ReadPin	Reads the current value on the pin.	<pre>myVar = CyPins_ReadPin(CYREG_PRT1_PC2);</pre>
CyPins_SetPin	Sets the output value for the pin to logic HIGH.	CyPins_SetPin(CYREG_PRT1_PC2);
CyPins_ClearPin	Sets the output value for the pin to a logic LOW.	CyPins_ClearPin(CYREG_PRT1_PC2);
CyPins_SetPinDriveMode	Sets the drive mode for the pin.	CyPins_SetPinDriveMode(CYREG_PRT1_PC2, PIN_DM_ALG_HIZ);
CyPins_ReadPinDriveMode	Reads the drive mode for the pin.	<pre>myVar = CyPins_ReadPinDriveMode(CYREG_PRT1_PC2);</pre>
CyPins_FastSlew()	Sets the slew rate for the pin to fast edge rate.	CyPins_FastSlew(CYREG_PRT1_PC2);
CyPins_SlowSlew()	Sets the slew rate for the pin to slow edge rate.	CyPins_SlowSlew(CYREG_PRT1_PC2);



# A.3 GPIO Registers

The following registers are used to configure the GPIOs. They are accessible by firmware during normal operation. Further details and register maps are in the PSoC 3 and PSoC 5LP Registers TRM documents that are available for free from the Cypress website. Table 5 lists the GPIO registers.

Register	Name	Description
PRTx_PCy[7:0]	Port Pin Configuration	This register accesses several configuration or status bits of a single I/O port pin at once.
PRTx_DR[7:0]	Port Data Output	This register is used to set the output data state for the corresponding GPIO port.
PRTx_PS[7:0]	Port Pin State	This register holds the logical pin state for the corresponding GPIO port. If the drive mode for the pin is set to High-Z Analog, the state will always read 0.
PRTx_DM2[7:0] PRTx_DM1[7:0] PRTx_DM0[7:0]	Port Drive Mode	These registers' combined value determines the unique drive mode of each bit in a GPIO port.
PRTx_SLW[7:0]	Port Slew Rate Control	This register is used to set a fast or slow edge rate for any strong drive mode GPIO pin.
PRTx_BYP[7:0]	Port Bypass Enable	This register selects whether the output data for the corresponding GPIO is sourced from the DSI or port logic data register.
PRTx_BIE[7:0]	Port Bidirection Enable	This register is used to enable dynamic bidirectional control through the DSI.
PRTx_INP_DIS[7:0]	Input Buffer Disable Override	This register is used to force the input buffers off.
PRTx_CTL[0]	Port Wide Control Signals	This register is used to select the internal buffer trip point.
PRTx_PRT[7:5,3:1]	Port Wide Configuration	This register accesses several available configuration registers on a port-wide basis with a single bit write.
PRTx_BIT_MASK[7:0]	Bitmask for Aliased Register Access	This register allows or blocks access to the data registers from the aliased register address space.
PRTx_AMUX[7:0]	Port Analog Global Mux Bus Enable	This register controls the analog global mux switch for the corresponding GPIO port.
PRTx_AG[7:0]	Port Analog Global Enable	This register controls the analog global switch for the corresponding GPIO port.
PICUx_INTTYPE[1:0]	Port Interrupt Control Type	This register configures the type of interrupt for the corresponding GPIO pin.
PICUx_INTSTAT[7:0]	Port Interrupt Control Status	This register shows posted interrupts for the corresponding GPIO port.
PICUx_SNAP[7:0]	Port Interrupt Control Snapshot	This register shows the state of input pins at the last read of the PICUx_INTSTAT register.
PICUx_DISABLE_COR[0]	Disable Status Register Clear on Read Feature	This register disables the "clear on read" feature of the PICUx_INTSTAT register.

## Table 5. GPIO Registers



## A.4 Nonvolatile Latches

PSoC 3 and PSoC 5LP have an array of nonvolatile latches (NVLs) that are used to configure the device behavior in reset. The following latches are used to configure the GPIOs. They are not accessible from firmware during normal operation. Further details and register maps for the NVL array are included in the "Nonvolatile Latches" section of the PSoC 3 and PSoC 5LP datasheets and TRM. Table 6 lists the NVL latches.

NVL Latch	Name	Description
PRTxRDM[1:0]	Port Reset Drive Mode	Controls reset drive mode of the corresponding I/O port.
XRESMEN[0]	Optional XRES Enable	Controls whether pin P1[2] is used as a GPIO or as an external reset.
DPS[1:0]	Debug Port Select	Controls the use of various Port1 pins as a debug port.

## Table 6. NVL Latches Relating to GPIOs





# Appendix B. PSoC Creator Settings and Registers

The GPIO settings established in PSoC Creator are part of the cy\_boot startup code and take effect during initial device configuration. The tables in this appendix show the relationship between the settings in the Pins Component configuration window and the GPIO registers. In addition, simple code examples demonstrate how to perform the same function in the firmware during normal operation, if applicable. The configuration window may look slightly different, depending on which version of PSoC Creator you are using.

Table	7.	Drive	Mode	Parameter
rabic		DIIVO	mouc	

Drive Mode				
This parameter configures the pin to provide one of the eight available pin drive modes. Pin type determines default settings.				
PSoC Creator Configuration Window	Component APIs			
Configure 'cy_pins'	<pinname>_SetDriveMode()</pinname>			
Pins     Mapping     Reset     Built-in     Image: Additional system       Number of Pins:     1     X     X     X       [All Pins]     Type     General     Input     Output       Drive     Mode     Initial State:       Strong Drive     Low (0)	Per-Pin APIs CyPins_SetPinDriveMode() CyPins_ReadPinDriveMode()			
Strong Drive         Open Drain, Drives High         Open Drain, Drives Low         Resistive Pull Up         Resistive Pull Down         Resistive Pull Up/Down         High Impedance Digital         High Impedance Analog         Data Sheet         OK       Apply         Cancel	Associated Registers PRTx_PCy[3:1] PRTx_DMy[7:0] PRTx_BIE[7:0]			
Code Examples				
/* Set pin to Resistive Pull-up Using Component API */ MyPin_SetDriveMode(MyPin_DM_RES_UP);				
<pre>/* Set pin to Resistive Pull-up Using Per-Pin API */ CyPins_SetPinDriveMode(CYREG_PRT1_PC2,PIN_DM_RES_UP); /* Read Drive Mode Using Per-Pin API */ mular = CuBing BeadDipDriveMode(CYDEC_DDF1_DC2);</pre>				
<pre>/* Set pin to Resistive Up/Down Using Register Write */ CY_SET_REG8(CYREG_PRT1_PC2, CY_GET_REG8(CYREG_PRT1_PC2)   0x07);</pre>				



## Table 8. Initial State Parameter

Initial State				
This parameter specifies the value written to the pin's data register after power-on reset (POR).				
PSoC Creator Configuration Window	Component APIs			
Configure 'cy_pins'	<pinname>_Write()</pinname>			
Pins     Mapping     Reset     Built-in     ↓ ▷       Number of Pins:     1     × ▷     ▲     ▲       [All Pins]     ✓     ✓     General     Input       □     MyPin_0     □     □     □       □     Strong Drive     ✓     Low (0)     ✓	Per-Pin APIs			
Low (0) High (1) Voltage:	Associated Registers			
	PRTx_DR[7:0]			
Code Examples				
/* Set pin to logic state HIGH output */ MyPin_Write(1);				
<pre>/* Set pin P1[2] to logic state HIGH output */         CyPins_SetPin(CYREG_PRT1_PC2);</pre>				
<pre>/* Set pin P1[2] to logic state LOW output */</pre>				
<pre>/* Set pin P1[2] output to logic state LOW using a register write */ CY_SET_REG8(CYREG_PRT1_DR, CY_GET_REG8(CYREG_PRT1_DR)   0xFB);</pre>				



## Table 9. Threshold Parameter

Threshold			
This parameter selects the threshold levels that define a logic HIGH level (1) and a logic LOW level (0). The setting applies to all physical pins in the port. Only CMOS and LVTTL settings are valid for GPIO pins.			
PSoC Creator Configuration Window	Component APIs		
Configure 'cy_pins'	N/A		
Number of Pins:     1     X     A     +     E       [All Pins]     Type     General     Input     Output	Per-Pin APIs		
MyPin_0 Threshold: CMOS → Hysteresis CMOS CMOS or LVTTL LVTTL 0.4 x Vddio 0.5 x Vddio 0.5 x Vref Vref	N/A Associated Registers PRTx_CTL[0]		
Data Sheet OK Apply Cancel			
Code Examples			
<pre>/* Set port 1 logic threshold to CMOS using a register write */         CY_SET_REG8(CYREG_PRT1_CTL, 0);</pre>			
<pre>/* Set port 1 logic threshold to LVTTL using a register write */         CY_SET_REG8(CYREG_PRT1_CTL, 1);</pre>			



## Table 10. Interrupt Parameter

Interrupt				
This parameter selects the interrupt type of the GPIO.				
PSoC Creator Configuration Window	Component APIs			
Configure 'cy_pins'     ? ×       Name:     MyPin       Pins     Mapping       Reset     Built-in       A     >       Number of Pins:     1       Image: All Pins     Imput       Image: All Pins     Imput       Image: All Pins     Imput       Image: All Pins     Imput       Image: All Pins     Image: All Pins       Image: All Pins     Image: All Pins	N/A Per-Pin APIs N/A Associated Registers PICUx_INTTYPEy[1:0]			
Data Sheet OK Apply Cancel				
Code Examples	1			
/* Disable interrupt on P1[2] */ CY_SET_REG8(CYREG_PICU1_INTTYPE2, 0x00);				
<pre>/* Enable rising-edge interrupt on P1[2] */ CY_SET_REG8(CYREG_PICU1_INTTYPE2, 0x01);</pre>				
<pre>/* Enable falling-edge interrupt on P1[2] */ CY_SET_REG8(CYREG_PICU1_INTTYPE2, 0x02);</pre>				
<pre>/* Enable any edge interrupt on P1[2] */     CY_SET_REG8(CYREG_PICU1_INTTYPE2, 0x03);</pre>				



## Table 11. Input Buffer Enabled Parameter

Input Buffer Enabled				
This parameter determines if the pin's digital input buffer is enabled.				
PSoC Creator Configuration Window	Component APIs			
Configure 'cy_pins'         Name:       MyPin         Pins       Mapping         Reset       Built-in         Vumber of Pins:       1         Type       General         Input       Output         Threshold:       CMOS         Interrupt:       None         Hot Swap       Input Buffer Enabled         Imput Synchronized       Input Synchronized	N/A Per-Pin APIs N/A Associated Registers PRTx_INP_DIS[7:0]			
Code Examples				
<pre>/* Disable Input Buffer on P1[2] using register write. */ CY_SET_REG8(CYREG_PRT1_INP_DIS, CY_GET_REG8(CYREG_PRT1_INP_DIS)   0x04);</pre>				



## Table 12. Input Synchronized Parameter

Input Synchronized			
This parameter enables synchronization of the input of the pin to the bus clock.			
PSoC Creator Configuration Window	Component APIs		
Configure 'cy_pins'     ?       Name:     MyPin       Pins     Mapping       Reset     Built-in       Vumber of Pins:     1       X     Image: Arrow of Pins:       Image: Arrow of Pins:     1       Image: Arrow of Pins:     1 <t< td=""><td>N/A Per-Pin APIs N/A</td></t<>	N/A Per-Pin APIs N/A		
✓ Input burler Linburg ✓ Input Synchronized	Associated Registers		
Data Sheet OK Apply Cancel	PRTx_DBL_SYNC_IN[7:0]		
Code Examples			
<pre>/* Sync input of P1[2] to bus_clk using register write. */</pre>			



## Table 13. Slew Rate Parameter

Slew Rate			
This parameter determines the rise and fall ramp rate for the pin as it changes output logic levels.			
PSoC Creator Configuration Window	Component APIs		
Configure 'cy_pins'	N/A		
Pins     Mapping     Reset     Built-in     ↓ ▷       Number of Pins:     1     ×     Ø     Ø			
	Per-Pin APIs		
Imple     Series and input     Output       Slew Rate:     Fast       Drive Level:     Slow       Fast     Current:       4mA source, 8mA sink	CyPins_FastSlew(CYREG_PRTx_PCy) CyPins_SlowSlew(CYREG_PRTx_PCy)		
	Associated Registers		
Data Sheet OK Apply Cancel	PRTx_SLW[7:0]		
Code Examples			
<pre>/* Set fast edge rate for P1[2] */ CyPins_FastSlew(CYREG_PRT1_PC2);</pre>			
<pre>/* Set slow edge rate for P1[2] */ CyPins_SlowSlew(CYREG_PRT1_PC2);</pre>			
<pre>/* Set slow edge rate for P1[2] */         CY_SET_REG8(CYREG_PRT1_SLW, CY_GET_REG8(CYREG_PR</pre>	RT1_SLW)  = 0x02);		



## Table 14. Output Synchronized Parameter

Output Synchronized				
This parameter synchronizes the output drivers of the pin to the bus clock.				
PSoC Creator Configuration Window	Component APIs			
Configure 'cy_pins'         Name:       MyPin         Pins       Mapping         Reset       Built-in         Number of Pins:       1         X       X         Image: All Pins       Image: All Pins         Image: All Pins       Ima	N/A Per-Pin APIs N/A Associated Registers PRTx_SYNC_OUT[7:0]			
Code Examples				
<pre>/* Sync output of P1[2] to bus_clk using register write. */         CY_SET_REG8(CYREG_PRT1_SYNC_OUT, CY_GET_REG8(CYREG_PRT1_SYNC_OUT)   0x04);</pre>				



## Table 15. POR Parameter

Power-On Reset (NVL Array)			
This parameter determines how the pin behaves during reset. It is not configured during the boot process. Note that the POR setting is a per-por physical port to have the same value. This register is part of the NVL array	the same as the operating drive mode, which is t setting, which requires all pins placed in the same and cannot be changed during normal operation.		
PSoC Creator Configuration Window	Component APIs		
Configure 'cy_pins'     P       Name:     MyPin       Pins     Mapping       Reset     Built-in	N/A		
Power-On Reset: Don't Care	Per-Pin APIs		
The Power-On Reset High-Z Analog semi-permanent attribute that should not the pin behaves out of reset and is not process. In almost all cases, the hardware default of Hi-Z is appropriate and this parameter does not need to be changed. Note that the Power-On Reset setting is a per-port setting so all pins placed in the same physical port must have the same value (or be set to Don't Care in which case they will all end up with the same value). WARNING: Care should be taken during development if this setting is changed. Excessive reprogramming of the POR setting will cause the pin to fail. It is recommended that this is left as "Don't to be taken during development is the setting is changed. Excessive reprogramming of the POR setting will cause the pin to fail. It is recommended that this is left as "Don't to be taken during development is this setting is changed. Excessive reprogramming of the POR setting will cause the pin to fail. It is recommended that this is left as "Don't to be taken during development is this setting is changed. Excessive reprogramming of the POR setting will cause the pin to fail. It is recommended that this is left as "Don't to be taken during development is this setting is changed. Excessive reprogramming of the POR setting will cause the pin to fail. It is recommended that this is left as "Don't to be taken during development is the set tag "Don't development d	N/A		
Care" so that the pin does not get re-programmed when you download the application. If the POR setting must have a specific value, be sure to lock the pin so that it does not move and cause new			
pins to be programmed each time you change your design.       Data Sheet       OK       Apply       Cancel			
Code Examples			
See the PSoC 3 Device Programming Specifications or PSoC 5LP Device Programming Specifications documents for details and instructions on programming the NVL array.			



## Table 16. Enable Optional XRES Parameter

Enable Optional XRES (NVL Array)			
This parameter determines wheth array and cannot be changed dur	ner P1[2] will be configured as ing normal operation.	s an external	reset (XRES) pin. This register is part of the NVL
PSoC Creator	Configuration Window		Component APIs
Start Page TopDesign.cysch Design.cydwr • 4 b ×			N/A
Option	Value		
Configuration			Per-Pin APIs
- Programming\Debugging			N/A
Debug Select	GPIO		
- Enable Device Protection		Accessized Periotere	
- Require XRES Pin			
Use Optional XRES 📃 🔫			XRESMEN[0]
If enabled, a GPIO will be configured	i to be an external reset (XRES) p DMA 📝 System 🔛 Dire		
	Code E	xamples	
See the PSoC 3 Device for details and instruction	Programming Specifications on programming the NVL a	or <mark>PSoC 5LP</mark> array.	Device Programming Specifications documents



## Table 17. Debug Port Select Parameter

	Debug Port Select (NV	/L A	rray)	
This parameter sets the preferred changed during normal operation	d programming and debugging interfact	ce. T	his register i	s part of the NVL array and cannot be
PSoC Creator Configuration Window				Component APIs
Start Page     TopDesign.cysch     Design.cydwr     ▼ < ↓ ×			N/A	
Option	Value	-		
Configuration				Per-Pin APIs
Programming\Debugging			N/A	
Debug Select	GPIO 👻			
Enable Device Protection	5-wire JTAG 4-wire JTAG			
Require XRES Pin	SWD (serial wire debug) SWD+SWV (serial wire debug and viewe			Associated Registers
Use Optional XRES	GPIO	-	DPS[1:0]	
Sets the Port 1 preferred program/de chip enables by default for use after Clocks J Interrupts	bug interface (JTAG or SWD) that the power up or reset. Setting to GPIO frees	+		
	Code Examples	5		
See the PSoC 3 Device Program and instructions on programming	ming Specifications or PSoC 5LP Det the NVL array.	vice	Programmin	g Specifications documents for details



# **Document History**

Document Title: AN72382 - Using PSoC<sup>®</sup> 3 and PSoC 5LP GPIO Pins

Document Number: 001-72382

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3470167	GIR	12/20/2011	New application note
*A	3477593	GIR	12/28/2011	Updated Table 1 and the following text to reflect recent PSoC 5
*В	3526406	GIR	02/28/2012	Updated GPIO Power Structure and Limits section Updated Table 1, VDDIO Quadrant Current Limits Added Toggle section Updated Change PICU Settings with Firmware section.
*C	3820218	MKEA	11/26/2012	Updated for PSoC 5LP and PSoC Creator 2.1 SP1
*D	3884724	GIR	01/25/2013	Added GPIO interrupt sections – Port Interrupt Control Unit and Pins Component Interrupt. Added Special Function Registers section. Added additional text to the Introduction. Minor corrections and changes for overall look and feel.
*E	3942353	MKEA	03/22/2013	Added External Terminals section. Corrected some references to other application notes.
*F	4592891	GJV	12/10/2014	Removed reference to hidden pin component. Updated referenced application note names.
*G	5702158	BENV	04/19/2017	Updated logo and copyright
*H	6033709	GJV	01/16/2018	Added information on creation of a bi-directional data bus. Updated template



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