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Spec No: 001-68173

Spec Title: MIGRATING FROM SERIAL PERIPHERAL INTERFACE (SPI) FRAM TO SPI NVSRAM - AN68173

Sunset Owner: SHIVENDRA SINGH (ZSK)

Replaced by: NONE

Migrating from Serial Peripheral Interface (SPI) FRAM to SPI nvSRAM - AN68173

Author: Shivendra Singh
Associated Project: No
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Software Version: NA
Related Application Notes: AN6023

AN68173 application note describes the hardware/software changes needed at the system level to migrate from SPI FRAM to the SPI nvSRAM

Introduction

Cypress' nonvolatile synchronous random access memory (nvSRAM) cell integrates a fast speed SRAM cell and a SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) based nonvolatile cell into a single nvSRAM cell. The nvSRAM combines the best features of SRAM and EEPROM and makes it the fastest and the most reliable nonvolatile memory solution in the industry. The SRAM is read from and written to it an infinite number of times, while independent nonvolatile data resides in the nonvolatile elements. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation) either automatically when power supply goes off or through user controlled methods such as Software STORE or Hardware STORE (through Hardware Store Busy ( ) pin). Data is retrieved from the nonvolatile cell to the SRAM at power up (the RECALL operation).

The SPI nvSRAMs offer various advantages, such as infinite write cycle, fast access, low power consumption, wide operating voltage options, high endurance cycle in industry standard 8 pin and 16 pin small outline integrated circuit (SOIC) package options. These features of SPI nvSRAM make it one the best in class serial NVRAM product. System currently using any SPI nonvolatile memories, such as EEPROM, FLASH, FRAM or MRAM can easily migrate to SPI nvSRAM with minimal changes in hardware and updates in software.

This application note explains all key design considerations for migrating from SPI FRAM to SPI nvSRAM in a system design. All the details given in this application note help designers to make suitable changes in their system hardware and firmware.

For more information related to the nvSRAM technology and functionalities, see "Nonvolatile SRAM (nvSRAM) Basics – AN6023".

Comparison between nvSRAM and FRAM Technology

Table 1 list out the technology comparison between the SPI FRAM and SPI nvSRAM. These details are required for evaluating the device performance and reliability at the system level.

Table 1. Comparison of nvSRAM and FRAM Technologies

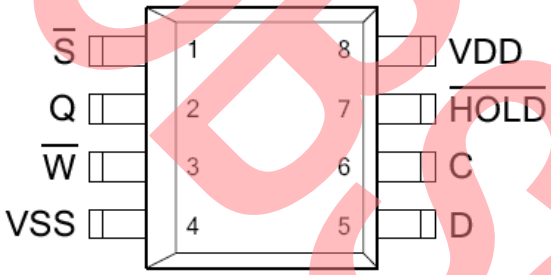
Features	nvSRAM	FRAM
Current Stable Technology	0.13u SONOS process	0.13u FRAM Process
Destructive reads	Not applicable	Due to destructive read, FRAM needs refresh after every read. This causes endurance loss during Read operation.
Endurance - read	Infinite	Total 10^{14} Reads and Writes cycle
Endurance - write	Infinite Write to SRAM 1M nonvolatile Store cycles	Total 10^{14} Reads and Writes cycle
Speed (cycle time)	104 MHz for all Reads & Writes	40 MHz for all Reads & Writes
Power consumption (I_{CC})	3 mA @ 40 MHz	12 mA @ 40 MHz
Standby mode current (I_{SB})	150 uA	150 uA
Sleep mode current	8 uA	8 uA

Replacing SPI FRAM with SPI nvSRAM

The SPI nvSRAM is offered as a pin compatible device with the SPI FRAM, which makes it easier for you to replace the current FRAM based solution with Cypress's nvSRAM. The SPI nvSRAM offers density up to 1 Mbit and operating frequency up to 104 MHz in 8-pin SOIC and 16-pin SOIC industry standard package options.

The SPI FRAMs are popularly available in 8-pin SOIC packages as shown in Figure 1. The SPI nvSRAM is also available in an 8-pin SOIC package, therefore it makes SPI nvSRAM pin compatible with the SPI FRAM.

Figure 1. SPI FRAM Pin Configurations (8-SOIC)



The SPI FRAM includes the following interface pins:

Table 2. SPI FRAM Pin Definition

Pins	Pin Definition
( )	Chip Select used to enable or disable the device
C (SCK)	Serial Clock used to synchronize all data access
D (MOSI)	Serial Input pin to the FRAM
Q (SO)	Serial output from the FRAM
( )	Write Protect pin for hardware write protection
	Hold pin to pause the serial communication

Hold pin to pause the serial communication The first four pins (, SCK, SI, and SO) in the above Table 2 are critical for the SPI communication in a system. The write protect ( ) and hold ( ) pins provide additional functionalities and are used by the controller during memory access. The pin is used to prevent the memory from unintended write operation and mostly enabled when the memory is used as a read only program memory to store the firmware code of a controller. The is used to pause or suspend the ongoing SPI communication in a multi slave SPI configuration.

The SPI nvSRAM is available in two different pin configurations as nvSRAM without AutoStore and nvSRAM with AutoStore in 8-pin SOIC package options.

The SPI nvSRAM without AutoStore feature has a pin configuration that is identical with the SPI FRAM and can replace the FRAM directly on the same footprint as shown in Figure 2.

The nvSRAM with the AutoStore feature needs a dedicated V_{CAP} pin. Hence in this configuration the pin is replaced with the V_{CAP} pin as shown in Figure 3. One must connect a capacitor on the V_{CAP} pin for using nvSRAM's AutoStore feature.

Figure 2. SPI nvSRAM Pin Configuration Without AutoStore (Identical to SPI FRAM)

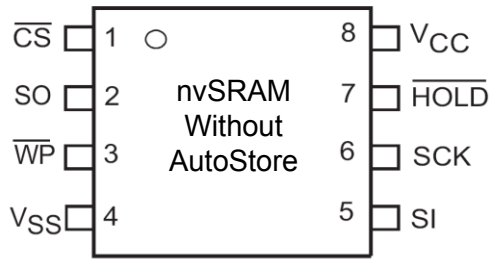
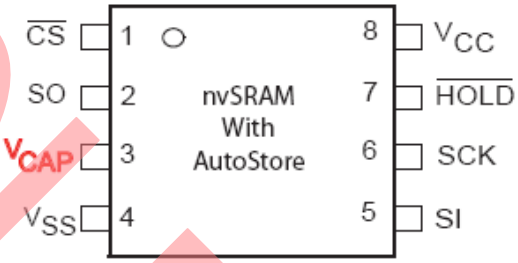


Figure 3. SPI nvSRAM Pin Configuration (With AutoStore)



The following sections describe relevant changes that should be considered in the hardware and/or software for an error free migration.

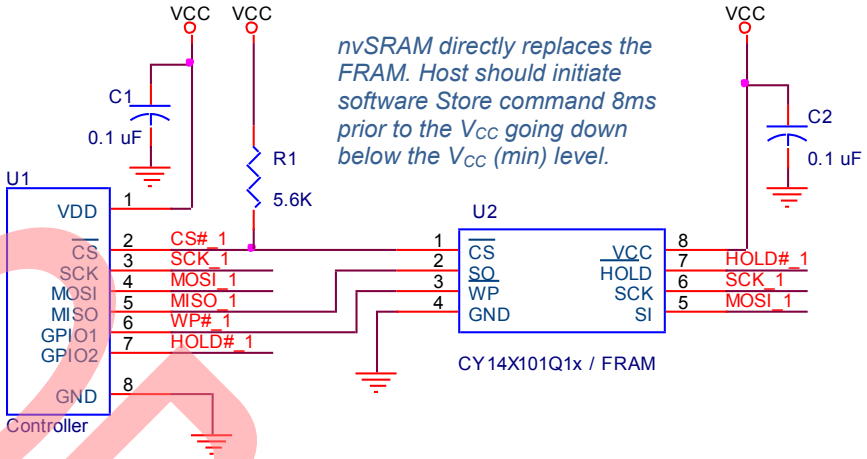
nvSRAM without AutoStore (with Software Store)

The nvSRAM without AutoStore depends on the system's ability to perform a Store operation to secure the data from SRAM to the nonvolatile memory, when the system power goes down. This is a perfect fit for those systems where a sag or failure in the system power supply can be detected in advance. The controller should initiate a software Store and secure the data into nonvolatile memory before shutting down the system's power. Alternatively, systems can have a mechanism of providing power supply to the nvSRAM for an extended duration (upto 8 ms) after detecting the power failure. This will ensure that the nvSRAM successfully completes the software Store cycle initiated by the controller after detecting the power failure.

Hardware Changes

The nvSRAM without the AutoStore option has a pin configuration identical with the FRAM. Therefore, there is no hardware change required to replace the FRAM with nvSRAM. Figure 4 shows an example of SPI nvSRAM connections in a system.

Figure 4. SPI nvSRAM Schematic (No AutoStore Option)



Software Changes

Systems that use the SPI nvSRAM without AutoStore feature should update their software for including the software Store sequence to save the data in non volatile cells of nvSRAM prior to the V_{CC} power down. The software Store operation is initiated in the SPI nvSRAM through a single-byte instruction (Op-code). It takes 8 ms to complete the NV Store cycle. Therefore, it requires the system to hold the nvSRAM V_{CC} power for 8 ms to successfully complete the Store operation once it is initiated. You must also consider the system level differences between the two parts which is mentioned in section Additional System Level Considerations.

nvSRAM with AutoStore (with VCAP Pin)

The SPI nvSRAM with the AutoStore feature requires a small capacitor connected to its VCAP pin to perform a nonvolatile Store automatically at power-down. The nvSRAM charges capacitor connected to its VCAP pin during the normal operation and uses stored charge as a backup power supply during AutoStore operation.

The VCAP pin replaces the hardware write protect pin ( ) in this package option. Figure 5 shows the SPI nvSRAM with AutoStore pin configuration.

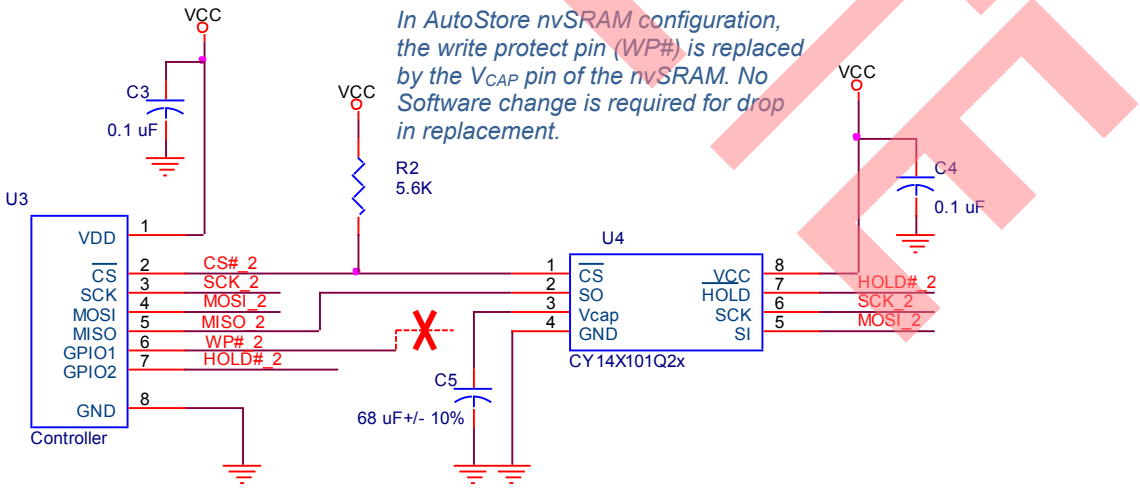
Hardware Changes

Using the nvSRAM with AutoStore feature requires the following hardware changes:

- Remove the controller's GPIO connection to Pin#3 (pin) of the FRAM.
- Connect the V_{CAP} capacitor to Pin#3. Typically the value of V_{CAP} capacitor lies in the range of 61 uF–180 uF for most nvSRAM devices. You must refer to the device datasheet for appropriate capacitor value.

Figure 5 shows an example schematic of the SPI nvSRAM in a system where the write protect ( ) pin is replaced by the V_{CAP} pin for using the AutoStore feature in nvSRAM.

Figure 5. SPI nvSRAM Schematic (With AutoStore Option)



Software Changes

The advantage of using nvSRAM with AutoStore feature is that the controller does not need to initiate a software Store operation at power down. Therefore, systems that use nvSRAM with AutoStore feature do not require any software change for all standard accesses. You must also consider the system level differences between the two parts which is mentioned in section Additional System Level Considerations.

In some applications where the hardware write protect feature is enabled through the hardware pin ( ), replacing those sockets with the nvSRAM with AutoStore will require some software modification to keep the write protect feature enabled. The following section provides a system level overview on using write protect features in applications with respect to different use models.

Write Protection – Use Model

This section explains write protect implementation in applications.

Write Protection through Pin

Typically, applications use the pin in one of the following two configurations.

1. The pin is connected to a dedicated GPIO of the controller. The controller toggles the pin to LOW for preventing any accidental write in the status register and/or protected memory block. Similarly to remove the write protection, the controller must require pulling the pin to HIGH.
2. Tie this pin ground (V_{SS}) in the hardware to save one controller pin and permanently disabling writes to the status register. This use case is mostly applied when memory is used as program memory and needs to be configured as read-only memory.

Needless to say that the pin is most commonly tied to HIGH or connected to a controller pin. In case this pin is tied HIGH, the system does not use this feature and therefore, replacing the FRAM with nvSRAM does not pose any issue. If this pin is tied to the controller in your system, the use of write protection needs to be verified. However, if this pin is tied LOW in your system, you may want to consider whether the hardware write protection is necessary in your system. If so, you should choose the nvSRAM with the Software Store (without AutoStore) option. All the other nvSRAM benefits remain the same over FRAM.

Write Protection through Software

Most applications prefer to use the software write protection instead of hardware protection to save one controller GPIO. Typically, the SPI nonvolatile memories support two levels of write protection through the software.

- Through the write enable latch (WEN) bit. Any write operation must be preceded with a 'Write Enable' (WREN) instruction to set the write enable (WEN) bit. Any attempt to write into nvSRAM is ignored until WEN is set to '1' prior to writing.
- Write protection through the memory block protect. In this scheme the block protect bits BP0 and BP1 of the status register are set accordingly to inhibit the write access to one fourth, half, or the entire memory array. The block protect bits are nonvolatile in nature.

If the is enabled by pulling this pin to LOW, it prevents writing into the status register. However, it does allow writing into unprotected memory block. Therefore, most systems can afford to do away with the hardware write protection feature. If write protection is required then the block based software write protection can be enabled by setting appropriate block protect bits (BP0 and BP1) in the status register.

Additional System Level Considerations

Table 3 lists out all the key feature/functional differences between multiple versions of SPI FRAM devices and Cypress SPI nvSRAMs. These differences should also be considered at the system level for a proper migration.

Table 3. Feature Comparison between SPI FRAM and SPI nvSRAM

Features/ Function	FRAMs	nvSRAM without V_{CAP}	nvSRAM with V_{CAP}
		CY14XXXXQ1A	CY14XXXXQ2A
V_{CC}	2 V to 3.6 V	2.5 V (Typ) - 2.4 V to 2.6 V (CY14CXXXX) 3 V (Typ) - 2.7 V to 3.6 V (CY14BXXXX) 5 V (Typ) - 4.5 V to 5.5 V (CY14EXXXX) (nvSRAM supports 3 operating voltage ranges. Depending upon the application requirement, nvSRAM operating voltage option should be selected).	
	2.7 V to 5.5 V		
PCB Change	-	No change	Add a V_{CAP} at Pin#3
Power up	250 us/10 ms	20 ms	

Features/ Function	FRAMs	nvSRAM without V_{CAP}	nvSRAM with V_{CAP}
		CY14XXXXQ1A	CY14XXXXQ2A
Hardware Write Protect	Yes	Yes	No (No pin)
Status Register	Device with Bit 6 is "1", Programmed with Serial No (Factory Set)	Bit 6 is SNL (Serial Number Lock). Factory default is 0. You can set this bit to "1" to lock the serial number after writing a new 8 Bytes serial number.	
	Device with Bit 6 is "0".	Bit 6 is SNL (Serial Number Lock). Factory default is 0. You can leave this bit to factory default setting "0" if not used.	
	Bit 0 is "0"	Bit 0 is . Default value is “0”. It is set to “1” during Store cycle, which is required only at power fail.	
Power down Store	Automatic	Host is required to initiate a Software Store and save the SRAM data into NV memory before power down.	Automatic
Last access to power down	0 µs	8ms, during which Store needs to be initiated.	0 µs, part automatically performs a Store for 8ms.
Time to enter sleep	Not specified	8 ms	
Wake from sleep	400 µs	20ms	
Device ID	7 Bytes. (This feature is available in select FRAM parts only).	4 Bytes (Available in All nvSRAMs)	
Serial Number	8 Bytes, Factory set. (This feature is available in select FRAM parts only)	8 Bytes, set by the user. (Available in All nvSRAMs)	

Summary

Cypress nvSRAM allows faster, easier, and more reliable data storage than FRAM. The SPI nvSRAMs are available in compatible packages, which make it easy to replace FRAM with the nvSRAM in any application.

Document History

Document Title: Migrating from Serial Peripheral Interface (SPI) FRAM to SPI nvSRAM – AN68173

Document Number: 001-68173

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3221809	ZSK	04/11/2011	New application note.
*A	3243316	ZSK	04/26/2011	Updated figure 4 and figure 6
*B	3338089	ZSK	08/11/2011	Added Figure 6, Table 1 and Table 2. Contents update.
*C	3752264	ZSK	09/21/2012	Contents rephrased. No change in any figures, tables or technical details. Applied new application note format.
*D	4047632	ZSK	07/02/2013	Obsolete the application note AN68173. Reason: SPI nvSRAM was developed primarily to compete against Ramtron's DPI F-RAM product offering. With the acquisition of Ramtron's Serial F-RAM portfolio, there is now an overlap of Serial (SPI and I^2C) non-volatile memory technologies (nvSRAM and F-RAM) Cypress offers to customers. Hence, we need to consolidate the NVP portfolio and position our offering appropriately. NVP PSP 2014 also captures this product positioning as our most immediate initiative, as stated in the horizon map Strategy 1: "*Sharpen positioning of nvSRAM as the fastest and FRAM as the lowest-energy nonvolatile RAMs*". (Ref: TUP#258)

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