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# THIS SPEC IS OBSOLETE

Spec No: 001-66311

Spec Title: TIMING RECOMMENDATIONS FOR BYTE ENABLES AND CHIP ENABLES IN MOBL(R) SRAMS - AN66311

Sunset Owner: Anuj Chakrapani (AJU)

Replaced by: NONE

COMMENT: The issue described in the rest of this document has been fixed, and devices with this fix are in production. The table below shows the date code marking on the devices that contain the fix. The first two digits represent the year, and the next two represent the workweek. For example, 1301 refers to the first week of year 2013. Devices with workweek on or after 1301 (like 1303, 1306 etc) contain the fix.
To know if you are affected by this issue, please feel free to create a Technical Support case on the website (www.cypress.com/support)

| **Device** | **Fixed device from date code starting** |
|---|---|
| 2 Mbit<br>(CY62136ESL, CY62136EV30, CY62136FV30, CY62137EV30, CY62137FV18, CY62137FV30, CY62138EV30, CY62138FV30, CY62138F) | 1301 |
| 4 Mbit<br>(CY62146E, CY62146ESL, CY62146EV30, CY62147EV30, CY62148ESL, CY62148EV30, CY62148E, CY62147EV18) | 1301 |
| 8 Mbit<br>(CY62157EV30, CY62157ESL, CY62157EV18, CY62157E, CY62158E, CY62158EV30) | 1301 |
| 16 Mbit<br>(CY62167E, CY62167EV18, CY62167EV30, CY62168EV30) | 1301 |
| 32 Mbit<br>(CY62177EV30, CY62177ESL) | 1301 |
| 64 Mbit<br>(CY62187EV30) | 1445 |

# Timing Recommendations for Byte Enables and Chip Enables in MoBL® SRAMs

**Author: Anuj Chakrapani**
**Associated Project: No**
**Associated Part Family: CY62136ESL, CY62136EV30, CY62136FV30, CY62137EV30, CY62137FV18, CY62137FV30, CY62138EV30, CY62138FV30, CY62138F, CY62146E, CY62146ESL, CY62146EV30, CY62147EV30, CY62148ESL, CY62148EV30, CY62148E, CY62147EV18, CY62157EV30, CY62157ESL, CY62157EV18, CY62157E, CY62158E, CY62158EV30, CY62167E, CY62167EV18, CY62167EV30, CY62168EV30, CY62177EV30, CY62177ESL, CY62187EV30**
**Related Application Notes: None**




## Abstract

AN66311 provides timing recommendations for the use of byte enable pins ( $\overline{BHE}$ and $\overline{BLE}$ ) and chip enables (single or dual, as applicable) in select Cypress MoBL® SRAMs. However, the issue responsible for the recommendations provided in this document has been fixed. Hence, Cypress devices with newer date code do not require you to implement these timing recommendations in your design. The nature of this fix is transparent to a user. If you were unaffected by this issue earlier, the fix will not affect you either. This fix does not affect any of the datasheet parameters or functionality of the devices.

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## Introduction

Cypress's 90-nm MoBL® SRAMs have best-in-class standby power. Their low standby currents ($I_{SB}$) make them ideal for use in low-power battery-operated applications.

This application note discusses certain timing recommendations that you must consider when designing in these SRAMs. The first section of this document provides timing recommendations related to byte enables and is applicable to the following parts:

- 2-Mbit (CY62137EV30, CY62137FV30, CY62137FV18)
- 4-Mbit (CY62147EV30, CY62147EV18)
- 8-Mbit (CY62157EV30, CY62157ESL, CY62157EV18, CY62157E)
- 16-Mbit (CY62167EV30, CY62167EV18, CY62167E)
- 32-Mbit (CY62177EV30, CY62177ESL)
- 64-Mbit (CY62187EV30)

These SRAMs have a byte power-down feature, which means that if the byte enable pins ( $\overline{BHE}$ and $\overline{BLE}$ ), used to control the I/Os) are disabled, the device switches to standby mode, regardless of the state of the chip enable pins ( $\overline{CE}$ , $\overline{CE}_1$, or $CE_2$). This feature creates significant power savings for the application because the device switches seamlessly from active mode to standby mode and vice versa.

The second section of this document provides timing recommendations related to chip enables and is applicable to the following parts:

- 2-Mbit (CY62136ESL, CY62136EV30, CY62136FV30, CY62137EV30, CY62137FV18, CY62137FV30, CY62138EV30, CY62138FV30, CY62138F)
- 4-Mbit (CY62146E, CY62146ESL, CY62146EV30, CY62147EV30, CY62148ESL, CY62148EV30, CY62148E, CY62147EV18)
- 8-Mbit (CY62157EV30, CY62157ESL, CY62157EV18, CY62157E, CY62158E, CY62158EV30)
- 16-Mbit (CY62167E, CY62167EV18, CY62167EV30, CY62168EV30)
- 32-Mbit (CY62177EV30, CY62177ESL)
- 64-Mbit (CY62187EV30)

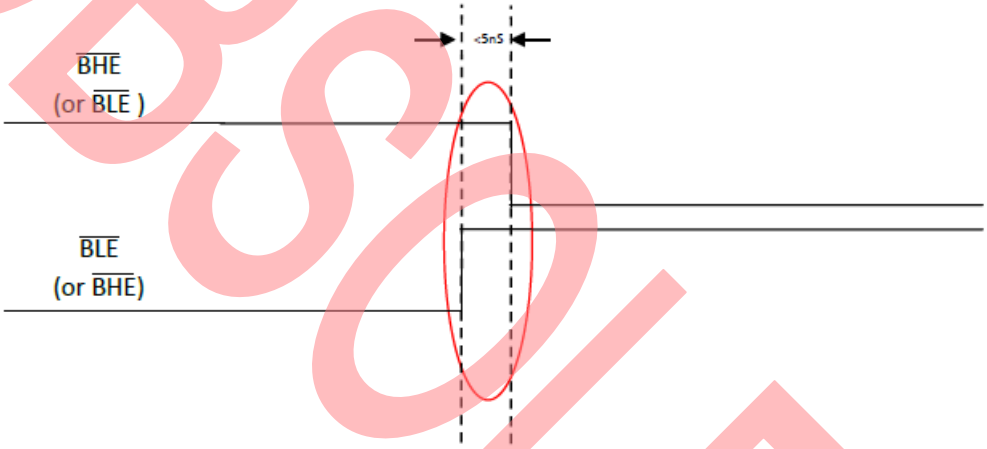
# Overview

## Byte Enables ( $\overline{\text{BHE}}$ / $\overline{\text{BLE}}$ ) Timing Recommendation

During normal device operation, you should avoid a skew of less than 5 ns between the byte enable pins ( $\overline{\text{BHE}}$ with reference to $\overline{\text{BLE}}$, or vice versa) when switching in the opposite direction.

This condition on the byte enable pins is illustrated in Figure 1.

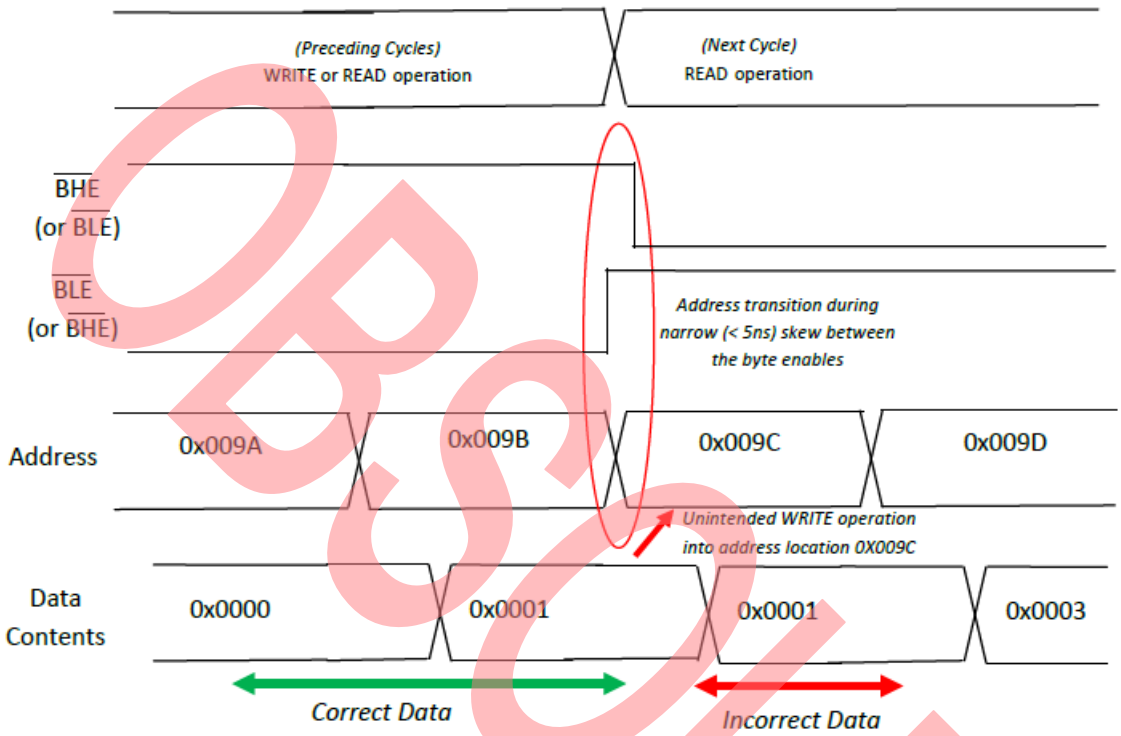
Figure 1. Narrow (< 5 ns) Skew between Byte Enables




If the condition (shown in) on the byte enable pins $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ is unavoidable, Cypress recommends that you not switch the Address lines in the vicinity (–5 ns to +15 ns window) of the byte enable signals.

Figure 2 illustrates a condition in which the SRAM address lines are switched in the vicinity (–5 ns to +15 ns window) of the switching of the byte enables $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$. When this happens, the data held in the previous location may be written into the new location being accessed, even though the device is not in a WRITE mode. Thus, the contents of the new location may be corrupted internally.

Figure 2. Example of Unintended Data Corruption when Address Lines are Switched in the Vicinity of Narrow (< 5 ns) Skew between Byte Enables




**Note** In this example, expected data: (0x009A) = 0x0000; (0x009B) = 0x0001; (0x009C) = 0x0002; (0x009D) = 0x0003

This is only an issue when the Address lines switch in the vicinity (–5 ns to +15 ns window) of a narrow (< 5 ns) skew between the byte enables. If either condition does not occur (that is, if there is no skew < 5 ns between the byte enables or if the Address lines do not switch in the vicinity of the narrow skew), there is no unintended data corruption. Therefore, if the narrow skew between byte enables is unavoidable in the application, it is strongly recommended that you avoid switching the Address lines in the vicinity of the skew. Examples are shown in Figure 3 and Figure 4.

Figure 3. Timing Diagram showing Recommended Address Transition before Narrow (< 5 ns) Skew between Byte Enables

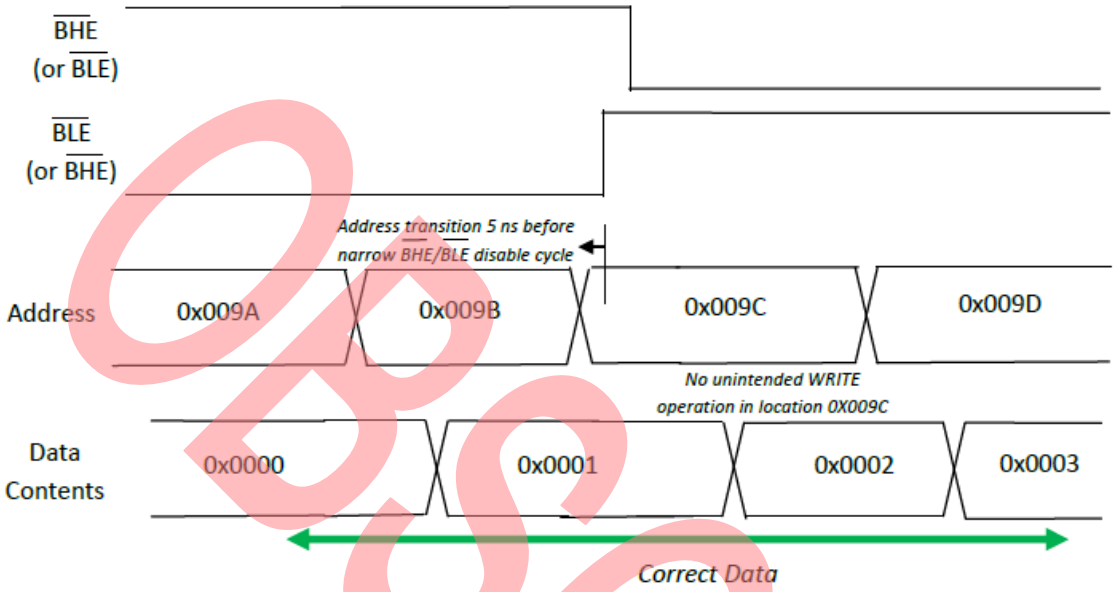
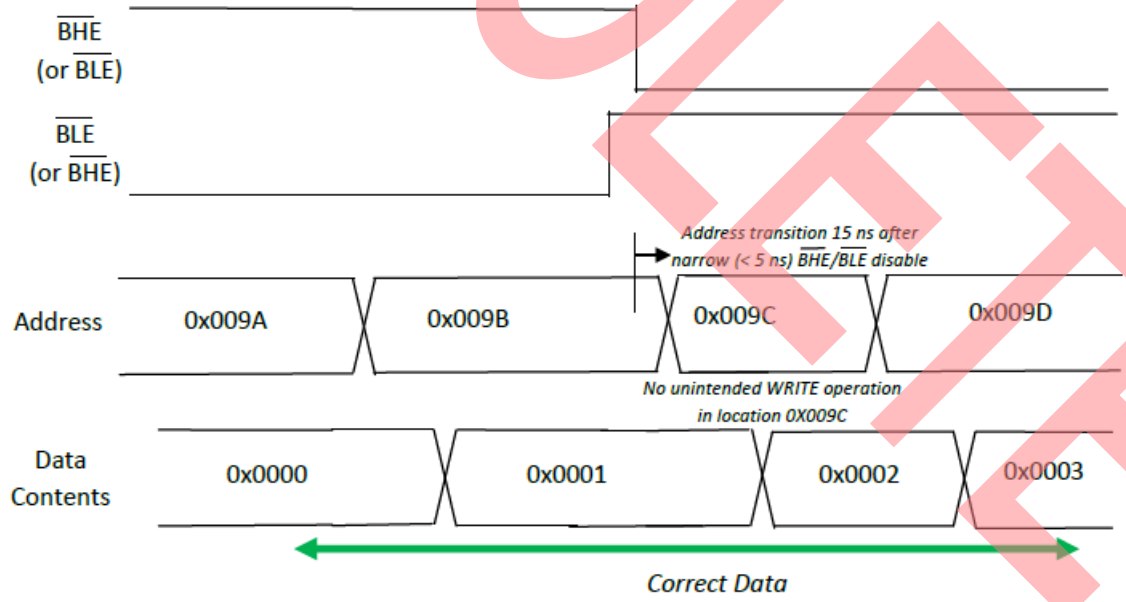



Figure 4. Timing Diagram showing Recommended Address Transition after Narrow (< 5 ns) Skew between Byte Enables



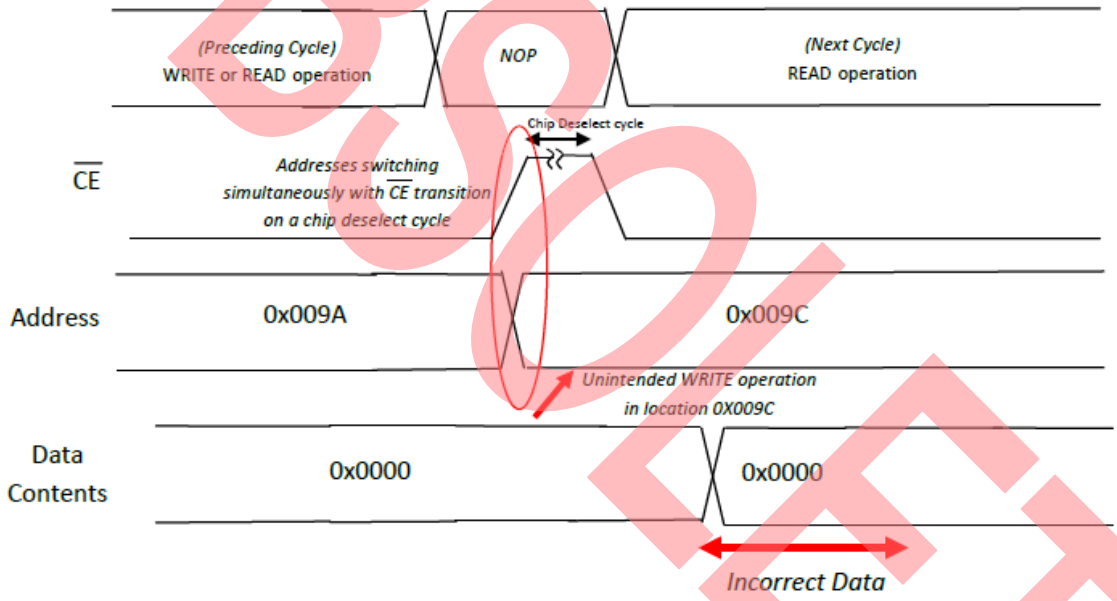
## Chip Enable ( $\overline{CE}$ , $\overline{CE}_1$, $CE_2$) Timing Recommendation

The scenario of unintended data corruption may also arise in a very specific application condition in which Address lines switch simultaneously with Chip Enables ( $\overline{CE}$ , $\overline{CE}_1$, or $CE_2$, as the case may be) when the latter initiates a chip deselect cycle.

Switching either of these lines (Address lines and Chip Enable lines) simultaneously could result in the new address location being selected before the internal data lines are cleared (in preparation for the operation). This could, in turn, cause an unintended WRITE operation into the new location. The effect is shown in Figure 5.

A suggested workaround (shown in Figure 6) is to avoid simultaneous switching of Address and Chip Enable signals when entering a chip deselect cycle by skewing either the Address lines or the Chip Enable signals by 3 ns. If any of these trigger conditions do not occur, you will not need this workaround because data is not corrupted.

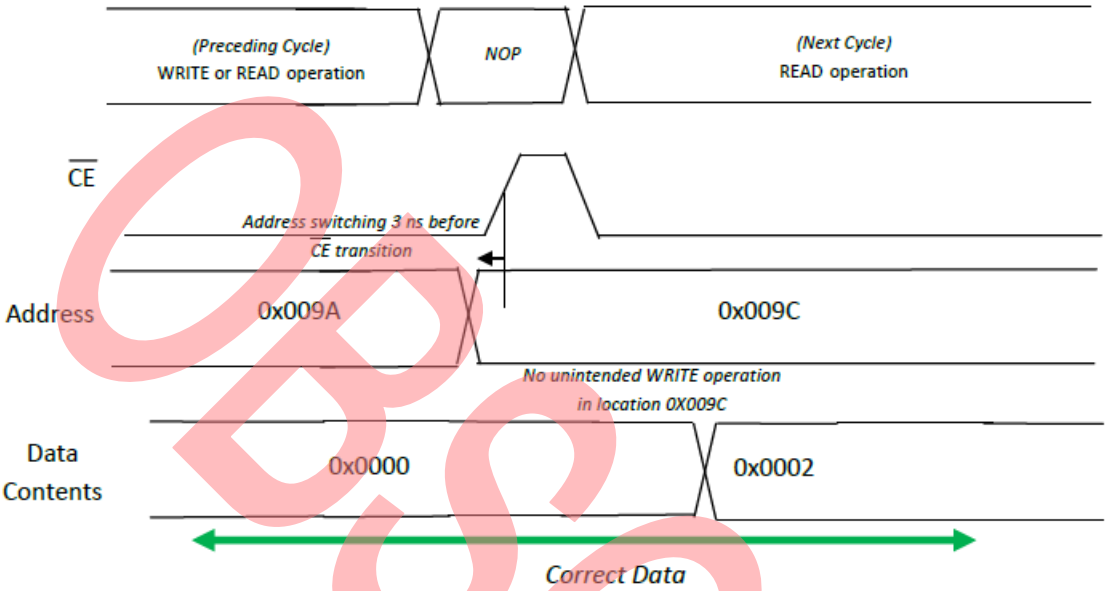
Figure 5. Example of Unintended Data Corruption when Address Lines are switched in the Vicinity of Chip Deselect Initiation




**Notes**

1. In the example above, expected data: (0x009A) = 0x0000; (0x009C) = 0x0002
2. NOP means that the SRAM is externally neither in a WRITE mode, nor in a READ mode.
3. The $\overline{CE}$ illustration in Figure 5 also applies to active low $\overline{CE}_1$ and active high $CE_2$ for dual chip enable devices.

Figure 6. Timing Diagram showing Recommended Address Transition 3 ns before Chip Deselect Initiation






**Notes**

1. NOP means that the SRAM is externally neither in a WRITE mode, nor in a READ mode.
2. The $\overline{CE}$ illustration in Figure 6 also applies to active low $\overline{CE}_1$ and active high $CE_2$ for dual chip enable devices.

## Summary

Under the conditions discussed in this application note, the above timing considerations can be made to avoid data corruption. If the input conditions are not as described, you do not need to consider these recommendations.

## About the Author


| | |
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## Document History

Document Title: Timing Recommendations for Byte Enables and Chip Enables in MoBL® SRAMs - AN66311

Document Number: 001-66311

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 3132892 | AJU | 01/10/2011 | New application note. |
| *A | 3289141 | AJU | 06/21/2011 | Updated application note with Chip Enable related information. |
| *B | 3338018 | AJU | 08/05/2011 | Updated Abstract.<br>Updated the sections Byte Enables ( $\overline{BHE}$ / $\overline{BLE}$ ) Timing Recommendation and Chip Enable ( $\overline{CE}$ , $\overline{CE}_1$, $CE_2$) Timing Recommendation under the main section Overview. |
| *C | 3723119 | AJU | 09/03/2012 | Updated all the figures in this application note.<br>Updated in new template. |
| *D | 3940344 | NILE | 03/21/2013 | Major rewrite of Abstract. |
| *E | 4054177 | AJU | 07/24/2013 | Removed references to 1Mbit SRAM devices<br>Obsolete application note. |

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