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Spec No: 001-64285

Spec Title: AN64285 - WIRELESSUSB(TM) NL LOW POWER RADIO RECOMMENDED USAGE AND PCB LAYOUT

Replaced by: NONE

Wirelessusb™ NL Low Power Radio Recommended Usage and PCB Layout

Associated Project: Yes
Associated Part Family: CYRF8935
Software Version: NA
Related Application Notes: None

To get the latest version of this application note, or the associated project file, please visit http://www.cypress.com/go/AN64285.

Wireless products are now found in abundance, all around us today, and their usage continues to rapidly expand. This application note introduces the Cypress CYRF8935 device and a sample PCB design. The appendix section guides you on antenna selection process.

Contents

Introduction

This note describes the NL RF module reference design, based on the CYRF8935 device. Various antenna choices are introduced, enabling designers to easily add 2.4 GHz wireless linking to a product.

Files List

The following PC files accompany this application note.

File Name	Contents
001-64285.pdf	This file.
NL_Altium.zip	Altium schematic and PCB layout.
NL_OrCAD.zip	OrCAD schematic of module, OrCAD reference design.
Antennas.zip	Documents for various antennas discussed.

Understanding the Schematic

The schematic has four (4) basic categories of circuitry: DC Power, MCU interface, Crystal Oscillator, and RF/Antenna Connection.

DC Power

Refer to pins 1, 2, 5, 8, 9, 19, and 22 of the device, on the schematic.

The CYRF8935 features an on-chip low dropout (LDO) regulator that is optimized for the analog mixed signal (AMS) and radio frequency (RF) needs of the device. The LDO regulator input pin, V_{IN}, connects to input power, while the output pin, V_{OUT}, connects to each of the V_{DD} pins of the device, as shown in the schematic.

It is recommended that V_{DD} bypass capacitors be placed approximately at the corners of the chip. See the sample layout shown in the figures.

Note that if the source of DC input power is from a switching power converter that may have high noise, additional DC filtering may be needed. Schematic note 3 details this, and provides initial guidance.

Note that a separate V_{DD_IO} pin is provided. Internal to the CYRF8935 device, this voltage drives the MCU interface I/O pads. In other words, voltage on this pin sets the expected I/O voltages. It normally connects to the same voltage source as the MCU.

MCU Interface

SPI: Refer to pins 13, 15, 16, and 17 of the device, on the schematic. The primary MCU interface is a conventional 4-wire SPI.

IRQ: Refer to pins 10 and 14 of the device, on the schematic. The CYRF8935 can generate two IRQ signals for the MCU. Most applications will only need the PKT IRQ output. PKT is used to inform the MCU that a packet is ready to be received, or a packet has been transmitted. FIFO is an IRQ that indicates the internal FIFO is running high (for Rx), or low (for Rx), and may need imminent read or write by the MCU.

In addition, the CYRF8935 expects a reset signal to initialize the device. This signal derives from a dedicated GPIO.

Crystal Oscillator

Refer to pins 23 and 24 of the device, on the schematic.

A good quality, low-cost external quartz crystal element is used as the frequency standard for the RF transceiver. For error free data transmission and reception, the oscillation must be free of excess phase noise and jitter. Circuit operation is explained in the CYRF8935 datasheet. Appropriate crystal loading capacitors must also be supplied as detailed in the datasheet.

Correct crystal loading is checked by measuring the frequency on BRCLK, pin 18. At power-up, it should measure 3.000,00 MHz; within approximately 10 ppm to 20 ppm error (It is better if the frequency error is at the least). Frequency on BRCLK is only accessible on bare die parts. For packaged parts, crystal loading is checked by measuring transmit carrier frequency; see datasheet for instructions. Under room temperature, nominal test conditions, frequency error should measure no more than 10 to 20 ppm. See datasheet for more in-depth detail regarding crystal specifications.

For proper startup, it is normally the Rs specification that is most important. See datasheet for maximum Rs specification for the crystal.

RF/Antenna Connection

Refer to pins 3 and 4 of the device, on the schematic. The shunt capacitor and series inductor serve to improve the impedance match between device and antenna. The values shown should not be modified. When selecting these components, choose parts that have low loss at RF. The chosen parts should exhibit a minimum Q of approximately 20 or better, at 2.4 GHz.

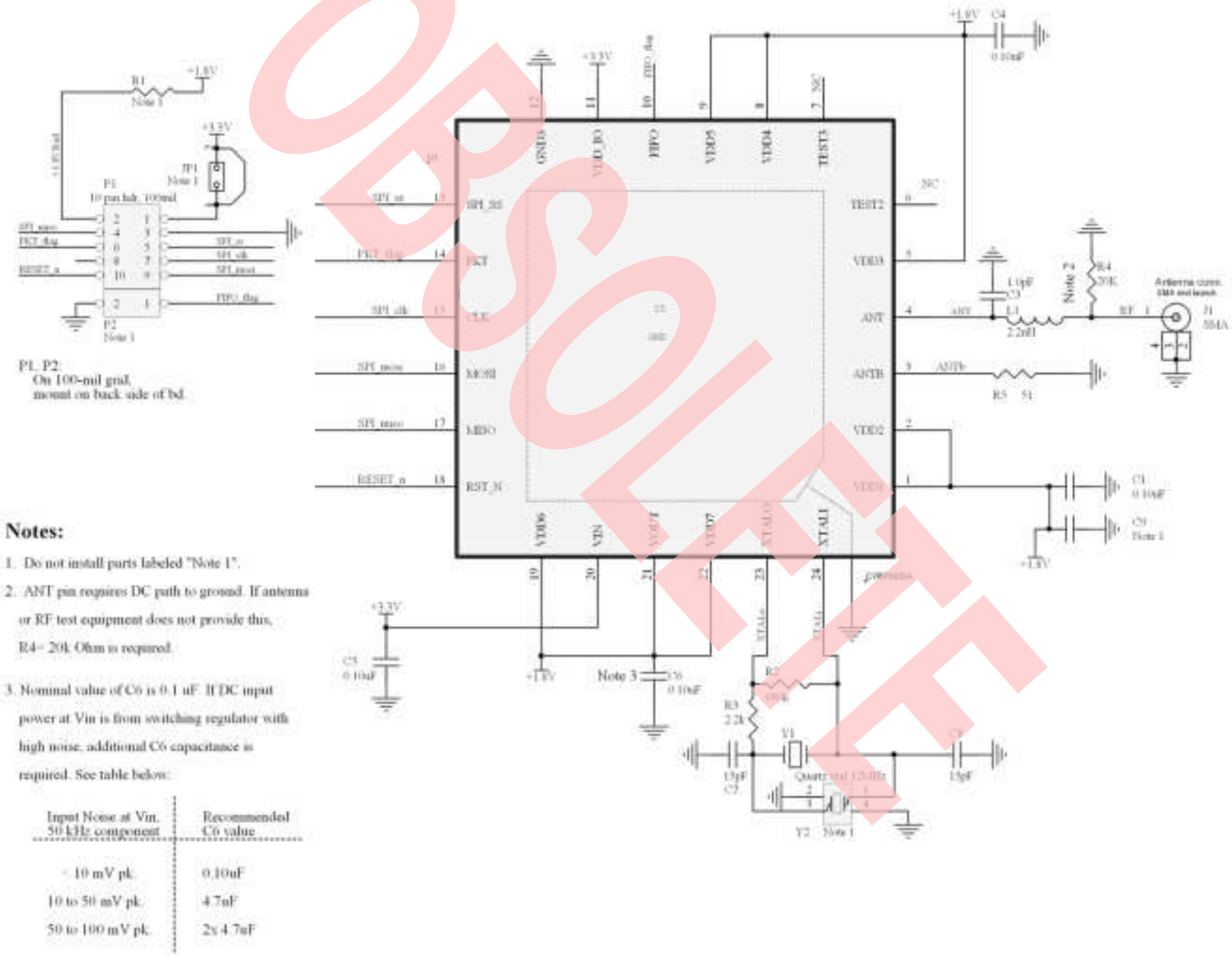
For EMC compliance testing, direct coaxial cable connection to the RF lab equipment is often helpful, as shown by the SMA connector in this reference design. Without the direct coaxial cable connection, a shielded and calibrated TEM cell test box may be necessary for some of the regulatory and EMC compliance testing.

Note

See http://www.temcell.com/ and http://www.rfshieldbox.com/products.html

Schematic Diagram

Figure 1. Schematic Diagram for the PCB



PCB Layout Notes

Following are the general guidelines to be observed as a matter of good design practice.

Highly important items are underlined, and their application is illustrated on the layout figures.

- RF layout guidelines
  - Solid RF ground plane between RFIC and Antenna.
  - Use ground vias liberally
  - Keep RF traces short for low-loss
- Crystal layout guidelines
  - Minimal ground noise on the crystal load capacitors
  - Ground via for each capacitor
  - Ground the crystal case if possible
  - Keep some separation between XTALi and XTALo. Grounds fill between the crystal leads.
- Miscellaneous layout guidelines
  - Ground vias under or at critical components
    a. RFIC
    b. Crystal
    c. Decoupling capacitors
    d. RF transmission line

Figure 2. Top view of PWB. Top layer of PWB (red)

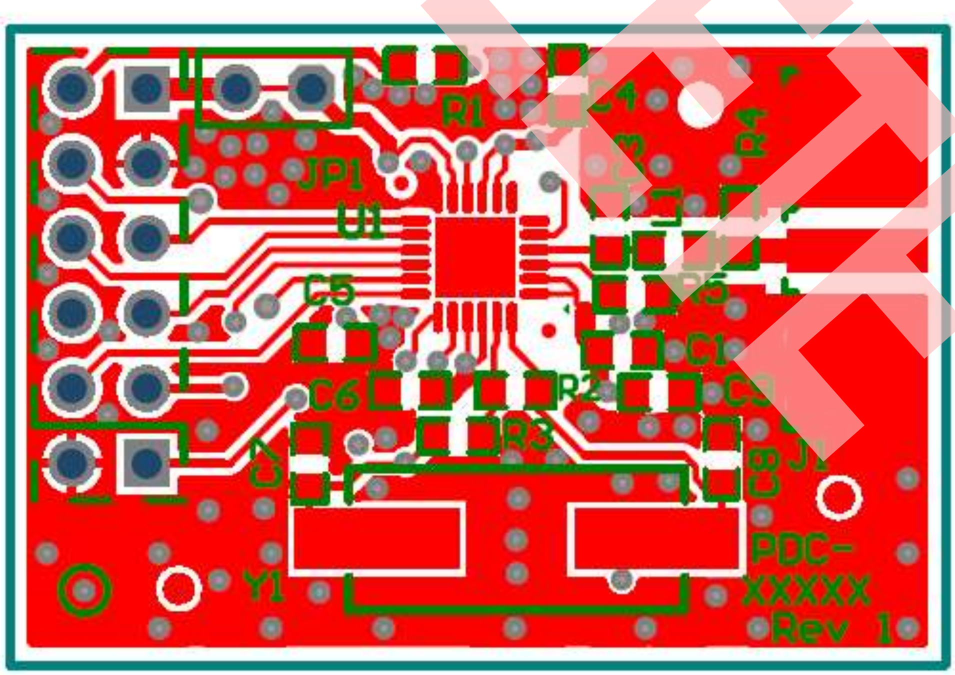
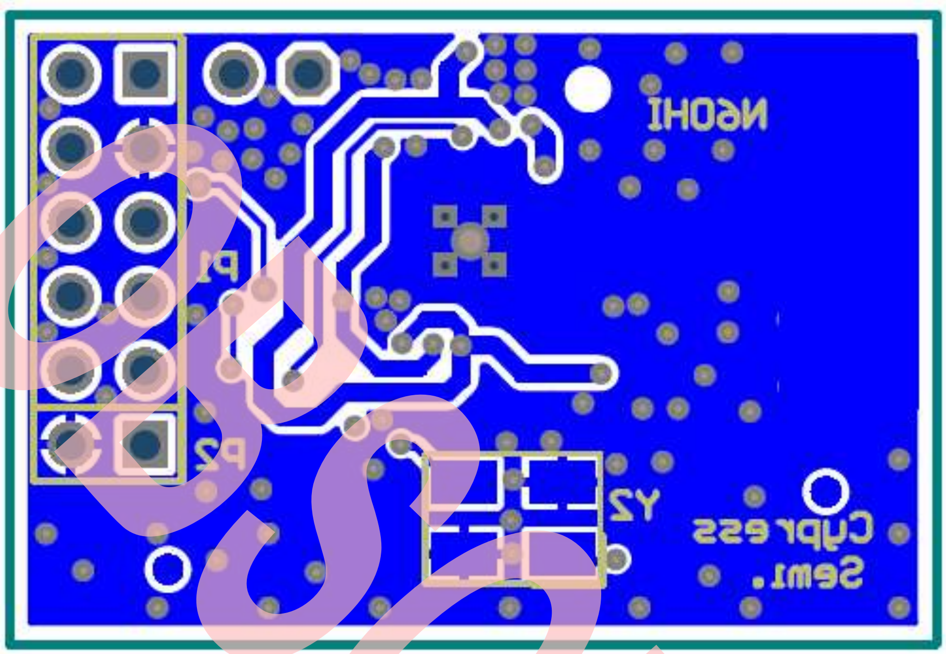


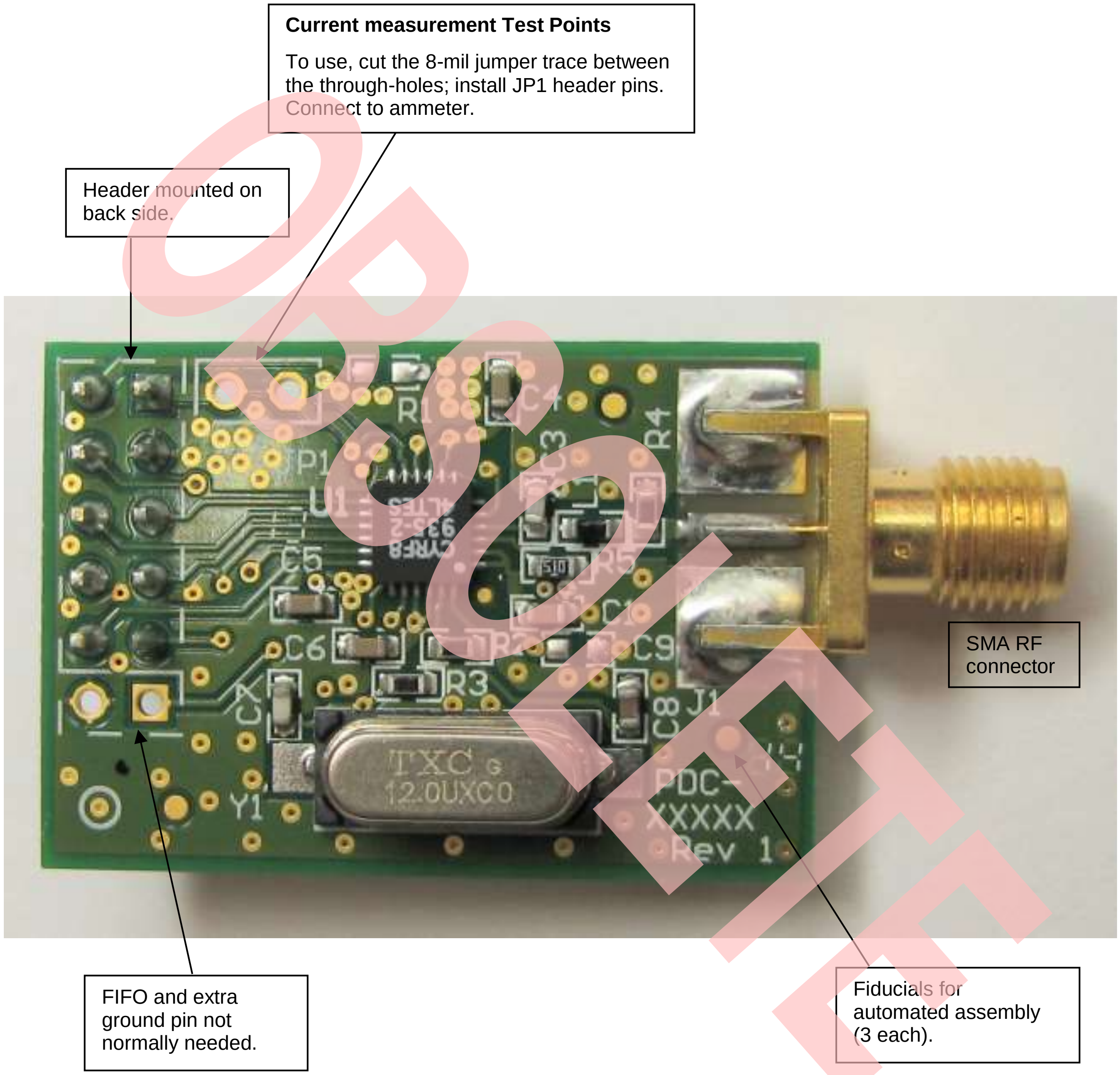
Figure 3. Top view of PWB, looking through the top layer to view the bottom layer of PWB (blue)



Overall dimensions:

1250 x 850 Mils

Figure 4. Completed PCB Assembly



Bill of Materials

Qty	Part Type	Designator	Footprint
1	1.0pF	C3	0603
2	15pF	C7 C8	0603
4	0.10uF	C1 C4 C5	0603
		C6 (see sch. note)	
1	680 k	R2	0603
1	2.2 k	R3	0603
1	20 k	R4	0603
1	51	R5	0603
1	2.2nH	L1	0603
1	SMA-Female	J1	SMA_LAUNCH
1	10-pin hdr, 100-mil	P1	HDR2X5
1	CYRF8935	U1	QFN24
1	Quartz xtal 12 MHz	Y1	XTL_49SS

Not used:

Qty	Part Type	Designator	Footprint
2	Note 1	C9 R1	0603
2	Note 1	JP1 P2	HDR1X2
1	Note 1	Y2	XTL_4X2.5

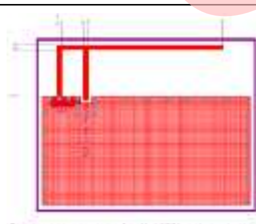
Note 1 Do not install parts labeled “Note 1”.

Appendix A – Antenna Recommendations

The antenna is normally the biggest factor in achieving successful performance. A rigorous antenna tutorial is beyond the scope of this paper, but some simple antenna recommendations that can be easily applied to CYRF8935 applications are introduced.

Virtually any type of good-quality 50 ohms, 2.4 GHz antenna can be used with the CYRF8935. Several choices are shown in Table 1.

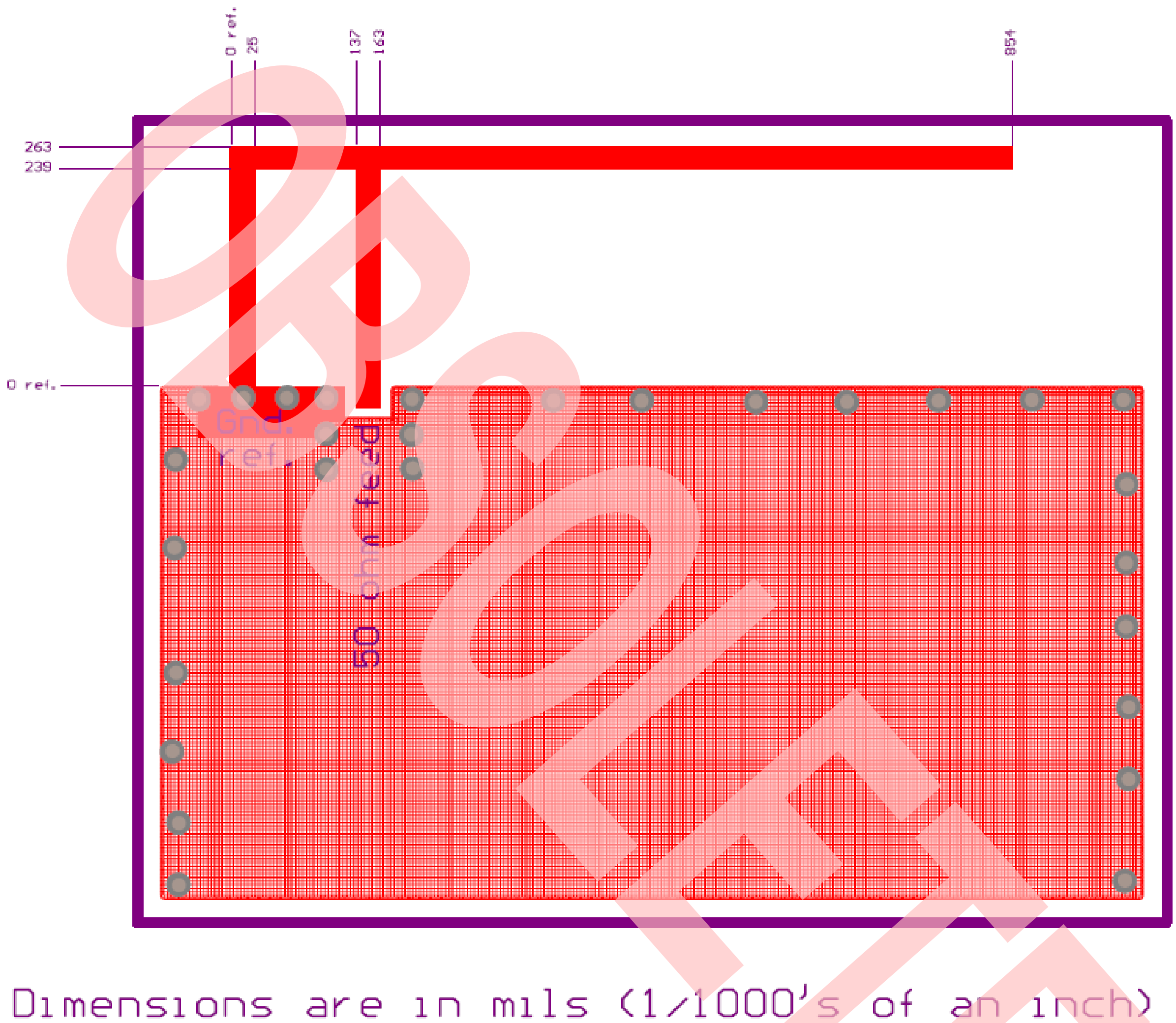
Table 1. Antenna Choices

Antenna type	Picture or Drawing	DC Grounded? See sch. Note 2	Description/Notes
Wiggle antenna		Yes	Described in Cypress Semiconductor AN48610 (Doc. no. 001-48610) Cost: Almost free of cost when added to existing PCB.
Custom printed-trace antenna	This is a specialized antenna, customized to each application.	Depends on the design	Cost: Almost free of cost when added to existing PCB.
Chip antenna	 Model 2450AT18B100E, Johanson Technology Inc.	No	Easy to use. Ensure to read the datasheet and follow all manufacturer instructions. Manufacturer's specification for mounting and layout must be exactly followed. Cost: Can be expensive.
PIFA		Yes	The Printed Inverted-F Antenna (PIFA). Cost: Almost free of cost when added to existing PCB. See Appendix B – PIFA Dimensions for detailed drawing.
1/2 wave end-fed dipole	 Illustrated: Model W1010, by Pulse.	No	Delivers 'textbook' 0 dBd performance. Easy removal and replacement. Accommodates EMC compliance and end applications. Requires RF connect on the board. Cost: Relatively expensive.

Antenna designs with inherent DC grounding are generally preferred over non-DC grounded designs. Grounded designs have inherently better ESD immunity, and the need for the 20 K resistor on CYRF8935 ANT pin is eliminated.

Appendix B – PIFA Dimensions

For 2.4 GHz. Substrate material is 1/32 inch (0.031) FR-4. Note that ideal dimensions may vary slightly, depending on application.



Document History

Document Title: AN64285 - WirelessUSB™ NL Low Power Radio Recommended Usage and PCB Layout

Document Number: 001-64285

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3037038	HEMP	09/23/2010	New Application Note.
*A	3349669	HEMP	09/13/2011	Content updated to QFN-24.
*B	4542074	CSAI	10/17/2014	Updated to new template. Completing Sunset Review.
*C	5810239	AESATMP8	07/11/2017	Updated logo and Copyright.
*D	5930488	ANKC	10/16/2017	Obsoleting the spec

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