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Spec No: 001-62914

Spec Title: AN62914 - PROGRAMMING FLEXO(TM) LOW NOISE CLOCK GENERATORS

Replaced by: None

AN62914

Programming FleXO™ Low Noise Clock Generators

Author: Kelly Mass, Brijesh A Shah
Associated Project: No
Associated Part Family: CY2X013, CY2X014, CY2XF23/24, CY2XF32/33/34
Software Version: CyClockWizard 1.0
Related Application Notes: Frequency Margining using FleXO and Its Applications

FleXO™ is a family of low phase noise clock generators and oscillators, consisting of both fixed frequency devices and programmable devices. This application note fully explains the software and hardware tools available for FleXO, and the process of programming devices for applications that are not supported by the off-the-shelf fixed frequency devices.

Contents

1 Introduction

FleXO is a family of high performance (low phase noise) single output clock generators and oscillators. Fixed frequency devices are available off the shelf for common frequencies. Programmable devices are offered to support applications that are not covered by the fixed frequency offerings. Available output standards are LVPECL, LVDS and CMOS.

Programmability means that these devices can be configured to almost any frequency between 8 MHz and 690 MHz. They can also be optimized for minimum phase noise over a user specified range of offset frequencies.

This application note collects in one place all of the information necessary to enable a user to select device, generate configuration and program FleXO devices.

2 FleXO Product Overview

The FleXO family consists of several device types. They all feature low phase noise and jitter, and have a single output.

2.1 FleXO Product Types

The two basic categories of FleXO devices are oscillators and clock generators.

- **Oscillator**: Uses an internal crystal
- **Clock generator**: Uses an external clock source – either a crystal or a 1.8 V clock

Additional features are available which distinguish certain devices from ordinary oscillators and generators.

- **Frequency margining**: Output frequency switching – either pin controlled or I^2C controlled. Also known as frequency select.
- Voltage controlled oscillator (VCXO) / clock generator

Table 1 and Table 2 summarize the FleXO device types and part numbers.

Table 1. FleXO Crystal Oscillator Products

Part Number	Function	Output	Package	Programmable
CY2X013	Crystal oscillator (XO)	LVDS	6-ld LCC 5 x 3.2 mm	Supports Factory and Field Programmability
CY2X014	Crystal oscillator (XO)	[LVPECL		
CY2XF23 [1]	Crystal oscillator with frequency margining, I^2C controlled	LVDS		
CY2XF24 [1]	Crystal oscillator with frequency margining, I^2C controlled	LVPECL		
CY2XF32	Crystal oscillator with frequency margining, pin select	CMOS		
CY2XF33	Crystal oscillator with frequency margining, pin select	LVDS		
CY2XF34	Crystal oscillator with frequency margining, pin select	LVPECL		

Note: 1. I^2C is used to write in volatile memory to change the output frequency.

Table 2. Fixed Frequency FleXO Clock Generator Products

Part Number	Function	Output	Package
CY2XLnn [2]	Clock generator	LVDS	8-pin TSSOP
CY2XPnn [2]	Clock generator	LVPECL	8-pin TSSOP
CY2VCnnn [2]	Voltage controlled clock generator	LVPECL	16-pin TSSOP

Note: 2. Rather than listing all available individual part numbers, this table lists “family” part numbers. The characters “nn” and “nnn” are place holders for numeric values which define particular devices.

2.2 Explaining Factory and Field Programmable Devices

Some FleXO devices, such as the CY2XP31 and CY2XL11, are fully pre-programmed for a particular frequency or set of frequencies. No field programming is required. Currently, all clock generator products are factory programmed and are not offered as field programmable devices. The frequencies are found in Appendix A and the individual datasheets. To request clock generator products with different frequencies, please contact your local Cypress salesperson.

The crystal oscillator products are also offered as factory programmed parts to support common frequencies. For all other frequencies, field programmable devices are available.

Field programmable devices have an internal one time programmable (OTP) memory which controls device functions such as output frequency and control pin functionality. This internal memory is not configured when the devices are shipped, and they must be programmed on a device programmer before being installed on a board. This permits you to define parts to suit your exact needs. This flexibility is particularly important for the frequency select devices, where few customers share the same requirements. Field programmable devices are the key topics of this application note.

Until it is programmed, a field programmable device's behavior is undefined. After it is programmed, it always powers on to the same configuration. They are not suitable to in-system programming and must be programmed prior to installation on a board. I2C can be used to write in volatile memory of device to change output frequency. Data written via I2C will last till next power down of device. For details on output frequency change using I2C, please refer Application Note "Frequency Margining using FleXO and Its Applications – AN52133".

2.3 Key FleXO Parameters

The following table summarizes some of FleXO's key operating parameters.

Table 3. Key FleXO Parameters

Parameter	Range
V_{DD}	2.5 V or 3.3 V
Number of outputs	1
Number of pin selectable output frequencies, CY2XF32 / 33 / 34	4
Number of I^2C configurable output frequencies, CY2XF23 / 24	Unlimited
Output Standards	LVPECL, LVDS, CMOS
Output frequency, LVPECL & LVDS	50–521 MHz, 529–596 MHz, 617–690 MHz
Output frequency, CMOS	8–200 MHz
Reference crystal	20–30 MHz
External input reference (1.8 V only)	15–40 MHz
Frequency synthesis resolution	< 0.1 ppm
Temperature range	0 to 70 ºC, –40 to +85 ºC
Oscillator frequency tolerance, commercial temperature	±35 ppm
Oscillator frequency tolerance, industrial temperature	±55 ppm
VCXO pull range	Up to ±115 ppm
Output control	Output enable, power down
Packages	6-pin LCC, 8-pin TSSOP, 16-pin TSSOP

3 FleXO Programming Tools

The following sections describe the Cypress software and hardware that are needed to program a field programmable FleXO clock. Third party support is also described.

3.1 Software

CyClockWizard is the latest software tool for Cypress clock products, and includes the following functionality:

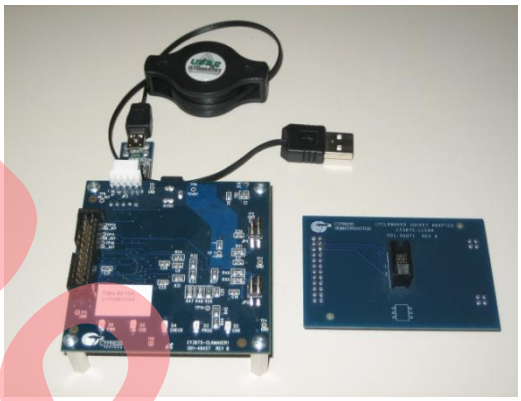
- Parametric device search
- Generate device configuration JEDEC file
- Programming using CY3675 Kit

CyClockWizard is the only software tool needed to generate configuration JEDEC and program FleXO devices. It is free and downloadable from following link: CyClockWizard 1.0.

3.2 Hardware

Cypress offers the CY3675 kit for programming FleXO devices. There are two parts to the programmer. The base unit – or motherboard – is the CY3675-CLKMAKER1. It is the larger board seen in Figure 1. This board contains all of the programming electronics, and also the USB communication interface. The appropriate socket adapter must be installed onto the base unit. The CY3675-LCC6A socket is available to support FleXO oscillator devices.

Figure 1. CY3675-CLKMAKER1 and CY3675-LCC6A



The CY3675-CLKMAKER1 and associated CY3675 adapter boards can be purchased online from the Cypress Store: CY3675-CLKMAKER1 CyClockMaker Clock Programming Kit.

3.3 Third Party Programmers

BP Micro offers programming support for many Cypress products, including FleXO. Their socket module ASML06LCC supports the FleXO oscillator devices in the 6-lead LCC package. This socket module works with a wide range of BP Micro programmers.

The list of Third party programmers for Cypress clocks is available on following link: Third-Party Programmer List

4 Programming Flow

Programming a FleXO device is a two step process. Both steps use the CyClockWizard software. First, the device parameters are entered and a JEDEC programming file is generated. The second step uses this programming file and the CY3675 programmer to program the device.

The demonstration of Generating configuration JEDEC file and programming FleXO device is shown in Video available at following link: Programming FleXO Low Noise Clock Generator

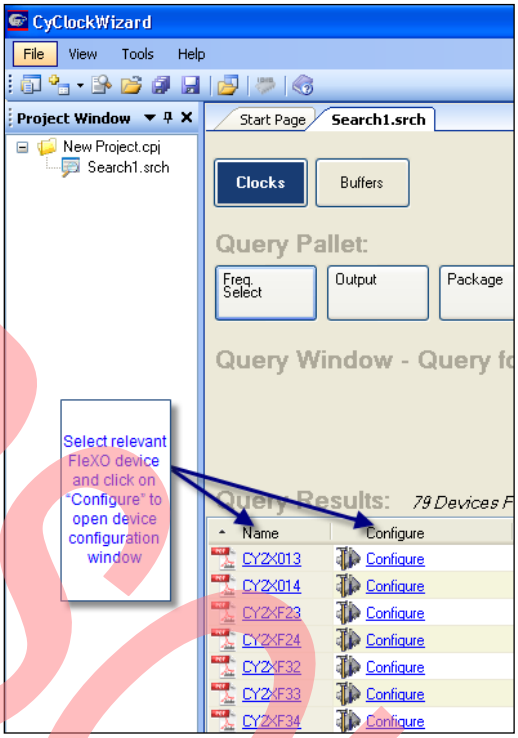
The following sections describe these two steps in detail.

4.1 Generate Configuration JEDEC File:

To generate JEDEC file for specific Application, user should pursue following steps. These steps are shown in Video.

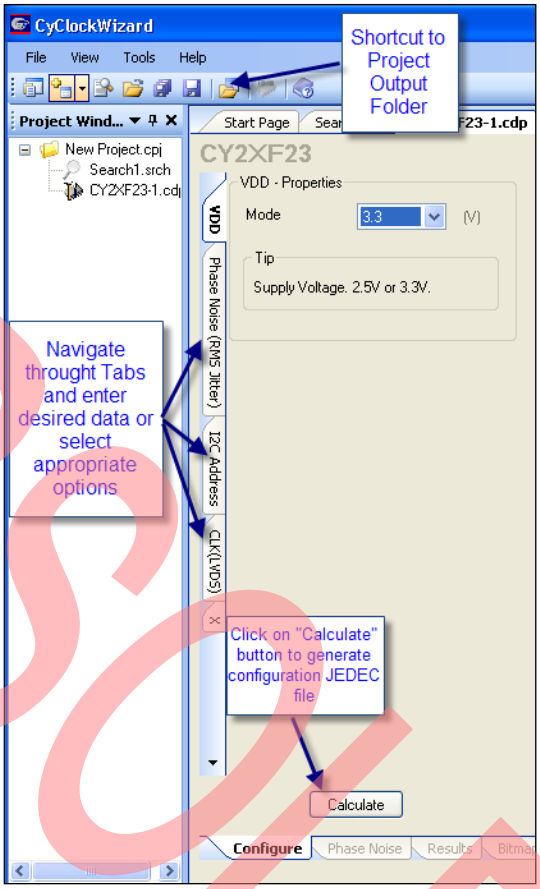
1. Install CyClockWizard 1.0 Software
2. Create New Project in CyClockWizard
3. Browse relevant FleXO device in Column “Name” and click on “Configure” to open device configuration window (shown in Figure 2)

Figure 2. Select Device and Open Configuration Window



4. Navigate to different Tabs and enter desired data or select appropriate options For example
   - Enter data in VDD, I2C Address, Phase Noise and CLK Tabs for Frequency margining device with I2C (shown in Figure 3)
   - Enter data in VDD, FSx, Phase Noise and CLK Tabs for Frequency margining device with Pin (shown in Figure 4)

Figure 3. Parameters Tabs for Frequency Margining Device with I2C



5. Click on “Calculate” button to generate configuration JEDEC file(shown in Figure 4).
6. Different options of Phase Noise plots will appear, select desired one and JEDEC file will get updated accordingly(shown in Figure 5)
7. Configuration JEDEC file is generated and saved in output folder of project. The shortcut to open project output folder is given in CyClockWizard menu bar(shown in Figure 3.

Figure 4. Parameters Tabs for Frequency Margining Device with Pin

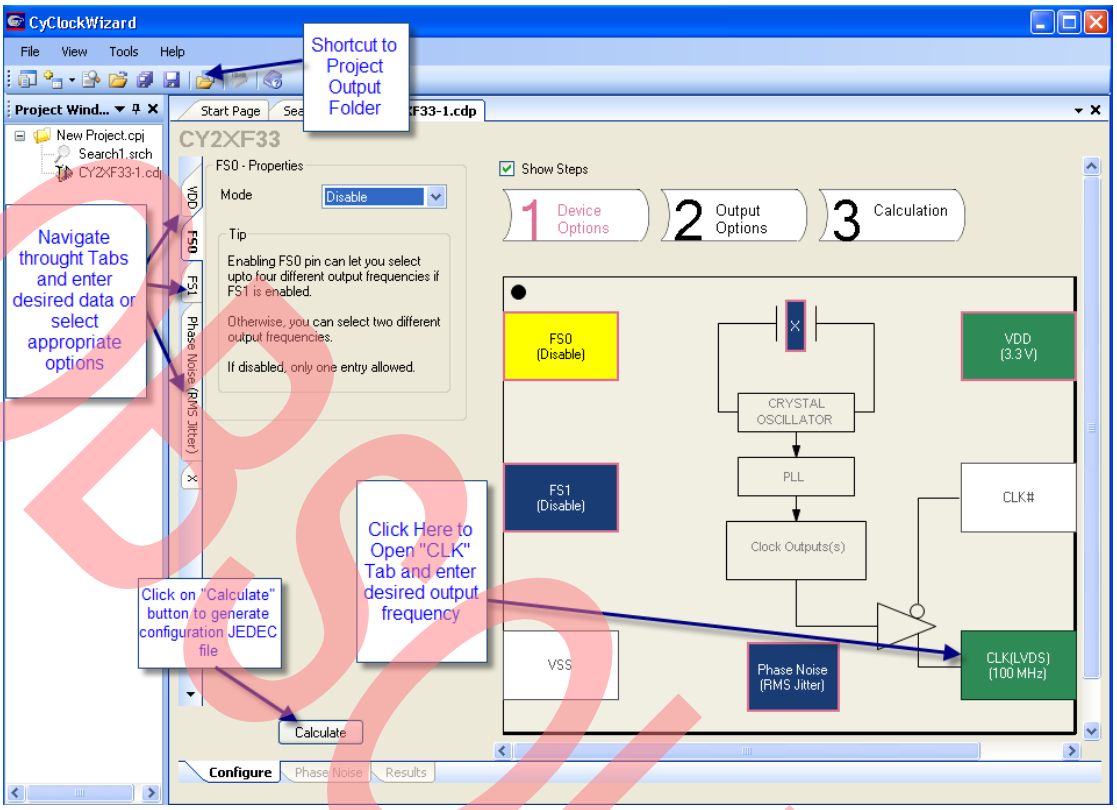
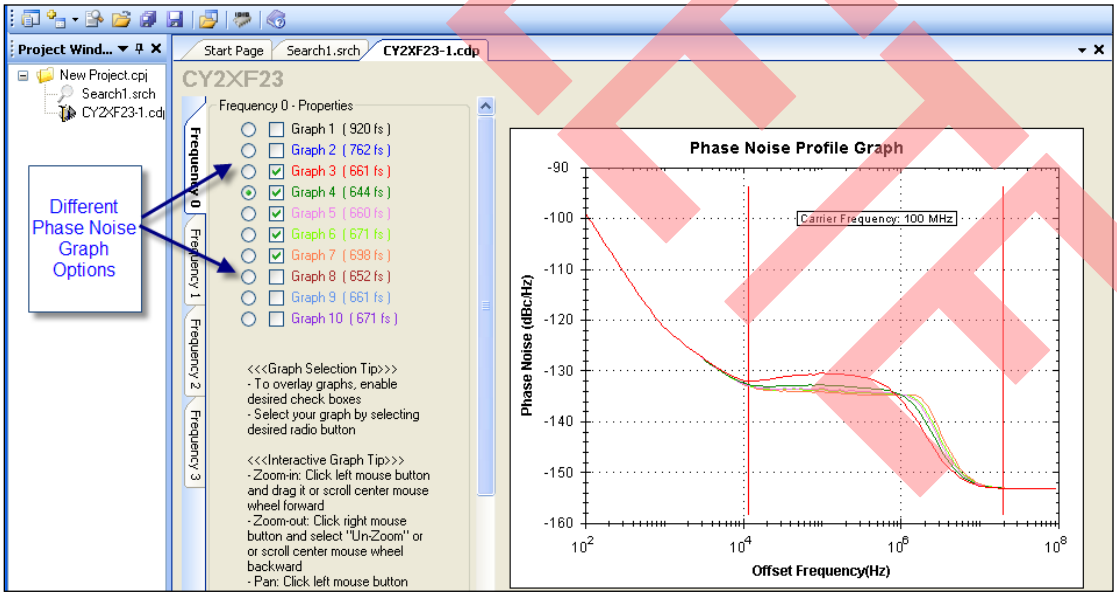


Figure 5. Different Phase Noise Graph Options



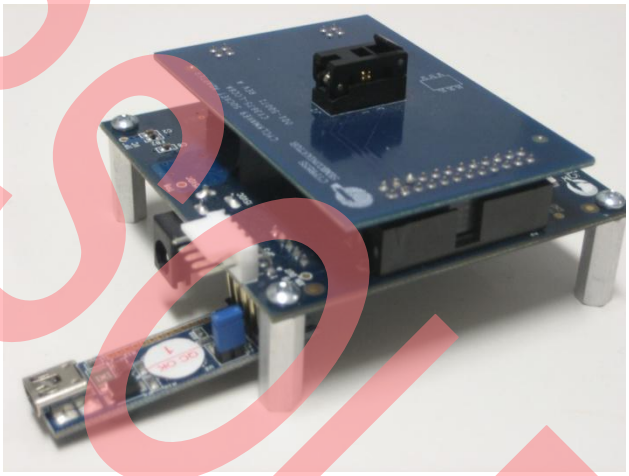
4.2 Device Programming with the CY3675

CyClockWizard software is used in combination with the CY3675 programmer to program FleXO devices. The required CY3675 programming adapter is CY3675-LCC6A.

Setting up the CY3675 is easy:

1. Mount the adapter CY3675-LCC6A onto the CY3675-CLKMAKER1 base board.
2. Install the USB interface board onto the 5 pin connector on the bottom of the board. *Do not* plug it into the 5 pin connector on the *top edge* of the board. Figure 6 shows all of the pieces connected together.
3. Connect the board to a power source and connect the USB cable between the board and the computer.
4. Place an unprogrammed FleXO device in the IC socket.

Figure 6. Connection of the USB interface board



The CyClockWizard has two possible flows to program a device.

1. **Instant Programming**: Immediately following the creation of a device configuration in CyClockWizard
2. **Multi Step Programming**: To program using a previously created device configuration

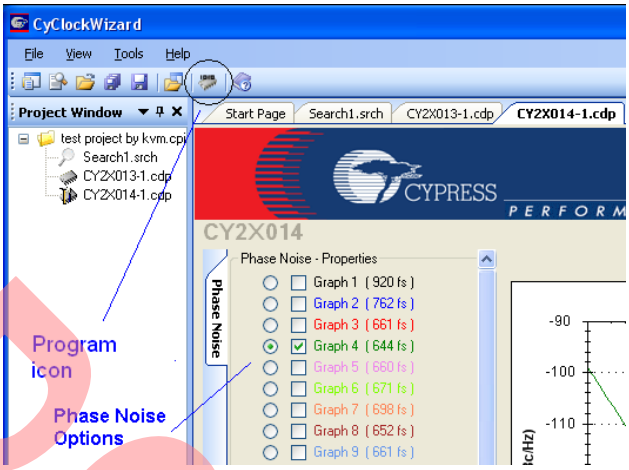
4.3 Instant Programming

After creating a device configuration in CyClockWizard (by clicking on the **Configure** button), the **Program** icon is available in the toolbar. This icon is shown in Figure 7. To program a device with the configuration just created,

1. Place a blank FleXO device in the CY3675 socket.
2. Click the **Program** toolbar icon.

CyClockWizard verifies that the CY3675 adapter board is correct, that the device is blank, and it verifies the final programming results. The results are shown in the pop-up log window.

Figure 7. Instant Program Icon



4.4 Multi-step Programming

One step programming is not available for previously created device configurations, as indicated whenever the **Program** icon is grayed out. The steps for programming a device using any previously created *.JED* file are outlined as following.

1. Place a blank FleXO device in the CY3675 socket.
2. Select **Programmer** from the **Tools** menu. This opens a new **Clock Programmer** window.
3. Click the port that appears in the **Available Port(s)** pane. If no port is shown, it is because Clock Programmer is not communicating with the CY3675.
4. Select a Device (part number).
5. Select a *.JED* files by clicking on the **Open JEDEC**" toolbar icon and selecting a file.
6. Click the **Program** toolbar icon.

5 Programming for Production

The CY3675 is a low cost programmer intended for prototyping and other low volume applications. To program devices in larger volumes, customers usually pursue one of the following paths:

- Programming by the customer using a production programmer
- Programming by a Cypress distributor or third party programming vendor
- Programming by Cypress as a custom device

If Cypress performs the programming, then a custom part number is assigned. This option is generally available only for high volume applications. To request a custom Cypress programmed device, please contact your local salesperson.

Regardless of who does the programming, the process of generating JEDEC configuration is the same, and the *.JED* file from CyClockWizard is the same.

6 Summary

The programming of FleXO family devices is two step process. Generate configuration JEDEC file using CyClockWizard 1.0 and program device using CY3675 kit. FleXO clocks provide high performance, and the programmable FleXO devices give you additional flexibility to quickly program parts to meet specific clocking needs.

Appendix A. Available Factory Programmed FleXO Devices

The following tables list some available fixed frequency FleXO devices and the application(s) most commonly associated with the indicated frequencies.

Table 4. Fixed Frequency Crystal Oscillator Products

Part Numbers		Frequency (MHz)	Application
LVDS Output	LVPECL Output		
CY2X013FLXI100	---	100	PCI Express
---	CY2X014FLXI106	106.25	Fibre Channel 1, 2
CY2X013FLXI122	CY2X014FLXI122	122.88	Wireless (UMTS, WCDMA)
CY2X013FLXI125	CY2X014FLXI125	125	1 Gig Ethernet / PCI Express
---	CY2X014FLXI132	132.8125	Fibre Channel / Wireless
---	CY2X014FLXI153	153.6	Wireless (WCDMA, etc.)
---	CY2X014FLXI155	155.52	SONET / SDH
CY2X013FLXI156	CY2X014FLXI156	156.25	10 Gig Ethernet / XAUI
---	CY2X014FLXI159	159.375	10 Gig Fibre Channel / XAUI
---	CY2X014FLXI212	212.5	4 Gig & 8 Gig Fibre Channel
---	CY2X014FLXI311	311.04	SONET / SDH
---	CY2X014FLXI312	312.5	10 Gig Ethernet / XAUI
---	CY2X014FLXI622	622.08	SONET / SDH

Table 5. Fixed Frequency Clock Generator Products

Part Numbers		Frequency (MHz)	Application
LVDS Output	LVPECL Output		
CY2XL11ZXC	---	100	PCI Express
---	CY2XP22ZXC	62.5	1 Gig Ethernet
		125	1 Gig Ethernet / PCI Express
---	CY2XP24ZXC / ZXI	156.25	10 Gig Ethernet / XAUI
		187.5	12 Gig Ethernet
---	CY2XP31ZXI CY2XP311ZXC / ZXI	312.5	10 Gig Ethernet / XAUI
---	CY2XP41ZXC	62.5	DVD-R
		75	SATA / SAS

Appendix B. Verifying Performance

For devices such as FleXO, the term performance almost always means phase noise and jitter. All performance measurements are best made using good quality coaxial cables. When using SMA connectors, the connections should be well tightened. When making measurements on differential signals, matched cables should be used.

Figure 8. FleXO 6-pin LCC Evaluation Board

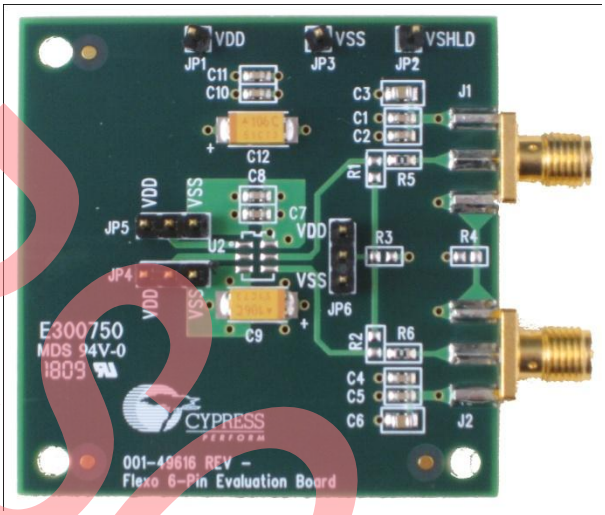
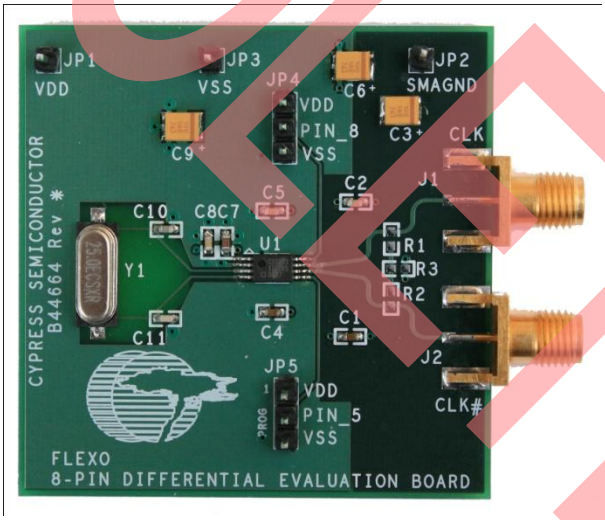


Figure 9. FleXO 8-pin TSSOP Evaluation Board



6.1 Evaluation Board

Evaluation boards are available for FleXO devices in both the 6-lead LCC and the 8-pin TSSOP packages. The SMA connectors make it easy to connect to instruments for measuring device performance. Please contact your Cypress Sales/Marketing person for availability of these boards.

6.1.1 Terminations Guidelines for Evaluation Board

6-pin LCC Evaluation Board(Figure 8)

LVDS Output:

- Fill R1, R2 with 50ohm and R5,R6 with 0 ohm
- Connect 3.3/2.5V to VDD(JP1) and GND to VSS(JP3)

6.1.2 LVPECL Output:

- Fill R1, R2 with 50ohm and R3, R5, R6 with 0 ohm
- For 3.3V supply voltage: Connect 2V to VDD(JP1), -1.3V to VSS(JP3) and GND to VSHLD(JP2)
- For 2.5V supply voltage: Connect 2V to VDD(JP1), -0.5V to VSS(JP3) and GND to VSHLD(JP2)

6.1.3 8-pin TSSOP Evaluation Board(Figure 9)

LVDS Output:

- Mount R1 and R2 resistors with 50ohm
- Connect 3.3/2.5V to VDD(JP1) and GND to VSS(JP3)

6.1.4 LVPECL Output:

- Mount R1, R2 resistors with 50ohm and R3 with 0 ohm
- For 3.3V supply voltage: Connect 2V to VDD(JP1), -1.3V to VSS(JP3) and GND to SMAGND(JP2)
- For 2.5V supply voltage: Connect 2V to VDD(JP1), -0.5V to VSS(JP3) and GND to SMAGND(JP2)

6.2 Phase Noise and Phase Jitter

The most common instrument currently in use for measuring phase noise on low jitter clocks is the Agilent E5052A/B.

The E5052 has a single input. To connect differential output devices, one of the two techniques can be used.

1. Connect only one of the outputs to the instrument. The output must be properly terminated with a 50 Ω DC path. The other output must likewise be terminated with 50 Ω.
2. Combine the two outputs using a 180º power splitter. 50 Ω DC terminations are required on the device side of the power splitter.

Phase jitter is the integration of phase noise over a specific offset frequency range. The integration range can have a significant effect on the resulting phase jitter. The most common range is 12 kHz – 20 MHz, but there are many other ranges in use, and the actual range is application dependent. Be certain to specify the correct range in the E5052.

Table 6. Common Phase Jitter Integration Ranges

Application	Phase Jitter Integration Range
Fibre Channel	637 kHz – 10 MHz
SONET	12 kHz – 20 MHz
1G and 10G Ethernet	1.875 MHz – 20 MHz

For detail on additive phase jitter please refer following white paper: Additive Phase Jitter in High Performance Clock Distribution

6.3 Simulated Versus Actual Phase Noise

CyClockWizard uses a sophisticated algorithm to calculate phase noise for each configuration that it creates. It also calculates the phase jitter over the offset frequency range entered by you.

Figure 10 and Figure 11 show that the calculated phase noise compares quite well with measured phase noise.

6.4 Measuring Jitter

Conventional jitter measurements are period jitter and cycle to cycle jitter. These parameters can be measured on any modern high performance oscilloscope with the appropriate software option. It is important to adjust the input channels so that the signal fills up 90% to 100% of the display vertically, and the scope sampling rate should also be maximized. Coaxial cables are preferred over probes for critical measurements.

Figure 10. Calculated Phase Noise from CyClockWizard

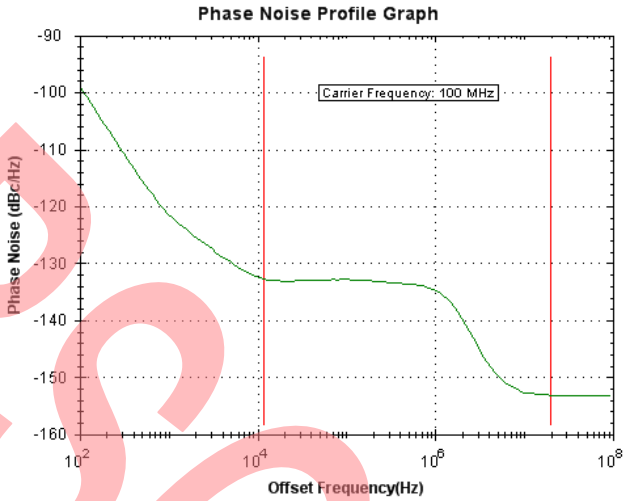
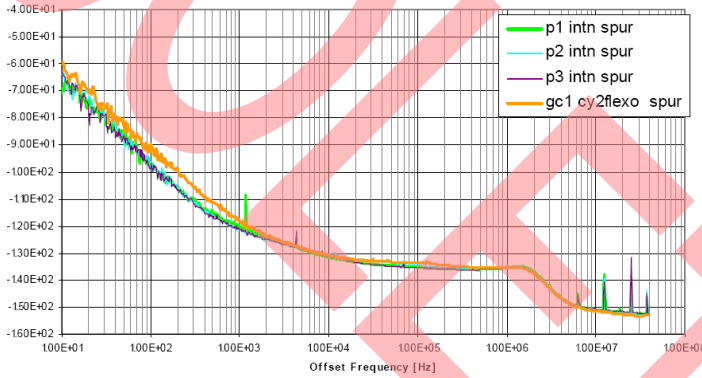


Figure 11. Measured Phase Noise



Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2989913	KVM	07/21/10	New Application Note
*A	3249510	CXQ	05/05/11	Fixed typos, removed references to CCW 2.0 and HiLo.
*B	3555288	BASH	03/20/12	Updated title to read “Programming FleXO™ Low Noise Clock Generators”. Updated Abstract. Updated FleXO Product Overview. Updated FleXO Programming Tools. Updated Programming Flow. Updated Summary. Updated Verifying Performance. Updated in new template.
*C	4472537	TAVA	08/12/14	No technical updates. Completing Sunset Review.
*D	5874297	PAWK	09/01/2017	Obsoleted the spec

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