AN62489 – Powerline Communication (PLC) Low Power Firmware

AN62489

Author: Jeffrey Hushley
Associated Code Example: Yes
Associated Part Family: CY8CPLC20/CY8CLED16P01
Software Version: PSoC® Designer™ 5.1 SP1
Associated Application Notes: None

Application Note Abstract

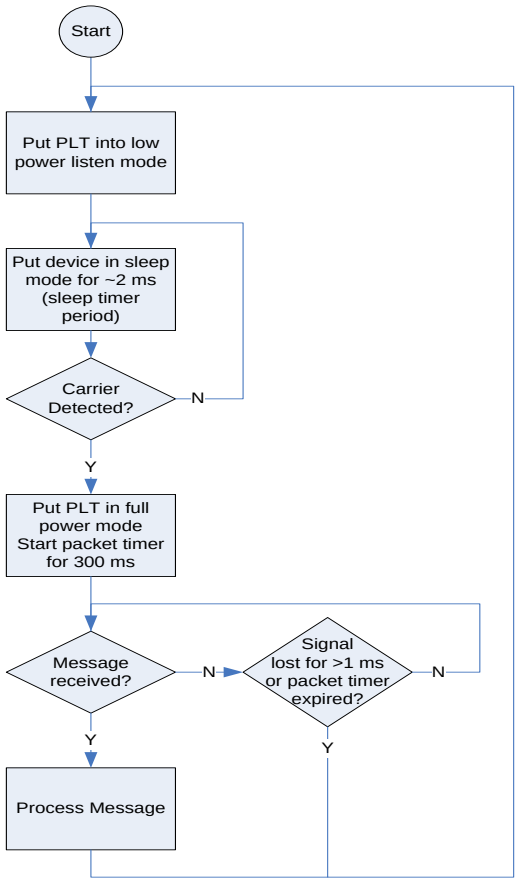
AN62489 describes how the Cypress Powerline Communication (PLC) device can perform with an average low power consumption of < 50 mW. The code example for the CY8CPLC20 is attached.

Basic Operation

Under normal receive mode operation, both CY8CPLC20 and CY8CLED16P01 devices consume ~43 mA of current, which is equivalent to 215 mW of power at 5 V VCC. For systems that have a requirement of < 50 mW average power consumption, the PLC device can be configured in a low-power 'listen' mode, where it turns off most of the Powerline Transceiver (PLT) blocks, turn on the carrier detect blocks, and wait to detect a signal on the powerline. After a signal is detected, the device turns on the remaining PLT blocks for demodulating the PLC signal and forming the PLC packet.

If the packet is intended for this node, the PLC device processes it and then returns to 'listen' mode. If the packet received is not intended for this node or if there is excessive noise that wakes the node up, the device returns to 'listen' mode when the carrier detection is lost or after a 300 ms timeout period. See Figure 1 for the basic low power algorithm.

Figure 1. PLC Low Power Firmware Basic Operation



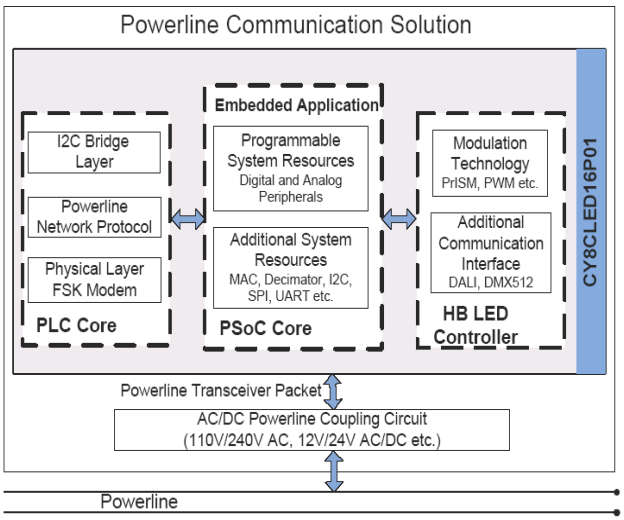
Powerline Communication

Powerlines are widely available communication medium all over the world for PLC technology. The pervasiveness of Powerline also makes it difficult to predict the characteristics and operation of PLC products. Due to the variable quality of Powerlines around the world, implementing robust communication over Powerline has been an engineering challenge for years. The Cypress PLC solution enables secure and reliable communication over Powerline. Cypress PLC solution includes:

- Integrated Powerline PHY modem with optimized filters and amplifiers to work with lossy high voltage and low voltage Powerlines.
- Powerline optimized Network Protocol that supports bidirectional communication with acknowledgement based signaling. In case of data packet loss due to noise on the Powerline, the transmitter can retransmit the data.
- The Powerline Network Protocol also supports 8-bit CRC for error detection and data packet retransmission.
- A Carrier Sense Multiple Access (CSMA) scheme is built into the Network Protocol; it minimizes collision between packet transmissions on the Powerline, supports multiple masters and enables reliable communication on a bigger network.

A block diagram of the PLC solution is shown in Figure 2 with the programmable CY8CLED16P01 PLC transceiver with HB LED controller as the example. The PLC family of devices also contains the fixed-function CY8CPLC10 PLC transceiver, which has an I^2C interface to the host, and a programmable CY8CPLC20 PLC transceiver. The programmable PLC devices can either have the host application running inside or an external interface (I^2C, SPI, UART, and so on.).

Figure 2. Cypress PLC Solution Block Diagram



To interface a PLC device to the Powerline, a coupling circuit is required. The following kits contain the required coupling circuitry for high-voltage or low-voltage powerline applications:

- CY3272 High Voltage PLC Evaluation Kit (EVK)
- CY3273 Low Voltage PLC Evaluation Kit (EVK)
- CY3274 High Voltage Programmable PLC Development Kit (DVK)
- CY3275 Low Voltage Programmable PLC Development Kit (DVK)
- CY3276 High Voltage Programmable PLC + HB LED Control Development Kit (DVK)
- CY3277 Low Voltage Programmable PLC + HB LED Control Development Kit (DVK)

The high voltage kits CY3272, CY3274, and CY3276, are designed with the filtering and power supply circuitry to operate on 110 V to 240 V AC Powerlines. They are compliant to the following CENELEC and FCC standards.

- Powerline Signaling (EN50065-1:2001, FCC Part 15)
- Powerline Immunity (EN50065-2-1:2003, EN61000-3-2/3)
- Safety (EN60950)

The low voltage kits CY3273, CY3275, and CY3277, are designed to operate on 12 V to 24 V AC/DC Powerlines. All three low voltage kits are designed with the filtering and power supply circuitry.

The CY3272 and CY3273 kits are used to evaluate the CY8CPLC10 PLC fixed function device, which has an I^2C port for interfacing to an external host microcontroller.

The CY3274 and CY3275 kits are used to develop an embedded powerline networking application on the CY8CPLC20 programmable PLC device. They contain user interface options such as I^2C, RS232, GPIO, analog voltage, LCD display, and LED to develop a full application.

The CY3276 and CY3277 kits are used to develop a powerline controller and embedded host application with High Brightness (HB) LED control on the CY8CLED16P01 Programmable PLC + HB LED Control device. They also contain many user interface options such as I^2C, RS232, GPIO, analog voltage, LCD display, and LED to develop a full application. They have the added feature of a HB RGB LED daughter card to evaluate lighting control with powerline communication by the CY8CLED16P01 device.

More information on PLC can be found at www.cypress.com/go/plc.

Power Consumption

In 'listen' mode, the device current consumption was measured to be 8.8 mA (power consumption of 44 mW). In normal receive mode, the device current consumption was measured to be 43 mA (power consumption of 215 mW). If the line is clean at least 97% of the time, the total average power consumed is < 50 mW as seen in Table 1.

Table 1. Average Power Consumption

			Average Power (mW)
	Current (mA)	**Power (mW)**	**97% Free Line**
Listen Mode	8.8	44	42.7
Receive Mode	43	215	6.5
Total			49.2

Adaptive Carrier Detect Threshold

The carrier detect threshold is designed to adapt to the noise on the line so that the average power consumption stays under 50 mW. If noise causes two consecutive false triggers, the threshold is increased. On there other hand, if there is no signal on the line for > 500 ms, the threshold is decreased. This is to ensure that the device has the best sensitivity possible while consuming < 50 mW.

To differentiate between noise and PLC signals, the free time between carrier detections is measured. According to the CENELEC Band-In-Use (BIU) protocol, which is used by the Cypress PLC solution, there must be at least 85 ms free time before another PLC signal can be transmitted. **Note** This system uses 80 ms as the threshold.

The minimum threshold is 125 µVrms and the maximum threshold is 5 mVrms. Therefore, if a signal that exceeds this carrier detect threshold is present for at least three sleep timer cycles (~6 ms total), the device switches to the receive mode so that it can demodulate the PLC signal. The TX Delay parameter should be set to the maximum (25 ms) in order to provide enough time for the receiver to detect the signal and switch to receive mode in time to demodulate the signal.

Code Example

The code example was created with PSoC Designer 5.1 SP1. A screenshot of the chip level view of the code example is shown in

Figure 3. The following user modules are used in the code example:

- Powerline Transceiver
- Counter16: For the 300 ms timeout. The configuration is shown in Figure 3.
- OneShot: Stabilizes the filtered received signal to generate a constant high logic level when a carrier is present. It drops to a low logic level when the carrier is absent for > = 8 * clock period = 8 * ~50 µs = ~400 µs. The configuration of the OneShot user module is shown in Figure 4. The output of the OneShot user module is connected to the port pin P2[6] to be monitored for the carrier detection in code.
- LED: Three LED user modules (TX, RX, BIU) are used to represent when the PLT user module is transmitting, receiving, or has detected a Band-In-Use timeout condition, respectively. In debug mode (when PLC_DEBUG = 1), there are two additional LED user modules that are used to indicate the power mode of the device. ReceiveMode_LED will go low when the PLT is in listen mode and go high when in full power receive mode. In listen mode, the SleepMode_LED user module will go high when the CPU is in low-power sleep mode, go low when it is checking for a carrier. In full power receive mode, the SleepMode_LED will always be low. The pins used are as follows:
  - P2[1] = BIU LED
  - P2[3] = RX LED
  - P2[5] = TX LED
  - P1[2] = Sleep Mode LED
  - P1[6] = Full Power Receive LED
- LCD: When a message is received, it will display the first byte of data on the second row of the LCD. It will also display the number of messages received on the first row of the LCD. In debug mode (when PLC_DEBUG = 1), it will also display the carrier detect threshold level in the bottom right corner of the LCD.

After placing the user modules, the following global resources were modified to reduce power consumption:

- CPU Clock = SysClk / 8. Running the CPU at this frequency (3 MHz) will reduce the current consumption by ~3mA.
- SysClk*2 Disable = Yes. Since the 48MHz clock is not used, this can be disabled. This will reduce the current consumption by ~1mA.
- Analog reference power, op-amp bias, and analog buffer power. These settings are dynamically modified in the firmware. In listen mode, they are set to low power. In receive mode, they are set to high power.

Figure 3. PLC Low Power PSoC Designer Chip View

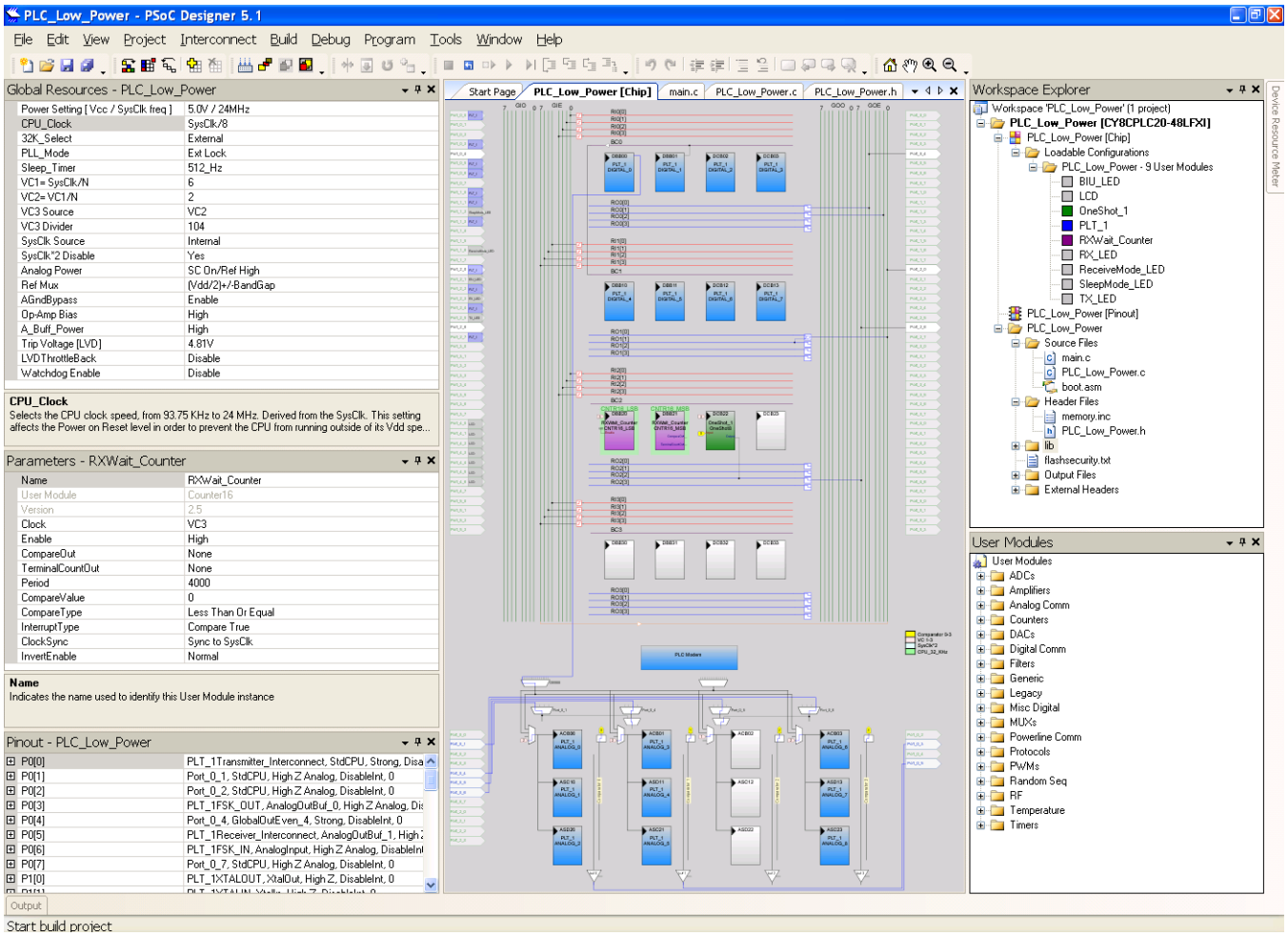


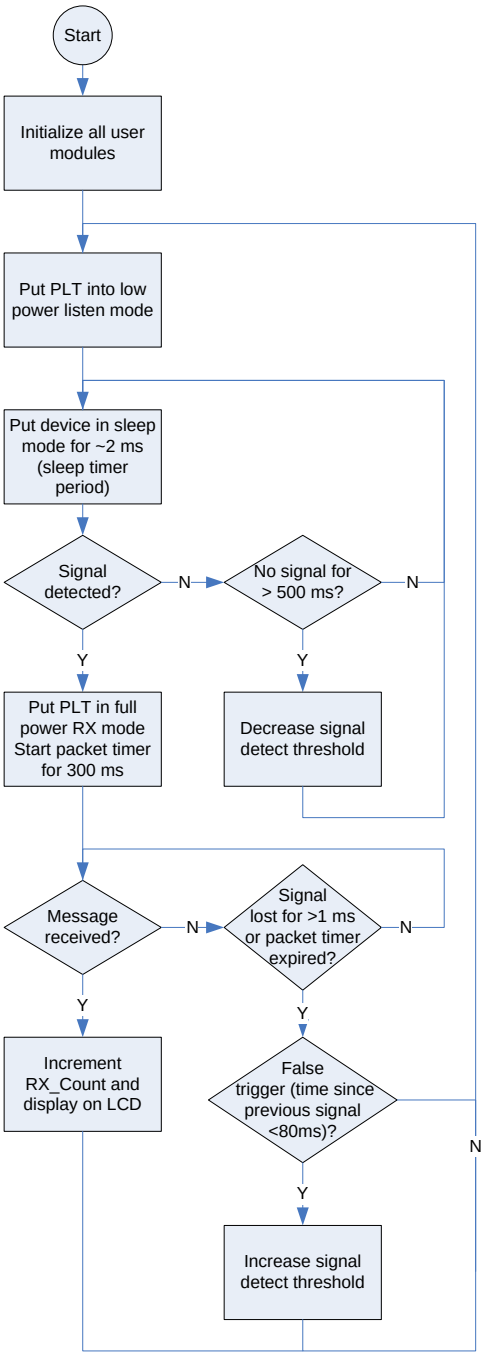
Figure 4. OneShot Configuration

Firmware Algorithm

The firmware is written in C, with the exception of the PLT interrupt routines (in *PLT_1INT.asm*), which are modified to drive the transmit, receive, and band-in-use LEDs.

The algorithm for the code example is shown in Figure 5. It is based on the basic operation diagram shown in Figure 1. It has additional details on detecting the carrier, as well as adapting the threshold based on the noise in the system. The received message is processed by incrementing a count and displaying it on the LCD.

Figure 5. PLC Low Power Code Exapmle



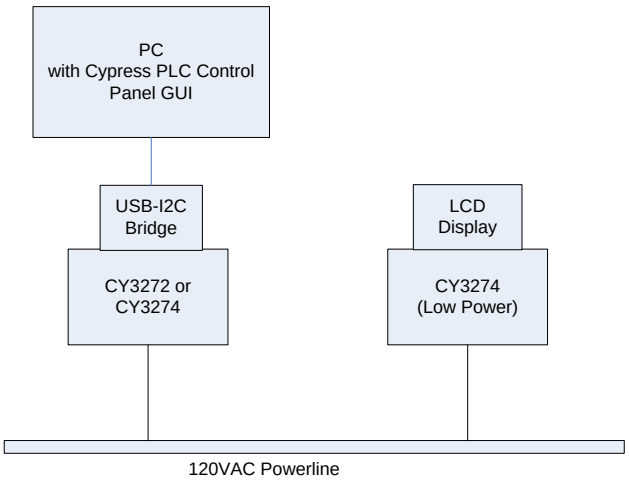
Implementation on Hardware

The attached code example uses the same hardware as the any of the PLC development kits (CY3274-CY3277). Follow these steps to set up the system:

1. Connect the LCD user module to the LCD header
2. Connect the power cable from the mains to the board. The blue power LED should turn on
3. Connect the USB cable from the PC to the MiniProg programmer (included in the DVKs)
4. Connect the MiniProg to the ISSP connector.
5. Either open PSoC Programmer or in PSoC Designer, click Program->Program Part. Load the PLC_Low_Power.hex file from the attached code example. Make sure programming mode is set to Reset. Program the device.
6. Remove the MiniProg from the ISSP connector.
7. Press the Reset button. The LCD should display:

To evaluate the system, a second PLC board with an I^2C interface can be used. The PLC Control Panel GUI can be run on a PC and interfaced to the board with the CY3240 USB-I^2C bridge board (included in the PLC kits). A high-voltage AC example using two CY3274 boards is shown in Figure 6. The receiving board displays the number of packets successfully received on an LCD display. The PLC Control Panel GUI can be downloaded at www.cypress.com/?rID=38135. The GUI user's guide contains Instructions for programming the PLC DVKs to work with the GUI.

Figure 6. PLC Hardware Test Setup



The receiving board is programmed with the listen mode firmware. The transmitting board has the following configuration (set by the GUI):

- 2400 bps baud rate
- 125 mVp-p transmit amplitude (CENELEC compliant when using the external circuitry on the CY3274). If using the low voltage PLC boards, then a 1.55Vp-p amplitude is recommended.
- 25 ms Transmit Delay (for ensuring a clean line before signal transmission and to give the PLC device time to wake up from listen mode)
- Acknowledgment mode
- Retry Count of 1

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Document History

Document Title: AN62489 – Powerline Communication (PLC) Low Power Firmware

Document Number: 001-62489

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2965438	FRE	06/30/2010	New Application Note.
*A	3222362	FRE	04/11/2011	Updated code example to PSoC Designer 5.1 SP1 Removed LED workaround In the code example, moved debug mode sleep and full power indicator LEDs to pins P1[2] and P1[6], respectively

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