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AN61904

How HX2LP™ Addresses Byte and Word-Addressable SPI EEPROMs

Author: Rama Sai Krishna Vakkantula
Associated Project: Yes
Associated Part Family: CY7C65630/20
Software Version: None
Related Application Notes: None

If you have a question, or need help with this application note, contact the author at rskv@cypress.com.

The SPI EEPROMs connect to the HX2LP™ to store configuration settings. To read the configuration settings from the EEPROM, HX2LP first identifies whether the connected EEPROM is byte-addressable or word-addressable. This application note lists the sequence of operations that HX2LP executes to identify the type of EEPROM connected to it.

Introduction

EZ-USB® HX2LP is Cypress's next generation family of high-performance, low-power USB 2.0 hub controllers. HX2LP is an ultra low-power single-chip USB 2.0 hub controller with integrated upstream and downstream transceivers. The hub also contains a USB serial interface engine (SIE), USB hub control, and repeater logic and transaction translators logic (TT). Cypress also integrates many of the external passive components, such as pull-up and pull-down resistors, reducing the overall bill of materials required to implement a hub design. The HX2LP portfolio consists of CY7C65630 and CY7C65620. CY7C65630 is for ultra low-power applications that require four downstream ports. All four ports share a single transaction translator. CY7C65620 is for a 2-port bus-powered application. Both ports share a single transaction translator.

Configuration Options

Systems using HX2LP have the option of using a fuse ROM, which is preset at the factory to configure the hub. Otherwise, it needs an external EEPROM for the device to obtain a unique VID, PID, and DID. HX2LP can communicate with SPI EEPROMs that are either double byte-addressed or single byte with the ninth bit within the instruction byte, such as the 25LC040 parts. The 25LC080 EEPROM uses the double-byte address format allowing the HX2LP to communicate with these parts. The '010s and '020s use the same command format that is used to interface with the '040', and thus these can also be used to interface with the HX2LP.

If the attached EEPROM is blank (0xFF), the hub enumerates as a vendor-class device. In this configuration, the hub connects to the Cypress driver to allow you to program the EEPROM. When the EEPROM is programmed, a power cycle configures the chip as a hub-class device.

0xD0 Load

With this EEPROM format, only a unique VID, PID, and DID must be present in the external SPI EEPROM. The contents of the EEPROM should contain the information provided in Table 1 in the same format:

Table 1. 0XD0 Load

Byte	Value
0	0XD0
1	VID (LSB)
2	VID (MSB)
3	PID (LSB)
4	PID (MSB)
5	Reserved
6	DID (MSB)

Similarly, there are 0XD2 and 0XD4 loads, which provide more flexibility to change the configuration settings of the HX2LP.

SPI EEPROM

The bus signals needed to access the EEPROM are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. A Chip Select (CS) input controls the access to the device. Table 2 contains a list of the possible instruction bytes and the format to access the EEPROM. This table explains the sequence of instructions that flows from the HX2LP to the EEPROM over the SPI interface bus.

Note The EEPROMs connected to the HX2LP can be from any company (as long as they use the SPI interface with double byte-addressed or a single byte with the ninth bit within the instruction byte). In this application note, Microchip EEPROMs are used to list the sequence of operations that the HX2LP follows to identify the specific type of EEPROM. Note that even if an EEPROM from another company is connected to the HX2LP, the sequence of operations will be the same. So you can use the flow charts provided in this application note as a reference to check the sequence of steps if there is a doubt that the HX2LP is unable to read data from the specific EEPROM that is connected to it.

Table 2. EEPROM Instruction Set

Instruction Name	Instruction Format (Bits/Hex)	Description
WRSR	0000 0001 (0x01)	Write status register
WRITE	0000 0010 (0x02)	Writes data to the memory array beginning at the selected address
READ	0000 0011 (0x03)	Reads data from the memory array beginning at the selected address
WRDI	0000 0100 (0x04)	Resets the write-enable latch (disable write operations)
RDSR	0000 0101 (0x05)	Read status register
WREN	0000 0110 (0x06)	Sets the write-enable latch (enable write operations)

Flow Chart

The flow chart in Figure 1 on page 3 shows the sequence of operations that the HX2LP executes to identify the type of EEPROM connected to it, before reading the configuration settings from it. The following sections discuss the steps for byte-addressable and word-addressable SPI EEPROMs.

HX2LP Connected to Byte-Addressable EEPROMs

As soon as the HX2LP is powered up, it sets the write-enable latch of the EEPROM by sending the WREN (0X06) instruction. Next, HX2LP reads the read status register by sending the RDSR (0X05) instruction, and ideally expects 0X02 as the response. HX2LP tries to get the data present at the address location 0X00. If the response data from the EEPROM is 0XD0, 0XD2, or 0XD4, then HX2LP reads the configuration data from the address location 0X00 by sending the READ (0X03) instruction. This sequence of steps is provided under the path 'BYTE ADDRESSABLE EEPROM' in the flow chart shown in Figure 1 on page 3.

Here is the summary of the sequence of steps that occur in the case of the byte-addressable EEPROM:

WREN (0X06) → RDSR (0X05) → 0X02 (expected response) → READ (0X03) the address 0X00 → response data (0XD0/0XD2/0XD4) → READ (0X03) the configuration data from the starting address 0X00. This sequence is shown in Figure 2 and Figure 3 on page 4.

Figure 1. Flow Chart

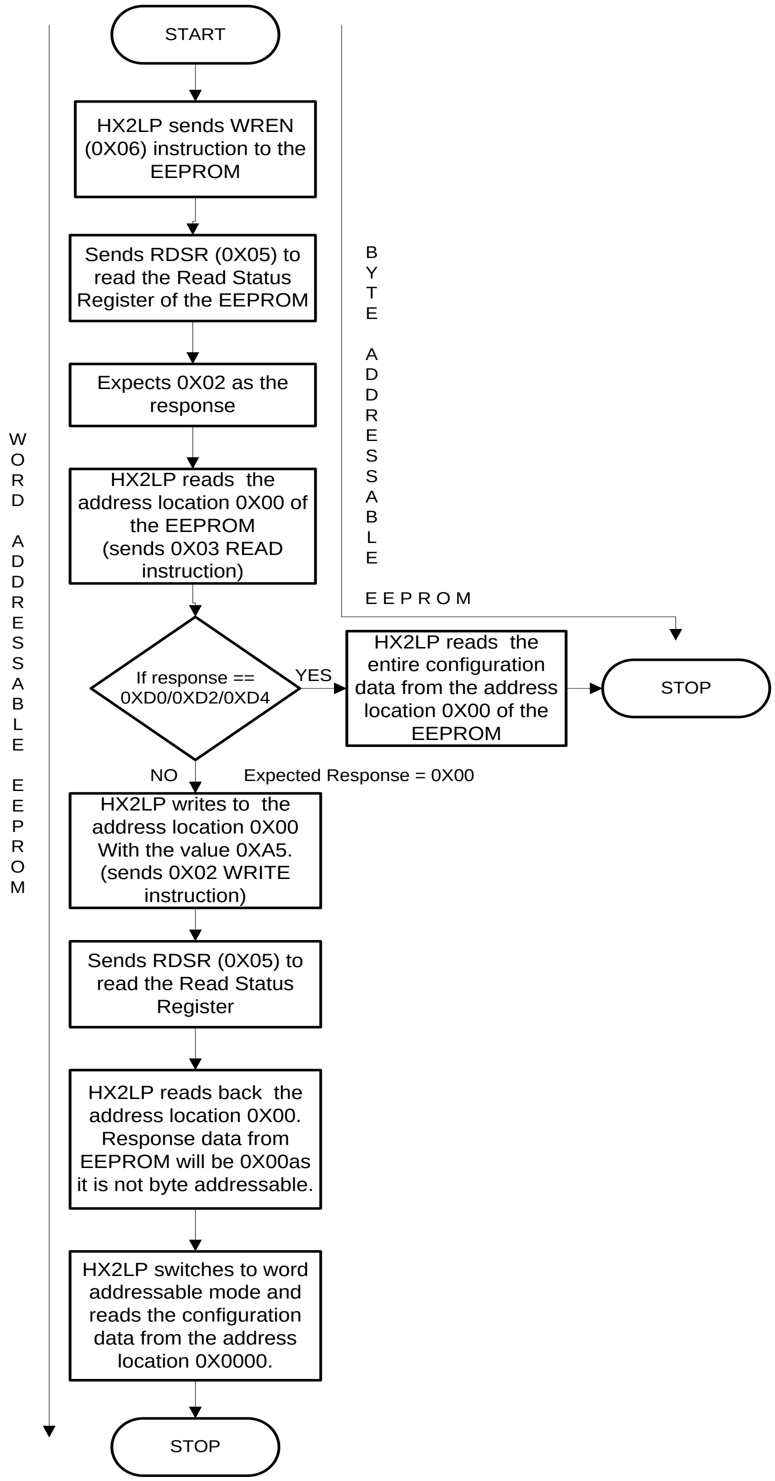


Figure 2. Data Flow Over the SPI Bus (HX2LP Connected to Byte-Addressable EEPROM with 0XD4 Load)

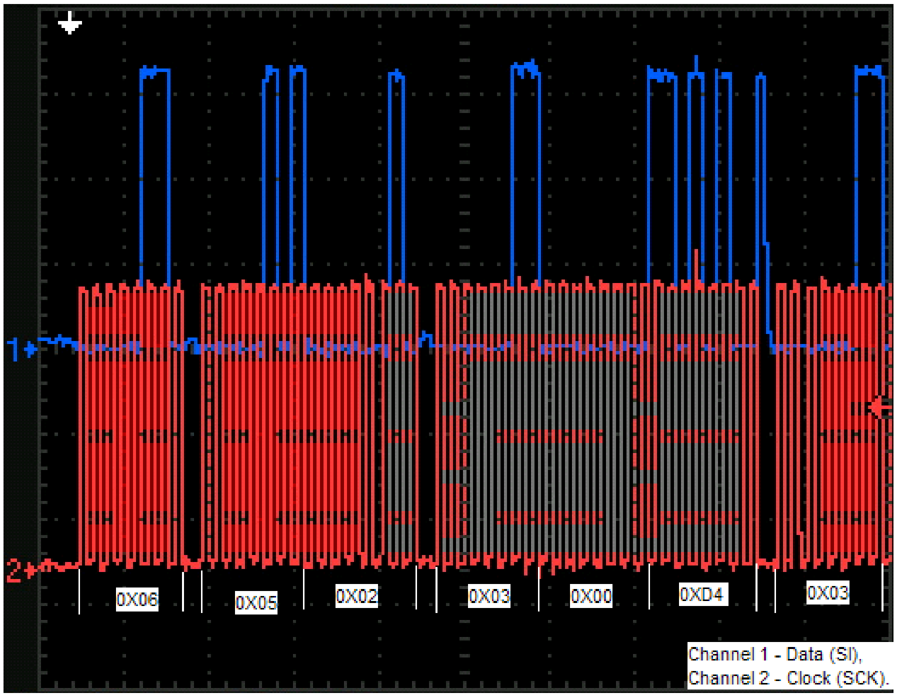
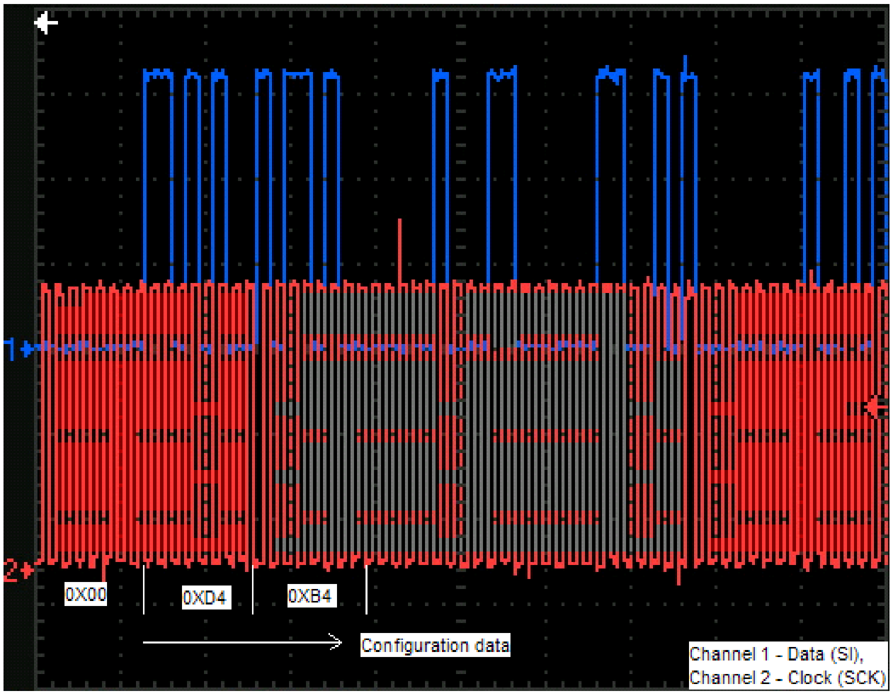


Figure 3. Continuation of Figure 2



HX2LP Connected to Word- Addressable EEPROMs

Until the HX2LP reads the address location 0X00, the initial steps are the same whether it is byte-addressable or word-addressable. Here, the response data from the EEPROM is not one among 0XD0, 0XD2, or 0XD4, because the connected EEPROM is word-addressable. HX2LP receives 0X00 as the response to READ at the address location 0X00. HX2LP writes the address location 0X00 with the value 0XA5 and reads it back. As the connected EEPROM is a word-addressable EEPROM, the HX2LP receives 0X00 as the response. HX2LP treats the connected EEPROM as word-addressable and reads the configuration data from the address location 0X0000 (16-bit address) by sending the READ (0X03) instruction. This sequence of steps is provided under the path 'WORD ADDRESSABLE EEPROM' in the flow chart shown in Figure 1 on page 3.

Here is the summary of the sequence of steps that happen in the case of the byte-addressable EEPROM:

WREN (0X06) → RDSR (0X05) → 0X02 (expected response) → READ (0X03) the address 0X00 → response data 0X00 → WRITE (0X02) the address 0X00 with 0XA5 → RDSR (0X05) → 0X02 (expected response) → READ back the address 0X00 → response data 0X00 → READ (0X03) the configuration data from starting address 0X0000 (16-bit address). This sequence is observed in Figure 4, Figure 5, and Figure 6 on page 5.

.Figure 4. Continuation of Figure 3

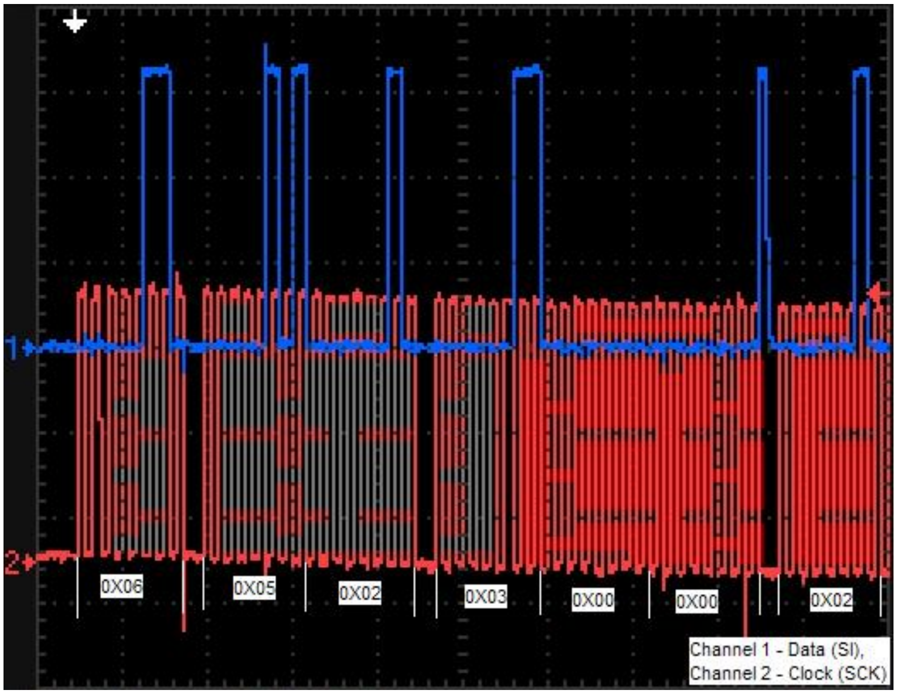


Figure 5. Continuation of Figure 4

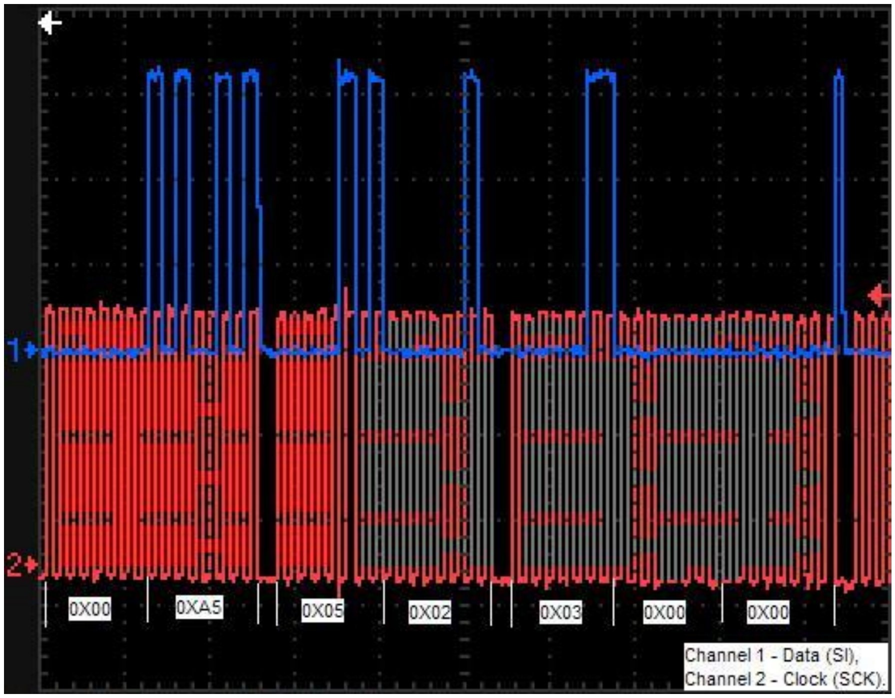
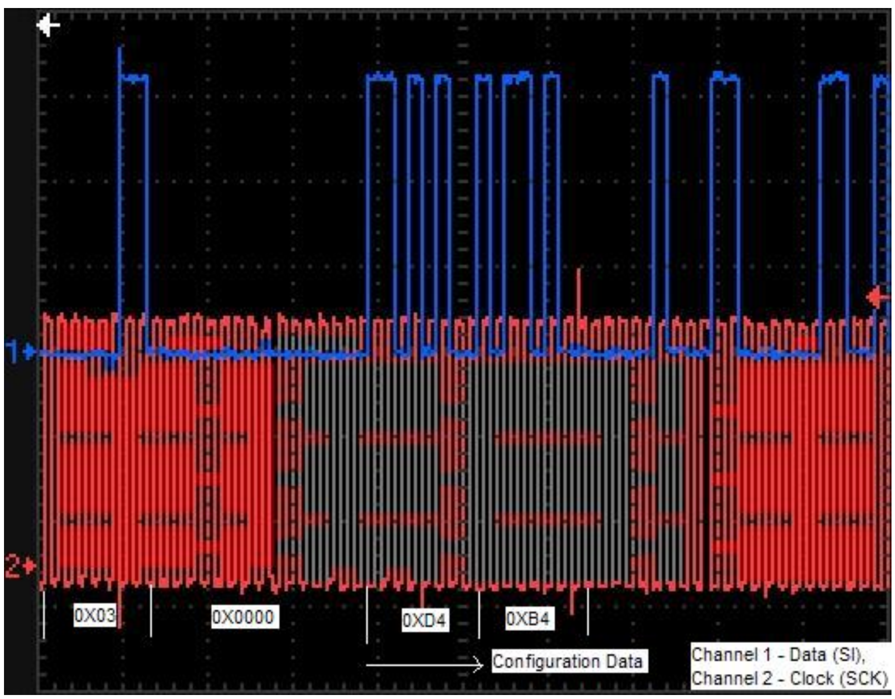


Figure 6. Continuation of Figure 5



Summary

The HX2LP can communicate with an SPI EEPROM that is either double byte-addressed or single byte with the ninth bit within the instruction byte. The sequence of steps that HX2LP goes through to identify the type of EEPROM that is connected are shown in the form of a flow chart and through the captured waveforms over the SPI bus.

References:

For more information about HX2LP, visit http://www.cypress.com/?id=2411.

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Document History

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**	2937619	RSKV	05/26/2010	New Application note
*A	3115986	RSKV	12/20/2010	Added Note to the SPI EEPROM section and references.
*B	4031558	RSKV	06/17/2013	Updated document template.

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