



Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

Peak Detection with PSoC[®] 3 and PSoC 5LP

Author: Dan Sweet
 Associated Project: Yes
 Associated Part Family: PSoC 3 and PSoC 5LP
 Software Version: PSoC[®] Creator™ 3.1 SP2
 Related Application Notes: None

This application note describes several techniques for implementing a peak detector in PSoC[®] 3 and PSoC 5LP. Some of the peak detector designs have been encapsulated as PSoC Creator™ components for easy reuse.

1 Introduction

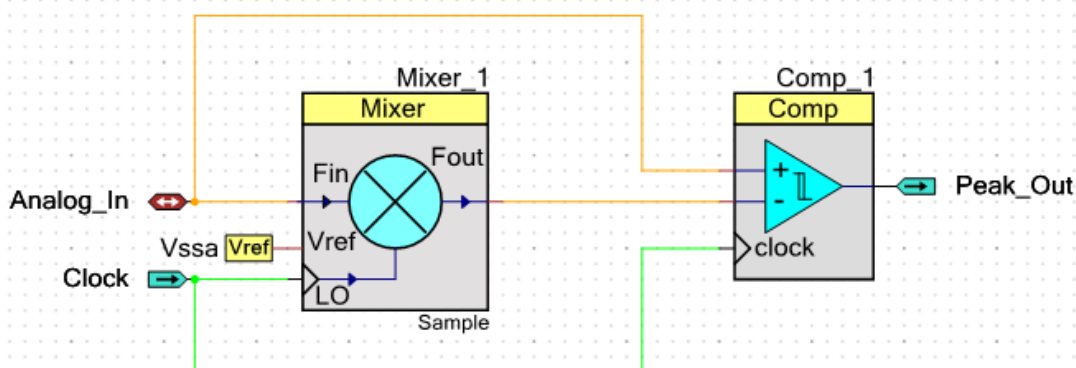
A peak detector identifies the peaks of an input waveform and produces an output based on the detected peaks. The output of the peak detector depends on the type of peak detector used. Some peak detectors produce a digital output consisting of information about when positive and negative peaks of a waveform occur. In this case, the digital information can also be used to determine the direction of the slope of the input waveform. Other peak detectors produce an analog output with a magnitude equal to the last detected peak, or the magnitude of the maximum peak encountered.

Accurately detecting the peaks in an input waveform can be useful in a variety of applications. This application note describes how several peak detection methods are implemented in PSoC 3 and PSoC 5LP.

2 Peak Detector Using Sample and Hold

One method for constructing a peak detector uses a comparator and a down-mixer acting as a sample and hold. When the slope of the input is positive, the output of the peak detector will be high. When the slope of the input is negative, the output of the peak detector will be low. Positive peaks are represented with a falling edge on the output, and negative peaks are represented with a rising edge. Figure 1 shows a schematic for this method. For additional information on how the mixer component acts as a sample and hold circuit, refer to the mixer component [datasheet](#) within PSoC Creator.

Figure 1. Peak Detector with Sample and Hold

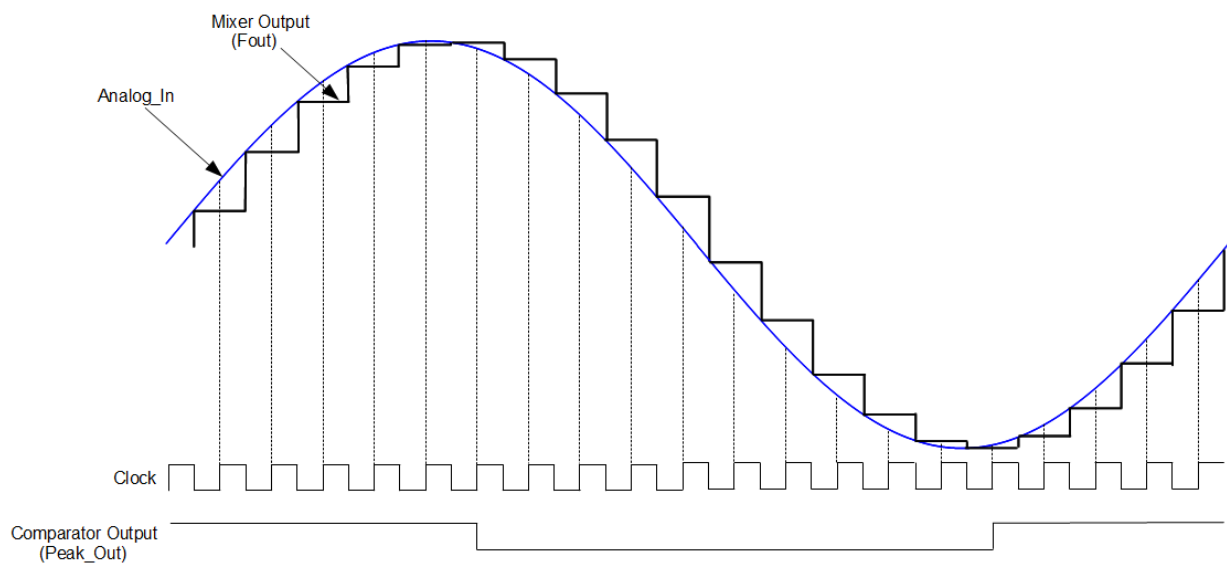


A down mixer is used as a sample and hold whose output is fed to a comparator and compared to the original input signal. The output of the sample and hold is held on the falling edge of the sample (LO) clock. The comparator is clocked on the rising edge of the sample clock which creates a half clock cycle delay between the two signals at the comparator. This ensures the sampled signal is stable and appropriately delayed from the input signal. This concept is illustrated in Figure 2.

There is approximately 10 mV of hysteresis built into the comparator. This helps ensure that slowly moving voltages or slightly noisy voltages will not cause the output of the comparator to oscillate. Enabling hysteresis in the comparator is recommended for most input signals to reduce false peak detections.

Figure 2 shows a sinusoidal input waveform. When the slope of the input waveform is positive, the sample and hold output is less than the input waveform at each rising edge of the comparator clock, so the output of the comparator is high. When the slope of the input waveform is negative, the sample and hold output is greater than the input waveform at each rising edge of the comparator clock, so the comparator output is low.

Figure 2. Sample-and-Hold Peak-Detection Waveform



To accurately detect each peak, the sample clock frequency must be adjusted to meet the frequency and noise characteristics of the input signal. As the input sample clock frequency increases, the delay between the peak of the input waveform and the output of the comparator decreases. However, the increased frequency also makes the circuit more susceptible to false peak detections because of noise. This is because there is less difference between the input waveform and the sample and hold output at higher frequencies. Decreasing the input sample clock frequency will increase the delay between the peak of the input waveform and the output of the comparator, but will also be less susceptible to erroneous peak detections due to noise.

Figure 3 shows the effect when the clock speed is set too high. The output of the comparator triggers very close to the peaks of the waveform, but the output triggers multiple times because of noise and a slowly changing input signal. In this case, the clock rate is 200x the frequency of the 1 V peak-to-peak input sine wave.

Figure 3. Clock Too Fast

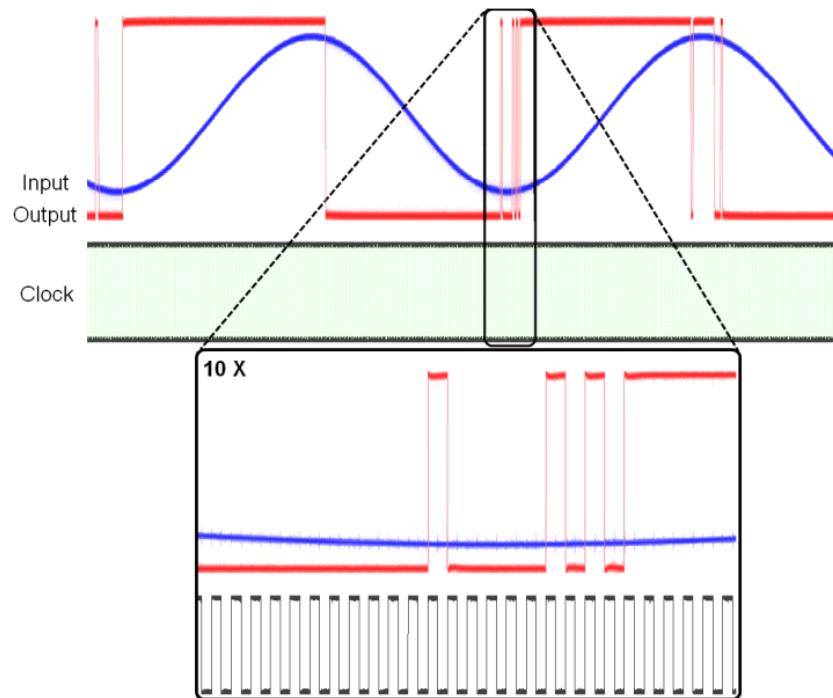


Figure 4 shows the effect when the clock speed is set too low. Notice that the output should be high during the positive slope; the output is severely delayed from the input waveform. Some peaks may be missed altogether. In this case, the clock rate is 2.5x the frequency of the 1 V peak-to-peak input sine waves; the input is sampled only two or three times per cycle.

Figure 4. Clock Too Slow

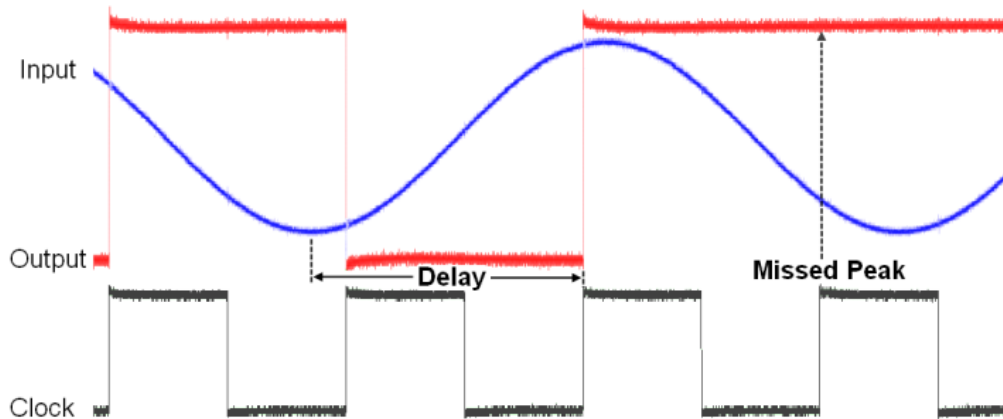
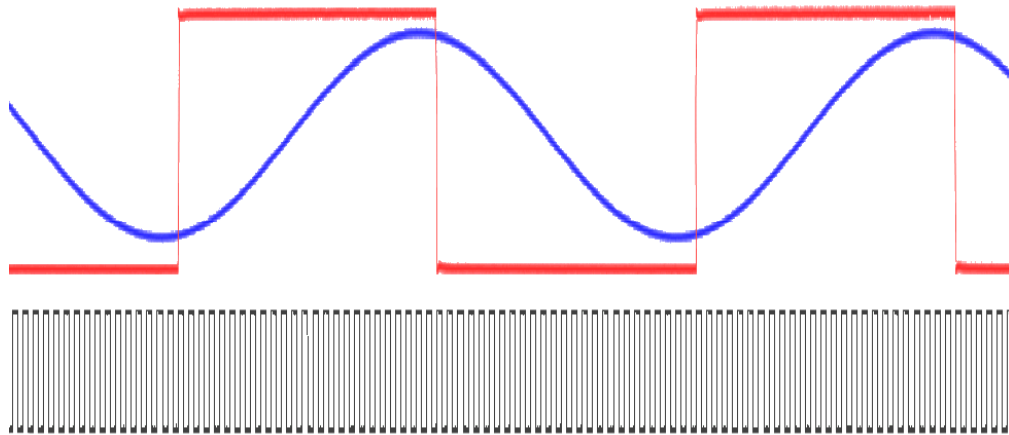


Figure 5 shows the output when the correct clock is selected. There is very little delay between the input peaks and the output; there are no erroneous triggers or missed peaks. In this case, the clock rate is 50x the frequency of the 1-V peak-to-peak input sine wave.

Figure 5. Correct Clock Selection

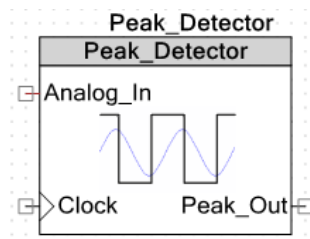


The appropriate clock speed differs for each application, depending on the frequency and noise characteristics of the input waveform.

Note: The LO Frequency parameter for the sample and hold component must be set to match the external LO clock. This parameter is used to determine the appropriate values for the internal input and feedback resistance of the mixer opamp circuit. The maximum LO input frequency supported by the mixer block is 4 MHz.

For easy reuse, the hardware-based design for this peak detector is encapsulated as a component in a PSoC Creator library project. Figure 6 shows the component symbol.

Figure 6. Sample and Hold Peak Detection Component



An example project (*A_SH_Peak_Detector*) is provided in the attached workspace to demonstrate the use of this component.

3 Peak Detector Using an SIO Pin

An alternative peak detecting method to the sample and hold technique can be created using a special I/O (SIO) pin in PSoC 3 and PSoC 5LP. SIO pins provide a programmable input threshold, which allows the SIO pin to function as an analog comparator. When a signal is supplied as an input threshold, it passes through a reference generator block. The reference generator block introduces a time delay of approximately 200 ns into the threshold signal. This time delay, similar to the delay introduced by the sample and hold component used in the last example, enables the SIO to be used as a peak detector.

Figure 7 shows the block diagram for an SIO peak detector, which requires two pins: one SIO input pin and one analog input pin. The input signal is tied to both the SIO input and to the SIO threshold input through an analog pin. The threshold input signal is delayed and compared to the original input signal using the differential input buffer of the SIO.

Figure 7. SIO Peak Detector Block Diagram

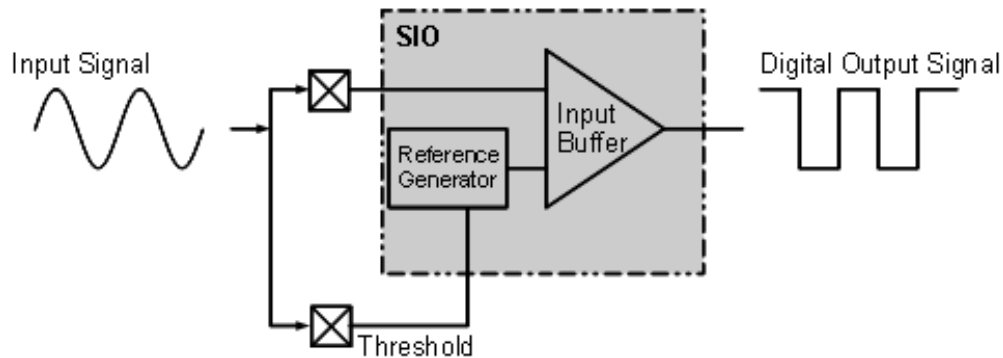
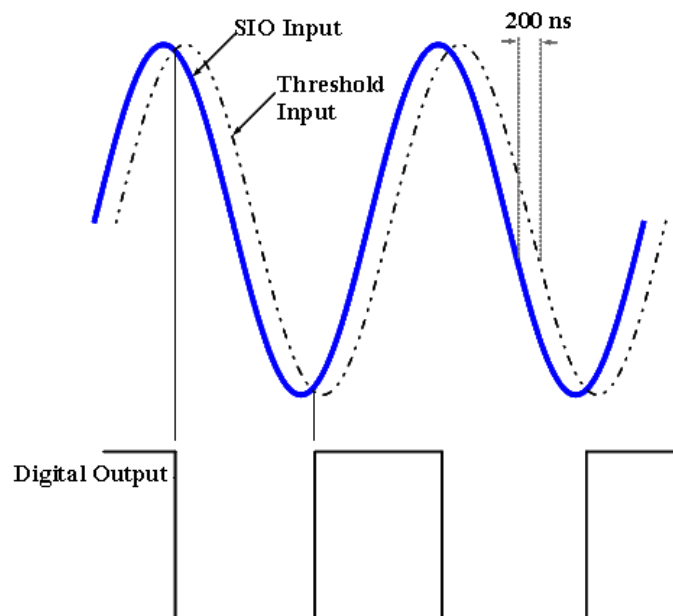


Figure 8 shows the expected waveforms for the SIO peak detector circuit. The threshold input is delayed by approximately 200 ns, which allows the differential input buffer (acting as a comparator) to detect the peaks in the input waveform.

Figure 8. SIO Peak Detector Waveform



The SIO has approximately 50 mV of hysteresis. This, combined with the 200-ns delay induced by the reference generator, limits the frequency range of this peak detector. With a 1 V peak-to-peak sine wave input, the frequency is limited to a range of approximately 250 kHz to 1.25 MHz. However, the frequency range also depends on the amplitude of the input signal and the amount of noise in the system. An additional RC delay circuit can be added to the threshold analog input to induce additional delay. This will enable the peak detector to work with lower frequency signals.

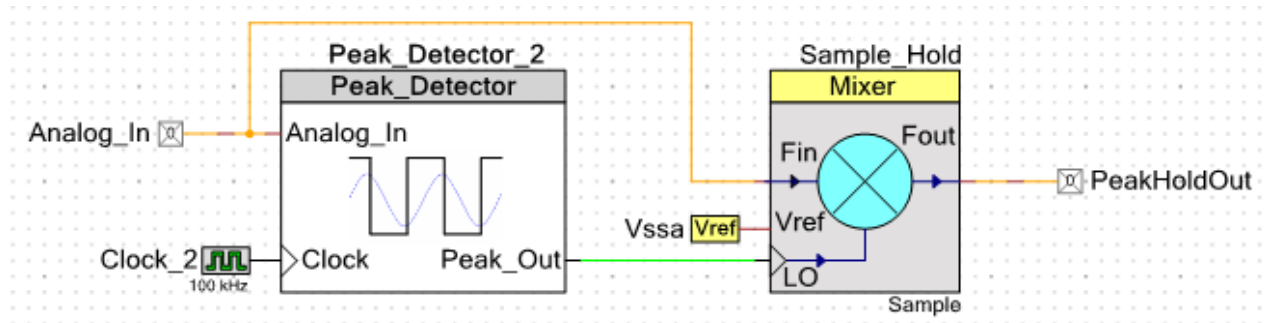
An example project (*B_SIO_Peak_Detector*) is provided in the attached workspace to demonstrate the use of an SIO pin as a peak detector.

4 Peak and Hold

Another useful form of a peak detector is a peak and hold. The peak detectors presented earlier in this application note detect the peak locations of the input waveform, but they do not detect the magnitude of the peaks. A peak and hold detector is useful in applications where the ADC is not fast enough to accurately measure the peaks of a waveform.

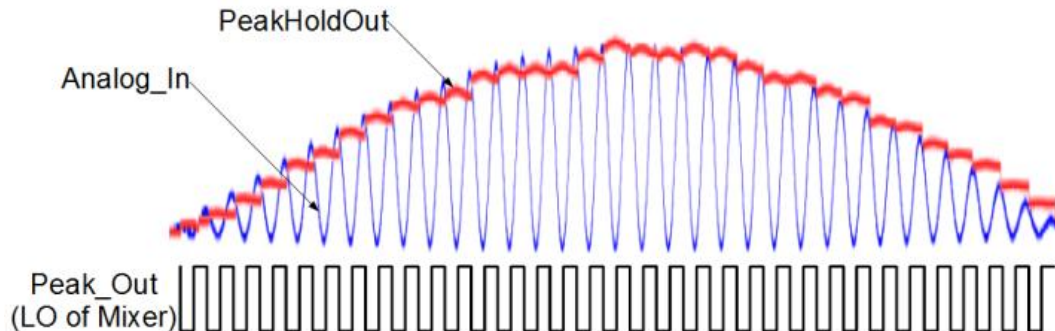
A peak and hold circuit can be created using a peak detector and an additional sample and hold Mixer component. The schematic for a peak and hold is shown in Figure 9.

Figure 9. Peak and Hold Schematic



At every peak from the peak detector component, the original input waveform is sampled by another sample and hold component. Because the output of the sample and hold is held on the falling edge of the LO input clock, each peak is held at the output until the next peak is detected. To create a negative peak and hold, simply invert the output polarity of the peak detector component. The output of the peak and hold circuit is shown in Figure 10.

Figure 10. Peak and Hold Waveform

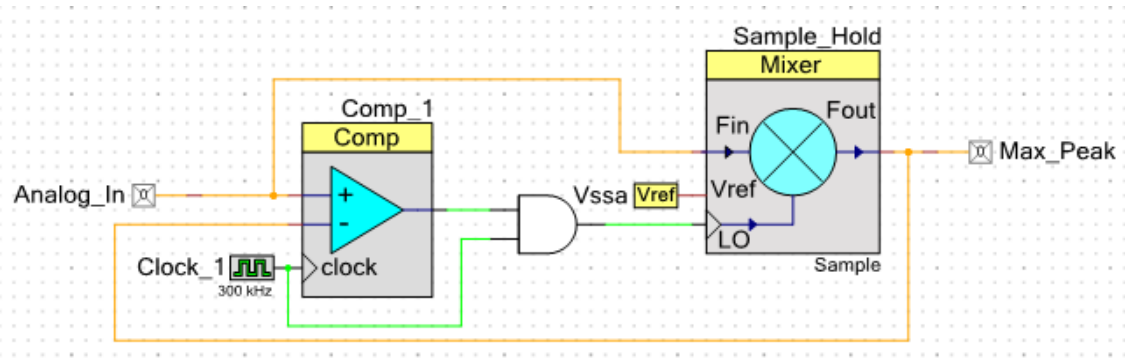


An example project (*C_Peak_Hold_Detector*) is provided in the attached workspace to demonstrate the use of the peak and hold circuit.

5 Maximum Peak Detector

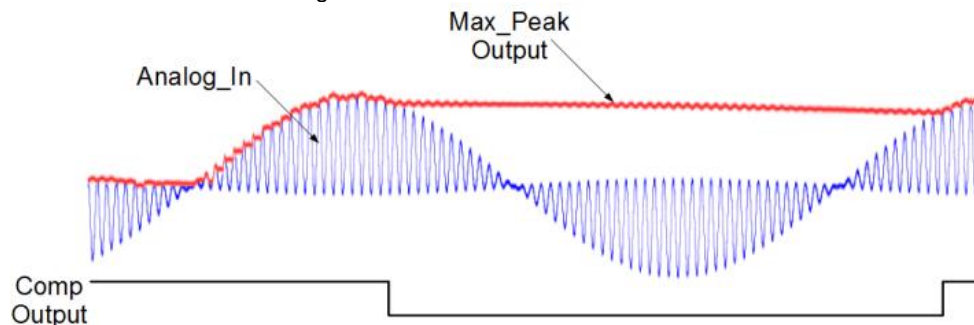
Certain applications require a peak detector that holds the maximum peak of a given input waveform. This can also be created with a comparator and a sample and hold component. The schematic for a maximum peak detector is shown in Figure 11.

Figure 11. Maximum Peak Detector Schematic



With this configuration, the sample and hold component is clocked only if the analog input is greater than the last maximum value held at the output. When the analog input is greater than the last held value, the comparator output asserts and the sample and hold is clocked to update the output to a new maximum value. Comparator hysteresis is not needed for this configuration. Figure 12 shows the output waveform for this peak detector.

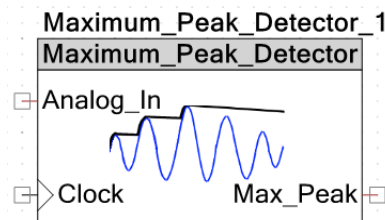
Figure 12. Maximum Peak and Hold Waveform



The output of the sample and hold will decay over time. Refer to the Mixer [datasheet](#) for specifications on this droop voltage. The output of the sample and hold will droop towards the supplied reference voltage for the sample and hold component. By changing your reference to V_{DDA} and inverting the comparator polarity, a minimum peak detector can be created.

For easy reuse, the hardware-based design for the maximum peak detector is encapsulated as a component in a PSoC Creator library project. This component supports both maximum and minimum peak detection. The component symbol is shown in Figure 13.

Figure 13. Maximum Peak Detector Component Symbol



An example project (*D_Maximum_Peak_Detector*) is provided in the attached workspace to demonstrate the use of the maximum peak detector component.

6 Summary

This application note presents three unique methods of peak detection with PSoC 3 and PSoC 5LP. Solutions have been provided to extract the peak timing, slope direction, peak amplitude, and maximum peak amplitude from an input waveform. Peak detection can be useful in a variety of different applications including magnetic card readers, ECG's, detecting the amplitude or timing of analog sensor output signals, and many more useful and interesting applications.

7 Attached Project Summary

Library Project `Peak_Detector_Component.cywrk`:

This library project contains the implementation of two components for easy reuse in other designs.

- `Peak_Detector`: Sample and hold-based peak detection component with digital output.
- `Maximum_Peak_Detector`: Component to detect and hold the maximum peaks of a given waveform.

AN60321-Proj.cywrk:

This workspace contains four example projects to demonstrate the techniques from this application note.

- `A_SH_Peak_Detector`: Demonstrates use of the `Peak_Detector` component.
- `B_SIO_Peak_Detector`: Demonstrates peak detection using an SIO pin.
- `C_Peak_Hold_Detector`: Demonstrates peak and hold implementation using the `Peak_Detector` along with a sample and hold component.
- `D_Maximum_Peak_Detector`: Demonstrates a maximum peak detector using the `Maximum_Peak_Detector` component.

About the Author

Name:	Dan Sweet
Title:	Applications Engineer Staff
Background:	Dan Sweet graduated from Western Washington University with a Bachelor of Science degree in Electrical Engineering Technology.

Document History

Document Title: AN60321 – Peak Detection with PSoC[®] 3 and PSoC 5LP

Document Number: 001-60321

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2899480	DRSW	03/25/2010	New application note
*A	2991597	SRIH	07/22/2010	Fixed branding discrepancies
*B	3154800	DRSW	01/13/2010	Updated for PSoC Creator 1.0. Added note about temporary project warnings.
*C	3451277	DRSW	11/30/2011	Template update Updated projects and components for PSoC Creator 2.0. Fixed typo in About the Author section Updated section covering warnings to inform users the warning will only occur in Creator 1.0, not in 2.0.
*D	3562896	DRSW	03/26/2012	Updated header with author email contact information Added a few common peak detection applications to the summary
*E	3812707	DRSW	11/15/2012	Updated Associated Part Family as "PSoC 3 and PSoC 5LP". Updated Software Version as "PSoC [®] Creator™ 2.1 SP1". Updated Introduction (Minor updates to text). Updated Peak Detector Using Sample and Hold (Minor updates to text). Updated Peak Detector Using an SIO Pin (Minor updates to text). Updated Peak and Hold (Minor updates to text). Updated Maximum Peak Detector (Minor updates to text). Updated Attached Project Summary (Removed section about warnings that occur in Creator 1.0). Replaced PSoC 5 with PSoC 5LP in all instances across the document.
*F	4499748	DRSW	9/11/2014	Updated project and components for PSoC Creator 3.0 SP1.
*G	4755468	DRSW	05/05/2015	Updated project and components for PSoC Creator 3.1 SP2. Removed reference to Legacy PSoC 5 project. Added hyperlinks to mixer component datasheet. Sunset review
*H	5257016	SJLE	05/03/2016	Sunset review Updated template
*I	5703335	AESATMP8	04/20/2017	Updated logo and Copyright.

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6](#)

Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Videos](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

All other trademarks or registered trademarks referenced herein are the property of their respective owners.



Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

© Cypress Semiconductor Corporation, 2010-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.