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Spec No: 001-14734

Spec Title: AN6023 - NONVOLATILE SRAM (NVSRAM) BASICS

Sunset Owner: Ravi Prakash (PSR)

Replaced By: 001-89467

Nonvolatile SRAM (nvSRAM) Basics

Author: Ravi Prakash
Associated Project: No
Associated Part Family: nvSRAMs
Software Version: None
Related Application Notes: None

AN6023 describes the basic operations of a nonvolatile static random access memory (nvSRAM), using a parallel nvSRAM as an example. The same basic operations also apply to the Cypress serial nvSRAMs.

Introduction

A static random access memory (SRAM) loses its content when powered down, and is classified as a volatile memory. The memory is volatile because there is no data when power is restored to the device. Another example of a volatile memory is the dynamic random access memory (DRAM) used in all personal computers and laptops. A memory that retains (does **not** lose) its data without power, is classified as a nonvolatile memory. Examples of nonvolatile memories are nVSRAM and flash memories. This class of memories is used in applications where critical data must be stored after power is removed, or when power is interrupted during operation. Example of power interruptions are hot plugging of cards in servers, industrial computers, and medical equipment. While the equipment is operating, several sub modules can be unplugged (their power interrupted) and new ones plugged in (hot plugged because power is present in the equipment) without loss of any critical data and/or operations to the equipment.

The nvSRAM is a class of nonvolatile memories that combines SRAM interface and speed with nonvolatility. Cypress nvSRAMs do not use batteries or any other energy sources to retain data. The nvSRAM has several advantages in applications where high speed and nonvolatile storage are required at low cost compared to alternative solutions that include large super capacitors and batteries to retain data on devices when power is interrupted. These applications include smart meters, servers, industrial programmable logic controllers (PLCs), gaming, multi-function printers (MFPs), and storage units.

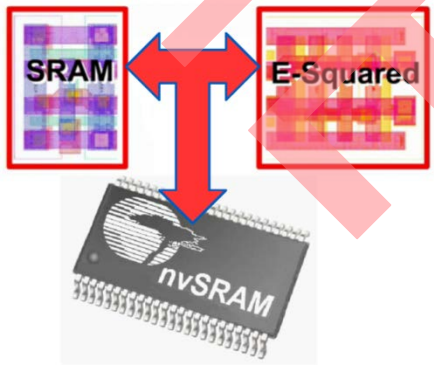
Cypress offers several families of high speed, high performance nvSRAM products that combine the performance characteristics of a high speed SRAM with reliable (over 20 years of data retention) nonvolatile elements. The data is retained in the nonvolatile elements that are integrated with each SRAM cell. While operating as a high speed (< 20 ns access time) SRAM, the nvSRAM can store or recall data to or from the nonvolatile elements. The store and recall can be done either by a user command (firmware) or by the device automatically without a user command. For example, the STORE command stores the SRAM data to the nonvolatile cells and a RECALL command restores the nonvolatile data to the SRAM cells. While using the nvSRAM device in its AutoStore mode, the nvSRAM device transfers the SRAM cell data automatically to the nonvolatile elements during power interruptions using charge from an external capacitor. It then restores the data from nonvolatile elements into the SRAM cells when power is restored to the unit (without the any software intervention).

The nonvolatile elements (also known as shadow EEPROM) guarantee data retention for a minimum of 20 years at the maximum operating temperature.

nvSRAM Cell Architecture

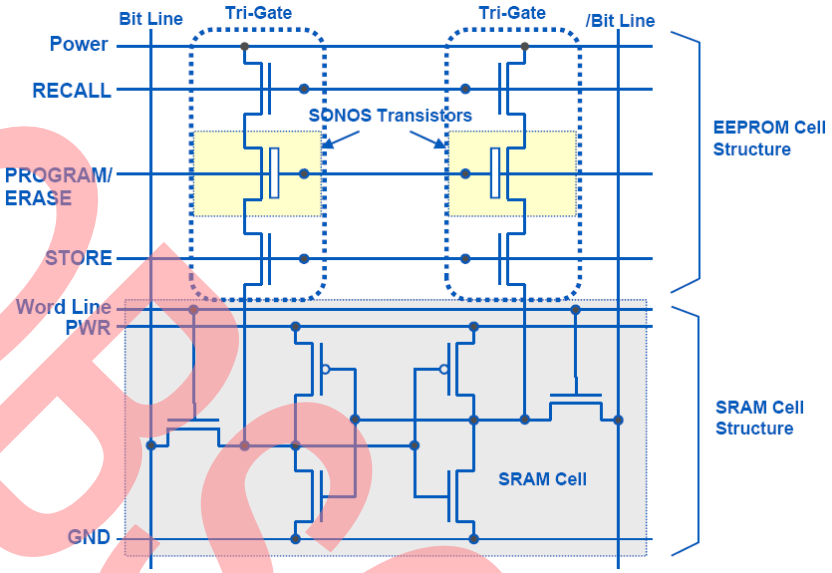
Cypress nvSRAM combines the standard SRAM cells with EEPROM cells in SONOS technology to provide fast read/write access and 20 years data retention without power. The SRAM cells are paired one to one with E-squared cells. Figure 1 shows a representation of the nvSRAM architecture.

Figure 1. nvSRAM Architecture



The nvSRAMs are in CMOS process with the E-squared cells having a SONOS stack to provide nonvolatile store.

Figure 2. nvSRAM Cell Architecture

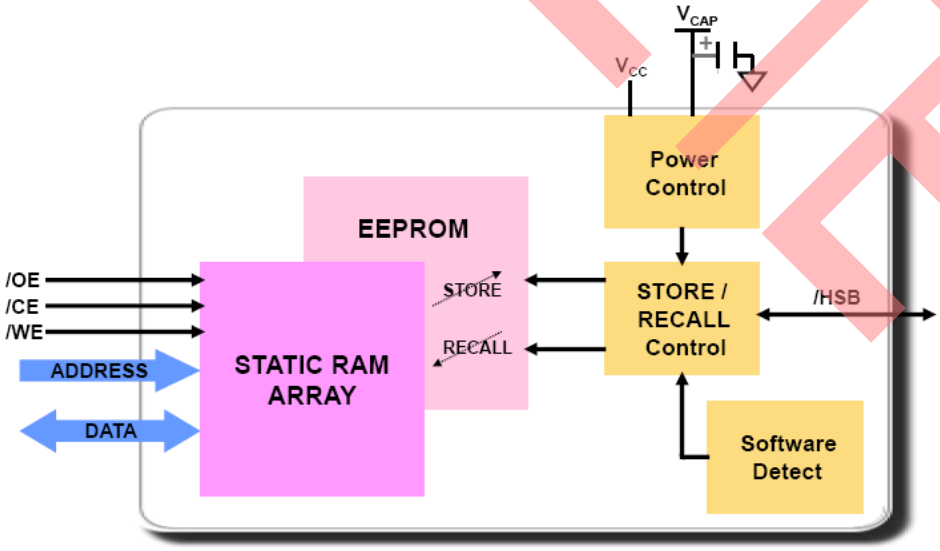


Cypress nvSRAM products feature the SONOS nonvolatile cell that is built upon a standard SRAM cell. When normal power is applied, the device looks and behaves similar to a standard SRAM. However, when power drops out, each cell's contents can be automatically stored into the nonvolatile element that sits on top of each SRAM cell. This nonvolatile element uses standard CMOS process technology to obtain the high performance of standard SRAMs. In addition, the SONOS technology is highly reliable and supports 1 million STORE operations.

Device Interface

The interface to the nvSRAM is identical to the high speed SRAM, except for a few extra pins exclusive to the device. Figure 3 shows the logic block diagram of a parallel interface nvSRAM. The address lines, data lines, and control lines (/OE, /CE, /WE) provide the same interface as a high speed SRAM. For normal Read and Write operations, the nvSRAM is accessed in the same way as an SRAM. The serial nvSRAMs have the same logic blocks as the SRAM except that they have serial interface instead of the parallel interface.

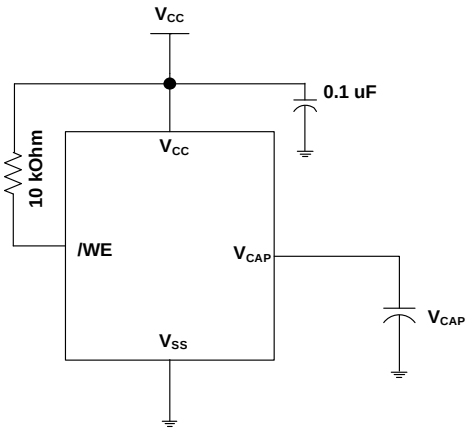
Figure 3. Logic Block Diagram



The Power Control block detects variations on the power supply V_{CC} to trigger an AutoStore operation. The Software Detect Block detects address read sequences for STORE, RECALL, and Enable/Disable AutoStore operations. The STORE/RECALL Control block initiates STORE or RECALL operations, including Hardware Store operation using the /HSB pin. The software sequences required to initiate nonvolatile operations use the standard SRAM control pins. As a result, very few hardware modifications are required to use nvSRAM instead of standard SRAMs.

The only external component required for nvSRAM AutoStore operations is the capacitor connected to the V_{CAP} pin, which is charged to the supply voltage on power up. Charge from this capacitor is used to perform an AutoStore operation (transferring the contents of SRAM to nonvolatile elements on power down) operation. Figure 4 shows the proper connection of the storage capacitor (V_{CAP}) and the recommended pull up on /WE pin. Because controllers take longer to boot up compared to the 20 ms for the nvSRAM, the controller I/Os can be floating when the nvSRAM is ready for read/write. The pull-up on /WE pin prevents any inadvertent writes to the nvSRAM due to the floating controller I/Os.

Figure 4. AutoStore Mode



Nonvolatile STORE Operation

A STORE operation is used to transfer the data in parallel from the SRAM to the nonvolatile SONOS cells. For example, in a 4-Mbit nvSRAM, the data of all the 4M SRAM cells is stored to the 4M EEPROM elements simultaneously. This parallel transfer of data enables the entire SRAM array to be stored in a maximum of 8 ms. The nvSRAM STORE operation can be initiated in three ways: AutoStore, activated on device power down; Software Store, activated by a software read sequence; and Hardware Store, activated by the /HSB pin.

During the STORE cycle, the previous nonvolatile data is first erased, followed by programming of the nonvolatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

The /HSB signal can be monitored by the system to detect if a STORE cycle is in progress. The busy status of nvSRAM is indicated by the /HSB pin being pulled LOW. To reduce unnecessary nonvolatile stores, AutoStore and hardware STORE operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. However, software initiated STORE cycles are performed regardless of whether a write operation has taken place.

AutoStore Operation

In AutoStore operation, data is automatically stored into the EEPROM elements when the system power supply V_{CC} drops below V_{SWITCH} level.

During normal operation, the device draws current from V_{CC} to charge the capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC} and a STORE operation is initiated with power provided by the V_{CAP} capacitor.

Hardware STORE

The /HSB pin is used to request a hardware STORE cycle. When the /HSB pin is driven LOW by the external controller, the nvSRAM conditionally initiates a STORE operation after t_{DELAY}. However, a STORE cycle begins only if a write to the SRAM has taken place since the last STORE or RECALL cycle. The t_{DELAY} time allows completing any write operation that is in progress. The /HSB pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition, when the STORE (initiated by any means) is in progress.

During any STORE operation, regardless of how it is initiated, the nvSRAM continues to drive the /HSB pin LOW, releasing it only when the STORE is complete. When the STORE operation is complete, the nvSRAM remains disabled until the /HSB pin returns HIGH. Leave the /HSB pin unconnected if it is not used.

Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The software STORE cycle is initiated by executing sequential /CE or /OE controlled read cycles from six specific address locations in exact order. During the STORE cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Nonvolatile RECALL Operation

A RECALL operation copies data from EEPROM to SRAM, in parallel, at a maximum of 20 ms. The RECALL cycle can be initiated by the following two methods:

Power Up RECALL

During power-up or after any low power condition (V_{CC}< V_{SWITCH}), an internal RECALL request is latched. When V_{CC} again exceeds the V_{SWITCH} on power-up, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete. During this time, the /HSB pin is driven LOW by the /HSB driver and all reads and writes to nvSRAM are inhibited.

Software RECALL

A Software RECALL operation is initiated in a similar manner as a Software STORE operation. This is done by reading a specific sequence of six address locations, with no access to other locations in between.

nvSRAM during Nonvolatile Operations

During STORE and RECALL operations, the nvSRAM is not available to the system. All levels and transitions on the input pins are ignored and all data pins are tristated (except the /HSB pin). After the nonvolatile cycle (Software STORE/Software RECALL) is completed, a READ or WRITE cycle can be initiated immediately by proper assertion of the control signals.

The /HSB pin indicates when a nonvolatile STORE is in progress. This pin is internally driven LOW whenever a nonvolatile STORE is in progress.

If the /HSB pin is connected to any other device in the system, a pull-up resistor to V_{CC} must be used on the /HSB line. A weak internal pull-up resistor keeps this pin HIGH, if an external pull-up is not connected (optional). The value of the pull-up resistor must be selected so that it does not overpower the internal pull-down driver on /HSB. Typically, a 10 kΩ pull up is sufficient.

Protection against Inadvertent STOREs

Cypress nvSRAM has several built in measures to prevent inadvertent STORE operations. User initiated STORE operations are not allowed if V_{CC} is below V_{SWITCH}. This ensures that STOREs initiated by /HSB and software sequences are not started if V_{CC} is too low to allow successful completion.

Hardware STORE and AutoStore operations require that at least one WRITE operation takes place since the last nonvolatile operation. This feature ensures that a fluctuation on the supply line or noise on the /HSB line does not initiate a second unnecessary STORE operation.

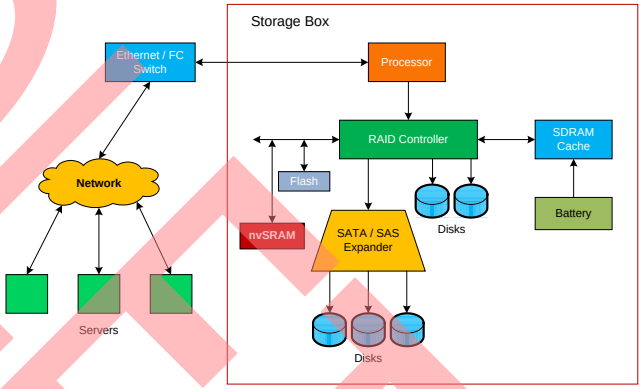
nvSRAM Applications

Cypress nvSRAMs are ideally suited for all applications that require fast access, high reliability, and unlimited endurance. These applications include write journaling in RAID storage systems, smart meters, industrial programmable logic controllers (PLCs), gaming, and multi-function printers (MFPs). The following are a couple of use cases.

Write Journaling in RAID Systems

Figure 5 presents a generic RAID storage system architecture. The servers connected on the network send the data to a switch, which directs it to different storage boxes. The processor in the storage box also interacts with multiple storage boxes through the switch to enable virtualization. The data received by the processor is sent to the RAID controller.

Figure 5. RAID Storage Architecture



The RAID controller has direct access to the cache memory that enables fast read/write access to the storage system. The cache is used to write the data in transition. The RAID system uses a cache to speed up the apparent I/O performance of the storage system so that the host processor is not kept busy. In modern RAID systems, the size of these cache memories is very large (SDRAMs).

The write access from the host is acknowledged as soon as the data is received and stored in the cache. Because the disk drive access is not required, the throughput of a write operation increases significantly. The data is transferred from the cache to the disk drives by the RAID controller in the background. This operation is transparent to the host, which assumes that the write operation is complete as soon as it receives an acknowledgement from the RAID controller

Although this approach significantly increases write performance, the actual data transfer to the disks is transparent to the host. This raises a potential risk to the

data integrity in case a power failure occurs after the host is acknowledged, but before the data is committed to the disk. A write journal based system is effective in recovering data from power losses.

The data stored is usually secured using a battery backed cache that retains the contents of the cache even during power failure. On the next power up, the storage system has to track back each transaction to find which blocks of data were not written into the physical drives. Therefore, even with battery backed cache, the system recovery time may be high as the system needs to be checked for the exact failing point before recovery can begin.

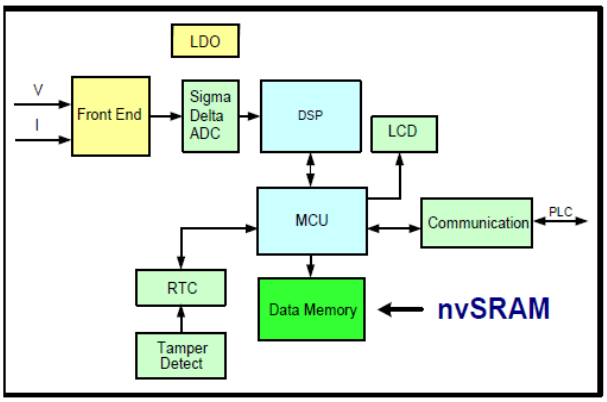
To avoid recovery delays, many storage systems log each transaction of data from the host to the cache and from the cache to the disk in a nonvolatile circular buffer. When the power goes off, this log can be played back to precisely identify the state of the storage system before failure. This strategy is called write-in-progress record or 'Write Journaling'.

nvSRAM is the preferred NV solution for write journaling because it is the fastest nonvolatile RAM. It also has proven reliability due to its SONOS architecture and has unlimited read write endurance.

Smart Meters

Solid state electricity meters primarily provide energy or power measurement and data display. They may also require a battery operation to support features such as reading without power when the product is not connected to a power main. As implementation and architecture becomes more sophisticated, electricity meters demand additional processing power, larger flash memories for software stacks to support communication protocols, and larger nonvolatile memories for data logging and remote firmware updates. Smart meters offer additional functionality to energy meters including real-time or near real-time reads, power outage notification, and power quality monitoring. They allow price setting agencies to introduce different prices for consumption based on the time of day and season. These price differences help bring down peaks in demand (load shifting or peak lopping), thus reducing the need for additional power plants. Another type of smart meter uses nonintrusive load monitoring to automatically determine the number and type of appliances in a residence, how much energy each uses and when. Electric utilities use this meter to do surveys on energy use. Figure 6 shows a typical block diagram of an energy meter.

Figure 6. Advanced Energy Meter Block Diagram



The serial nvSRAM offers industry standard SPI interface with up to 104 MHz speed. Data write and read to the nvSRAM cells happen at the speed of the processor bus. This allows controllers to write into nvSRAM cells directly rather than storing first into an on-chip SRAM buffer and then transferring to external memory such as EEPROM or flash due to its slow page based access. Also, the nvSRAMs take away the huge burden of wear leveling required for the EEPROMs.

The serial nvSRAMs are available in the industry standard 8-SOIC package and have proven high reliability based on the standard SONOS process.

Summary

Cypress parallel nvSRAMs offer the functionality of fast asynchronous SRAMs with the feature of nonvolatility. Cypress nvSRAMs retain data using integral EEPROM providing high reliability. A small external capacitor (V_{CAP}) is used to transfer the contents of SRAM to nonvolatile elements on power down, which eliminates the use of battery. The nvSRAMs have the same address, data, and control interface as an asynchronous SRAM; this simplifies interfacing and designing using the device. Other features are also added to the device internally to help applications reduce component count in their system. For example, some nVSRAMs are equipped with a real time clock (RTC) hence replacing components in many applications requiring nvSRAM and RTC. In addition, Cypress serial interface nvSRAMs provide industry standard I^2C and SPI interfaces enabling low pin count applications with high speed serial interface. Refer application notes AN61546, AN64574 and AN74875 for more information on RTC, SPI and I^2C nvSRAM.

Table 1 lists the nvSRAM features and parameters.

Appendix A

Table 1. nvSRAM Features and Parameters

Note No.	Feature/Parameter[1]		Specification (0.13 μμ τεχηνολογψ)
1	V_{CC}	Parallel interface	5 V, 3 V, separate I/O (1.8 V)
		Serial interface	5 V, 3 V, 2.5 V
2	Device interface		Parallel, x8/x16
			Serial – I^2C
			Serial - SPI
3	Speed	Parallel interface	20 ns access time
		Serial – I^2C	3.4 MHz
		Serial - SPI	104 MHz
4	Density	Parallel interface	Up to 8 Mbit
		Serial interface	Up to 1 Mbit
5	Low voltage trigger level (V_{SWITCH})	3 V	2.65 V
		5 V	4.4 V
		2.5 V	2.35 V
6	Software functions: STORE, RECALL, AutoStore Enable/Disable	Parallel interface	6 address software sequences
		Serial interface	Opcodes
7	RTC	Parallel interface	Available
		Serial interface	Available
8	STORE cycle duration		8 ms
9	Power up RECALL ($t_{HRECALL}$)	V_{CC} = 3 V, 5 V	20 ms
		V_{CC} = 2.5 V	40 ms
10	Software RECALL (t_{RECALL})	Parallel interface	200 μσ
		Serial interface	600 μσ
11	Time allowed to complete SRAM Write Cycle (t_{DELAY})		25 ns
12	SLEEP	Parallel interface	Not available
		Serial interface	Available
13	Time to enter sleep mode after issuing SLEEP instruction (serial parts only)		8 ms
14	Time for nvSRAM to wake up from sleep mode (serial parts only)	V_{CC} = 3 V, 5 V	20 ms
		V_{CC} = 2.5 V	40 ms
15	Endurance	SRAM read/write	Infinite
		NV STORE	1 million cycles
16	Data retention		20 years at 85 °C
17	Parts		See http://www.cypress.com/?id=65&source=header for the complete list of parts

Note 1 This table is intended to be illustrative. For more information, see the individual device datasheets.

Document History

Document Title: AN6023 - Nonvolatile SRAM (nvSRAM) Basics

Document Number: 001-14734

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1778687	SHOR	11/28/2007	New application note.
*A	2662643	NXR	02/20/2009	Content updates. Added Appendix to list the differences in features/parameters across technology. Changed title to “Nonvolatile SRAM (nvSRAM) Basics”.
*B	2802536	GVCH	11/09/2009	Table 1: Added CY14B256LA, CY14B256KA, CY14E256LA, CY14B108K, and CY14B108M to 0.13 m column.
*C	3338083	PSR	08/05/2011	Added nvSRAM Cell Architecture and nvSRAM Applications sections. Content updates throughout the document.
*D	3707951	GVCH	08/09/2012	Added more clarity to the content and updated Figure 5.
*E	4168504	GVCH	10/21/2013	Obsolete document.

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