AN6022

A Comparison between nvSRAMs and BBSRAMs

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AN6022 describes the comparison of features, capabilities, and benefits between Cypress nvSRAM and BBSRAMs.

Introduction

With lead-free initiatives being implemented globally, nvSRAMs have become a popular choice for NV RAM selection. This application note explores the advantages of nvSRAM over battery backed SRAM (BBSRAM). It provides a comparison of features, capabilities, and benefits between Cypress's nvSRAM and the BBSRAM technology from other manufacturers.

What is BBSRAM?

BBSRAM, sometimes referred to as BatRAMs, have a combination of multiple chips and battery elements embedded in a single package. The battery can be integrated inside the package as done in plastic DIPS. It can also be housed on top of the package and then mechanically attached with a covering such as those used in a SOIC. The BBSRAM is accessed similar to any other SRAM. When the supply voltage (V_{CC}) dips below a specified level, the internal battery is switched on to sustain the contents in the memory until V_{CC} returns to a valid condition.

What is nvSRAM?

The Cypress nvSRAM is a fast static RAM (SRAM), with a non-volatile element in each memory cell. The embedded non-volatile elements incorporate SONOS technology, producing the world's most reliable non-volatile memory. The SRAM provides infinite read and write cycles, while independent non-volatile data resides in the highly reliable SONOS cell. Data transfers from the SRAM to the non-volatile elements (AutoStore operation) takes place automatically at power-down using charge from a small capacitor connected to VCAP pin. On power-up, data is restored to the SRAM (Power-Up RECALL operation) from the non-volatile memory. Both the STORE and RECALL operations are also available under software control.

Benefits of nvSRAM

The nvSRAM is a single monolithic solution with a small external capacitor when compared to a multiple component solution. Therefore, it has many benefits when compared to a BBSRAM solution.

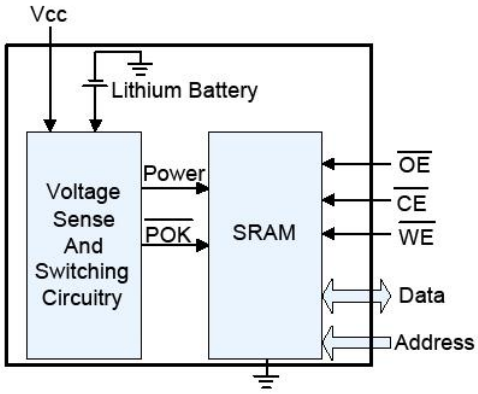
Table 1. Benefits of nvSRAM

nvSRAM Benefits	Description
Lower cost	Single monolithic solutions have lower manufacturing costs than multiple component solutions. The nvSRAM also eliminates the need for a battery, thus reducing costs further.
Higher reliability	Batteries have limited usage. In addition, for external battery packaging, corrosion and failing snappacks (external hardware used to hold the battery in place) contribute to lower reliability.
Smaller board space and lower height	BBSRAMs are significantly taller and larger than the nvSRAM because the battery is encased or attached to the package.
Improved manufacturing	The nvSRAM results in better manufacturing because battery inventory need not be tracked and there is no worry about the "shelf life" of the battery inventory.
RoHS compliance	With no battery, the nvSRAM is RoHS compliant, while the BBSRAM is not.
Higher performance	The access time for BBSRAMs are between 70 ns and 100 ns. The nvSRAM is specified at 20 ns to 45 ns access times.

Inside the BBSRAM

A BBSRAM includes three major components: a standard SRAM, a voltage sensor and switch chip, and a Lithium battery. Each BBSRAM module has a self-contained lithium energy source and control circuitry which constantly monitors VCC for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing. Figure 1 shows the block diagram of BBSRAMs.

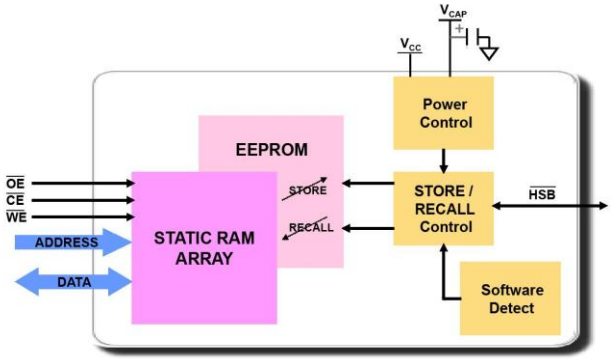
Figure 1. BBSRAM Block Diagram



Inside the nvSRAM

The nvSRAM technology is a combination of SRAM and EEPROM technologies on the same die. A nonvolatile EEPROM element is incorporated in each SRAM cell. In the SRAM mode, the memory operates as an ordinary static RAM, at SRAM speeds. In the nonvolatile mode, SRAM data is transferred or recalled in parallel to and from the EEPROM. The EEPROM is manufactured in a SONOS (Silicon-Oxide-Nitride-Oxide-Silicon), providing high yields and requires fewer masks than floating gate process technologies. Other key advantages of the SONOS technology are mature design and manufacturing processes, good integrability with CMOS micrologic, and low power consumption. The user data has an unlimited number of writes because it writes to a standard SRAM. The number of storage cycles in the EEPROM can be modified over 1 million times during the product's lifetime. No battery is required to transfer data; it occurs automatically during a power down cycle as the required power to perform a transfer from the SRAM to EEPROM is supplied by an external capacitor. nvSRAM is used also in combination with clock logic to create nonvolatile RTC components. Figure 2 shows a block diagram of the nvSRAM.

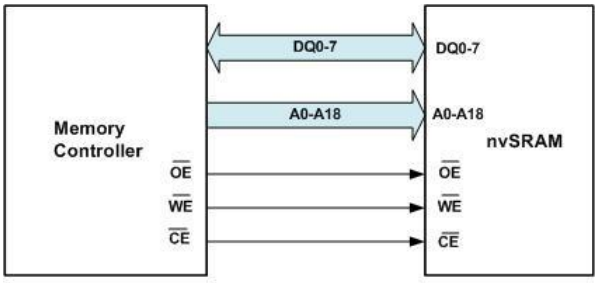
Figure 2. nvSRAM Block Diagram



Typical nvSRAM Connection with Memory Controller

Under normal operating conditions, read or write operations are functionally identical to a standalone SRAM. Using parallel I/O structure, user can easily store data or fetch data from any memory location defined by the address bits setting. Subsequent memory cycle can occur at this or any other location in any order with no write cycle count restrictions and no additional support circuitry is required for microprocessor interfacing.

Figure 3. Typical nvSRAM Connection



When V_{CC} drops below a threshold value (V_{SWITCH}), the Cypress nvSRAM enters into AutoStore mode and prohibits any READ/WRITE operation on the device by pulling DQ bus to high impedance state and ignoring all the transitions on its address and control lines.

Comparison of Technical Performance Characteristics

Along with the business benefits, nvSRAMs have many technical advantages over BBSRAMs. These include:

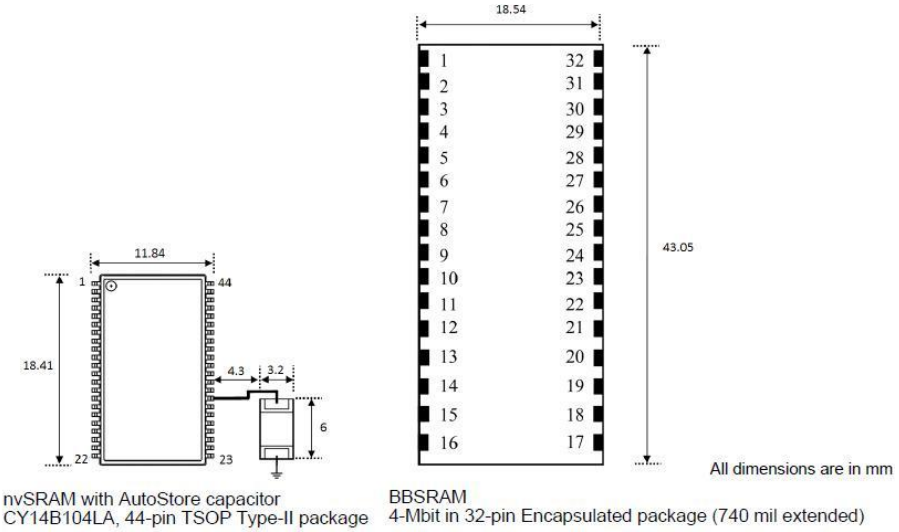
- Data retention and product lifetime — Data retention time is a specification on how long data can be stored before the data storage begins to deteriorate. Product lifetime refers to how long the device is operational after it is manufactured.
- Performance
- Device functionality on power up — Functionally, the power up requirements of the nvSRAM and BBSRAM are similar:
  - The nvSRAM automatically transfers data from the EEPROM to the SRAM
  - A BBSRAM automatically switches from the lithium source to the V_{CC} supply
- Board space

Table 2. Technical Comparison between BBSRAM and nvSRAM

BBSRAM	nvSRAM
Data Retention and Product Lifetime	
■ BBSRAM ceases to function as nonvolatile memory after the battery loses its charge, typically 4 to 7 years in commercial systems. ■ Battery lifetime is reduced by two major factors: ▫ Current drain from memory circuits - This depends on the current requirements of the memory and is the predominant factor in determining lifetime at room temperature. ▫ Evaporation of electrolyte - At 70 °C, the rate of evaporation is such that disconnection of the battery from the memory does not extend its life. At 85 °C, the battery typically lasts no more than two years, even if the device was never powered up. ■ The battery's ability to sustain current is also reduced at low temperature. ■ The battery's ability to supply current is degraded by 20% at –40 °C by much the same mechanism that makes the chemistry of a car battery inefficient at low temperature. ■ Uncontrolled power down sequences has detrimental effects on battery life. In particular, V_{CC} undershoots due to ringing on power down can cause current to be drawn from the battery. Further, if $\overline{CE}$ is not maintained high during power down, an inadvertent read or write may occur. The full current requirement of these cycles reduces battery life.	■ Data retention of 20 years and 1 million STORE operations are guaranteed on the nvSRAM. ■ The nonvolatile memory element in an nvSRAM is an EEPROM cell. This cell consists of a nitride insulator and a thin oxide insulator placed between a conductor and the silicon surface. The programming charge is stored in the nitride insulator. Injection of a charge into the nitride is controlled by the electric field between the conductors. ■ Data retention is determined by the insulator's ability to hold this charge. As the cell is cycled or the temperature increased, the insulator permits more charge to leak. The data retention of an nvSRAM is determined by the storage temperature of the device and the number of STORE operations performed. ■ All Cypress nvSRAM devices are tested with a temperature acceleration factor that guarantees the full retention specification on the last specified STORE cycle when maintained at maximum operating temperature.
Performance	
■ Battery backed devices must optimize the standby power consumption to maximize retention and sacrifice access time in the process. ■ The fastest 4 Mb BBRAMs have 70 ns to 100 ns access times.	■ The SRAM portion of a nvSRAM is identical to a standard SRAM using an industry standard 6T cell. Hence, the performance specifications are similar to standard SRAMs, with current access times in 20 ns through 45 ns.

BBSRAM	nvSRAM
Device Functionality on Power Up	
■ Chip Enable ($\overline{CE}$), must be maintained high for at least 125 ms after power up. While $\overline{CE}$ is high, the chip cannot be read or written.	■ There is no special requirement on $\overline{CE}$ during power up. Data is available 20 ms after V_{CC} reaches V_{SWITCH} on power up.
Device Functionality on Power Down	
■ V_{CC} must drop from 3.0 V (depending on the device) to 0 V in 150 µs. The system requires a power supply slew rate which meets this specification.	■ When the nvSRAM recognizes V_{CC} drop below the threshold voltage V_{SWITCH}, it automatically transfers the SRAM contents into EEPROM.
Board Space	
■ Systems implementing batteries must sacrifice board space in height or width to accommodate the battery. ■ Typical packaging ranges from 9 mm × 15 mm to 18.5 mm × 43 mm. ■ BBSRAM manufacturers have recently introduced smaller surface mount packages, but these require an additional snap-on hand assembly for the battery. This mechanical and electrical interface has proven to affect manufacturers who require very low PPM requirements.	■ Cypress's nvSRAM is available in SOIC, SSOP, FBGA and TSOP Type-II packages allowing the nvSRAM to be substituted for BBSRAM without increasing board space. Figure 4 shows the package comparison and board space saving of 67%.

Figure 4. Board Space Comparison between Cypress nvSRAM and BBSRAM



Summary

nvSRAMs have a clear edge over the BBSRAM devices with respect to data retention, access times and package size. For systems requiring almost infinite endurance, high data retention and high-speed access to data stored in the memory, nvSRAMs are a great fit.

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1770467	PSR	11/27/2007	New application note
*A	2677485	NXR	03/23/09	Updated Comparison of Technical Performance Characteristics (Extensive updates to content in the section).
*B	3337067	GVCH	08/04/2011	Updated What is nvSRAM? (Updated the contents in the section). Updated Inside the BBSRAM (No updates in the content, updated only Figure 1 in the section). Updated Inside the nvSRAM (Updated the contents and also Figure 2 in the section). Included the section Typical nvSRAM Connection with Memory Controller. Updated Comparison of Technical Performance Characteristics (No updates in the content, updated only Table 2 in the section). Updated to new template.
*C	3754949	GVCH	09/26/2012	Updated Benefits of nvSRAM (Rephrased description). Added Summary. Updated to new template.
*D	4566270	GVCH	11/12/2014	Removed reference of AN6023 as the application note is obsolete. Completing Sunset Review.
*E	5857709	HARA	08/18/2017	Updated logo and copyright.

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