Please note that Cypress is an Infineon Technologies Company.
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

THIS SPEC IS OBSOLETE

Spec No: 001-14655

Spec Title: IBIS4-14000 FREQUENTLY ASKED QUESTIONS - AN6020

Sunset Owner: Evelyn Beard (EYB)

Replaced by: None

IBIS4-14000 Frequently Asked Questions - AN6020

Table of Contents

1. Why do some sensors have dark rows that move in correlation with the integration time?

This phenomenon is visible when there is a defect row in the pixel array. The reset or readout of a defect row can disturb the reset or readout of the other row (both Y shift-registers select a different row simultaneously; the difference between these rows is the integration time). The reset or readout of a defect line draws more current in the columns as expected and this disturbs the readout or reset of the other line.

Figure 1. Defect Line Moves in Correlation with the Integration Time

Figure 1 shows an image taken with an integration time of 1000 lines. The defect line 3422 (in the middle) can be seen at location 2422 and 4422. Note that these images were amplified heavily to make the effect more visible.

The moving line problem can be solved by not reading out the defect line. This can be done by reading out the line before the defect line twice (suppressing of the CLK_YL pulse). When the line before the defect is readout twice, two succeeding CLK_YL pulses should be asserted. This way, the defect line is skipped and shall not influence the reset voltage of the row that is currently being reset.

Figure 2 shows the timing that should be used when a line is defect. The timing assumes that the third line is defect.

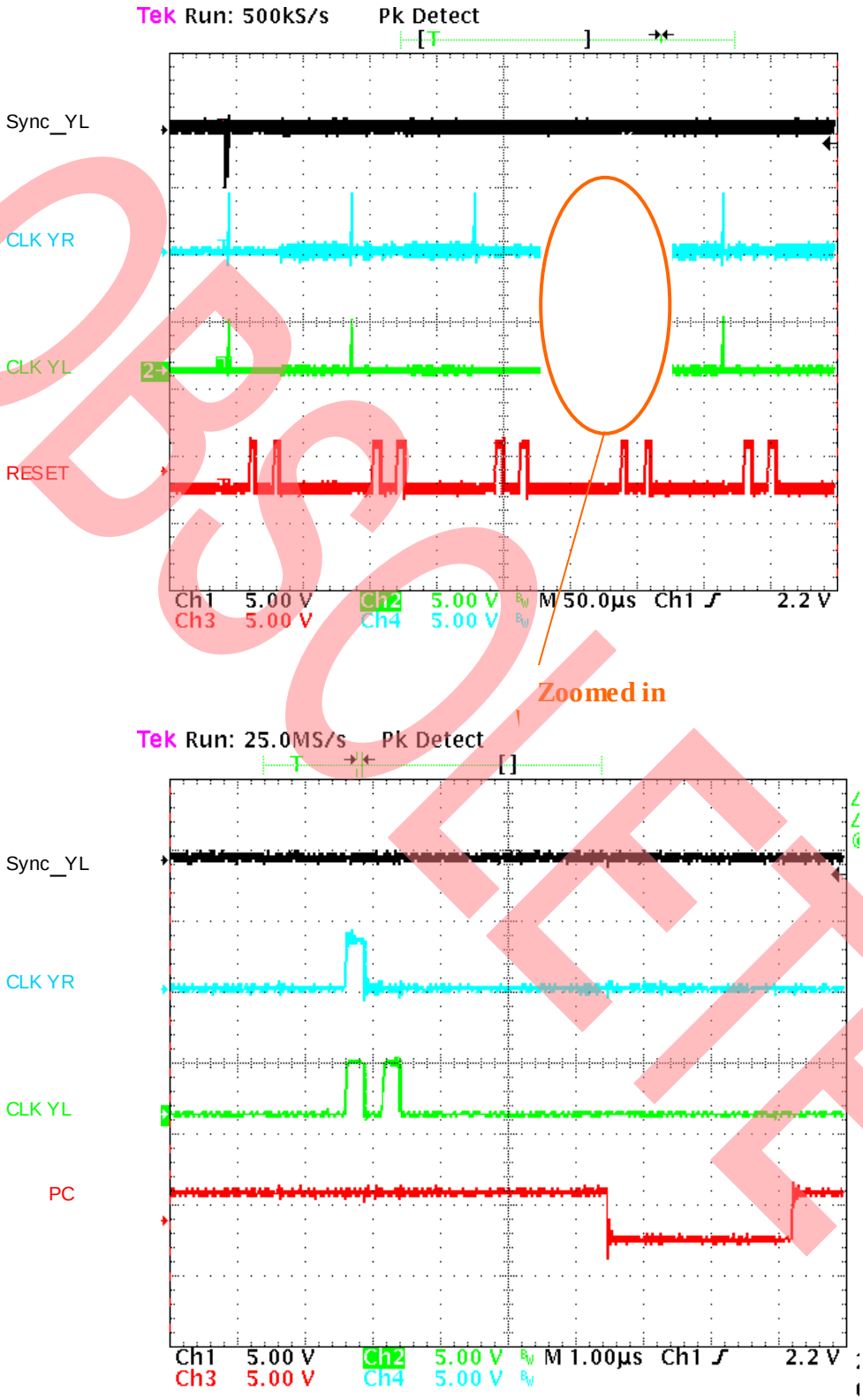


Figure 2. Modified Timing; in this case line 3 is defect and skipped

Figure 3 shows the full line readout sequence with the modified timing. The row before the defect is readout twice (CLK_YL is suppressed). Two CLK_YL pulses after the same line has been readout will skip the defect line.

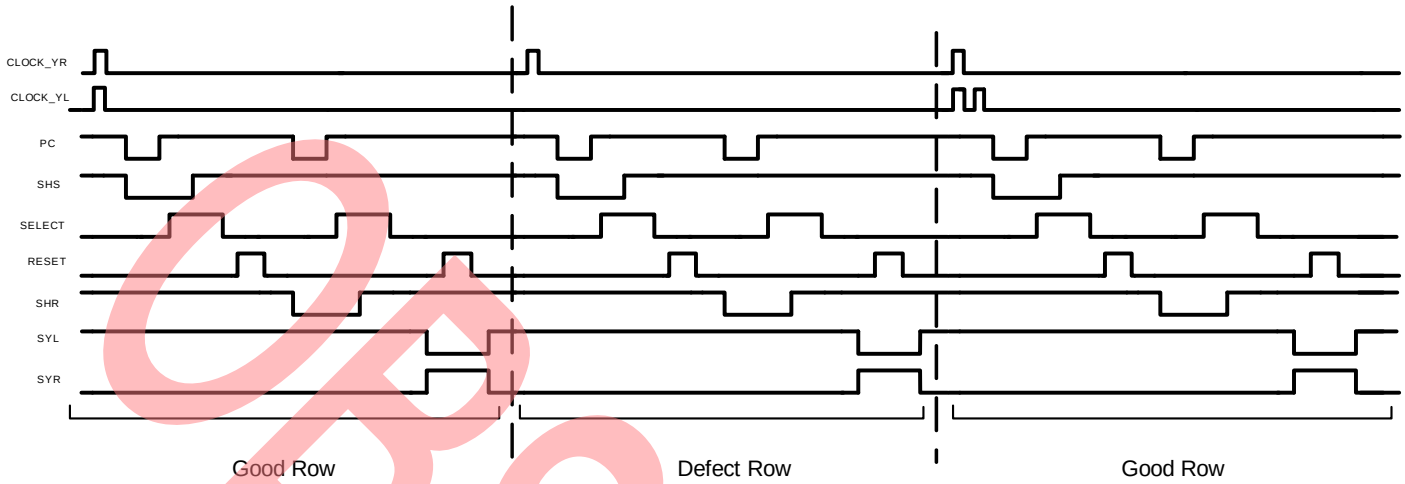


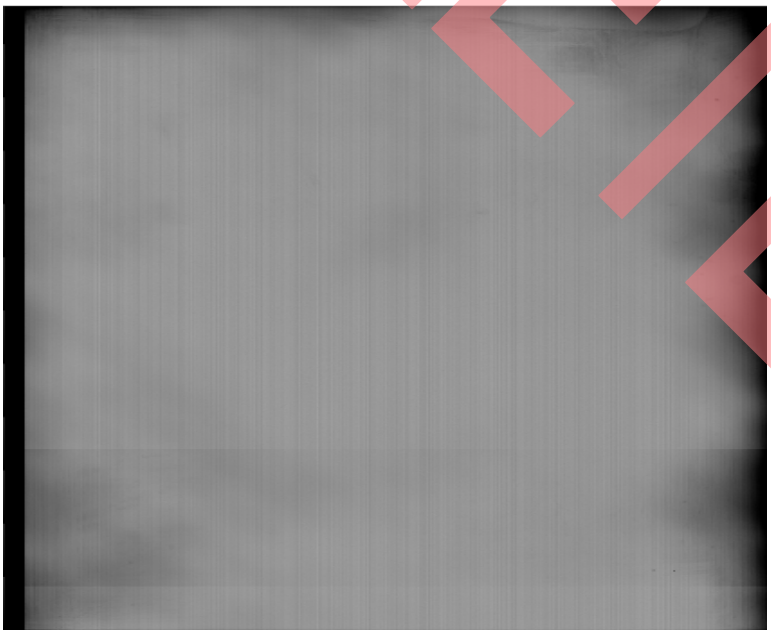
Figure 3. Modified Line Readout Sequence

2. Are the pixels more sensitive in sub-sample mode than in full resolution?

When Y-sub sampling is enabled, certain rows will not be readout and reset. These lines will saturate. As a consequence, some of the generated electrons will not be picked up by the saturated pixel but by the neighboring pixels. This problem can be solved by asserting extra CLK_Y and RESET pulses, to quickly reset the unwanted lines, instead of using the Y sub sample modes.

3. What is the cause of the banding in the image?

The banding is caused when vertical blanking is used to increase the integration time (delaying the assertion of SYNC_Y). When one of the Y-shift register points to the end of the image array, a SYNC_Y pulse will reset this shift register. If SYNC_Y is not asserted, the Y-shift register will be clocked out of the array while the other Y-shift register is still within the pixel array. This causes a voltage offset in the pixel. Both Y-shift registers should always be pointing in the array to eliminate this effect. When integration times longer than the frame readout time are required, one should apply horizontal blanking, i.e., program additional delay times at the end of each row. It is very important that the SYNC_Y and Y_CLOCK pulses are always asserted with the same interval.



4. What is the cause of the gray shades visible in a white to black transition

Note: this effect is only visible when the image is amplified.

The resistance of the NMOS switches increases for larger signals (smaller Vgs). When VDD = 3.3V this resistance is too high, which causes a gray shade in the black pixel when this is proceeded by a white pixel.

There are 2 solutions:

5. Increase VDD to 4V—this will lower the resistance of the NMOS switches (increases Vgs). This is, however, not recommended, since this will decrease the lifetime of the image sensor.
6. Decrease VDDR to 3.3V—this will lower the signal swing, causing a decrease of the resistance of the NMOS switches (increases Vgs). This decrease in signal swing can be neglected because the image is amplified (or else the effect would not have been visible) and thus the full signal swing is never used.

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone: 408-943-2600
Fax: 408-943-4730
http://www.cypress.com