AN6017

Differences in Implementation of 65 nm QDR™ II/DDR II and QDR II+/DDR II+ Memory Interfaces

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The differences between the 65 nm QDR II/DDR II and QDR II+/DDR II+ devices are explained in this Application Note. It also contains guidelines on how to design for both.

Introduction

Memory devices are evolving to match the needs of applications which are in continuous demand like higher performance communications, networking, and digital signal processing (DSP) systems. Specialized memory products that optimize memory bandwidth for a specific system architecture are successful in increasing the overall performance in a variety of data processing systems. Operating speeds have increased beyond 400 MHz. The generation of the 65 nm QDR family of SRAMs released by the QDR consortium meets these requirements. The QDR II+ and DDR II+ products offers improved speeds up to 50 percent faster than the existing QDR II and DDR II products. QDR II+ and DDR II+ products deliver a higher bandwidth than QDR II and DDR II respectively up to 80 Gbps, while using the same footprints and a 165-pin fine-pitch ball gate array (FBGA) package. The QDR II+/DDR II+ architecture leverages the existing infrastructure to create higher performing products and allow a direct transition to higher frequencies.

The QDR and DDR family of SRAM provides designers with a complete memory solution for almost any network application. The QDR II/QDR II+ devices have two ports operating independently at twice the selected clock rate, allowing a transfer of four data words across the two ports in a single clock cycle. The DDR II/DDR II+ devices allow double data rate transfers over a common IO data bus.

This application note contains information on the differences between the 65 nm QDR II/DDR II and QDR II+/DDR II+ devices and contains guidelines on how to design for both. For specific design guidelines on the QDRII/DDRII family of SRAMs, refer to the *Application Note*, QDR™-II, QDR-II+, DDR-II, and DDR-II+ Design Guide - AN4065.

- Description of the QDR II+/DDR II+ SRAM devices
- Differences between QDR II/DDR II and QDR II+/DDR II+ functionality and timing
- Design changes required to accommodate both QDR II/DDR II and QDR II+/DDR II+ SRAM Devices

Description of QDR II+/DDR II+ SRAM Devices

Cypress, along with the other QDR consortium members, defined the 65 nm QDR II+/DDR II+ SRAM devices architecture for high performance communications systems supporting up to 550 MHz frequencies. The QDR II+/DDR II+ SRAM devices are an extension of the existing QDRII/DDRII family of SRAMs in terms of frequency and performance.

The QDR II+/DDR II+ SRAM devices are similar in functionality to a QDR II/DDR II SRAM. The timing of the QDR II+/DDR II+ devices is slightly different from the QDR II/DDR II devices. However with similar functionality and only a few software changes to the host controller and a few modifications to the board, both of these parts can be used interchangeably depending on the application. Designing to both QDR II/DDR II and QDR II+/DDR II+ paves the path for higher performance in the existing QDRII/DDRII designs.

Differences between QDR II/DDR II and QDR II+/DDR II+ Functionality and Timing

Functionally, the QDR II/DDR II and the QDR II+/DDR II+ devices are the same. However, they have certain differences in AC and DC parameters due to the higher speeds of operation in QDR II+/DDR II+ devices.

The major changes are:

- Higher read latency enables achieving higher frequency of operation.
- The QDR II/DDR II has a latency of 1.5 cycles and the QDR II+/DDR II+ supports both 2.0 and 2.5 cycle latencies

  (Note: the latency is not user selectable within a device. Devices with different latencies have different part numbers.)
- Output clocks C and $\overline{C}$ are removed: At high speeds (above 200 MHz), CQ clocks are recommended to latch data. In this case, it is not required for the customer to implement the C clocks.
- QVLD pin: For easier board design, an output valid indicator (QVLD) pin is added. The QVLD is edge aligned to the echo clonks and is issued half a cycle prior to the valid output data.
- Linear Burst Addressing is removed: In DDRII, there is a feature “Linear Burst addressing” which is used to select between the banks for complete flexibility. In DDR II+, this feature is removed as it is not possible to meet the higher speeds with this feature enabled.
- Improved Signal Integrity: In the 65 nm technology node, the QDR II+/DDR II+ devices are offered in two flavors; ODT enabled and ODT disabled (without ODT) devices. The ODT enabled devices have on-die termination for inputs such as data inputs, byte write signals, and input clocks (K/Kb). On-die termination improves signal integrity because It eliminates the need for external termination resistors thereby simplifies board routing, reduces the cost, board area and power consumed by external resistors. For more details regarding on-die termination, see the application note *On-Die Termination for QDRII+/DDRII+ SRAMs - AN42468.*
- Pinout changes: In the QDR II/DDR II devices, the pins P6 and R6 are used as C and $\overline{C}$ clocks. In ODT disabled QDR II+/DDR II+, the P6 is used as the QVLD pin and R6 is a No connect (NC) and in ODT enabled QDR II+/DDR II+, the P6 is used as the QVLD pin and R6 is an ODT. In DDR II+, since the linear burst addressing is not supported, the pins A0 and A1 are NCs.
- Miscellaneous:
  - The tKH$\overline{K}$ H (K clock rising edge to $\overline{K}$ clock rising edge) parameter is modified to be 42.5% from 45% of the input clock cycle.

A summary of all the differences is listed in the following table. For more information on the AC timing and DC parameters, refer to the datasheets of the respective devices.

Table 1. Differences between QDR II/DDR II and QDR II+/DDR II+

	QDR II / DDR II	QDR II+ / DDR II+	Remark
Frequency - 65 nm technology devices	120 MHz~333 MHz	120 MHz~550 MHz	Burst of 2 QDR II+/DDR II+ support 333 MHz and Burst of 4 QDR II+/DDR II+ support 550 MHz as highest frequency.
Organization	x8, x9, x18, x36	x18, x36	–
VDD	1.8 V ± 0.1 V	1.8 V ± 0.1 V	–
VDDQ	1.8 V ± 0.1 V or 1.5 V ± 0.1 V	1.8 V ± 0.1 V or 1.5 V ± 0.1 V	–
Read latency	1.5 clocks	2.0 and 2.5 clocks	QDR II+/DDR II+ read latency is not user selectable. Offered as two different devices.
Input clocks	Single ended (K, $\overline{K}$)	Single ended (K, $\overline{K}$)	–
Output clocks (C, $\overline{C}$)	Yes	No	–
ODT (On-Die Termination) [1]	No	Offered in ODT and Non ODT versions	
A0 (DDR B2)	Yes	No	–
A0, A1 (DDR B4)	Yes	No	–
Echo clock number	1 Pair	1 Pair	Echo clocks are single ended
PKG	165 ball FBGA	165 Ball FBGA	–
Individual byte write ($\overline{BW}$ 0, $\overline{BW}$ 1)	Yes	Yes	–

[1] For more details regarding on-die termination; see the application note AN42468, On-Die Termination for QDRII+/DDRII+ SRAMs.

Design Changes required to accommodate both QDR II/DDR II and QDR II+/DDR II+ SRAM devices

QDR II+/DDR II+ provide a higher speed path for most applications. It is advantageous because you can implement certain design changes in the existing designs to enable designing to both QDR II/DDR II and QDR II+/DDR II+ devices. Most of the changes mentioned in the earlier section can be met without a lot of changes to the board.

The changes can be categorized as:

1. Pinout changes
2. Host controller changes
3. Board changes

Pinout Changes

- The pins which were C and $\overline{C}$ clocks in the QDRII/DDRII are replaced by a QVLD and the NC pin in the ODT disabled QDR II+/DDR II+ devices. This requires the designs not use the output clocks C and $\overline{C}$. Also, the pin P6 should be pulled high with a 1 kΩ resistor. This will help in disconnecting the resistor to float the pin when QDR II+/DDR II+ is designed. ODT enabled QDR II+/DDR II+ devices have QVLD and ODT pins in place of C and $\overline{C}$. The pin R6 (ODT) is used to select high range or low range of impedance for the inputs [2].
- As the linear burst addressing is not present in DDR II+, the pins A0 and A1 are no connects. This is a minor change compared to the rest of the changes because the pins are internally bonded so their connection state does not matter. They can be connected to any value or left floating.

Figure 1, Figure 2, and Figure 3 highlights the pinout differences between a QDR II, Non ODT QDR II+ and ODT enabled QDR II+ x18 devices.

Figure 4, Figure 5, and Figure 6 highlights the pinout differences between a DDR II, Non ODT DDR II+ and ODT enabled DDR II+ x18 devices.

Figure 1. QDRII (x18 Pinout)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	V_{SS}/144M	A	$\overline{WPS}$	$\overline{BWS_1}$	K	NC/288M	$\overline{RPS}$	A	A	CQ
B	NC	Q9	D9	A	NC	K	$\overline{BWS_0}$	A	NC	NC	Q8
C	NC	NC	D10	V_{SS}	A	NC	A	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	A	A	A	V_{SS}	NC	NC	D1
P	NC	NC	Q17	A	A	C	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

Figure 2. Non ODT QDRII+ (x18 Pinout)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/144M	A	$\overline{WPS}$	$\overline{BWS_1}$	K	NC/288M	$\overline{RPS}$	A	A	CQ
B	NC	Q9	D9	A	NC	K	$\overline{BWS_0}$	A	NC	NC	Q8
C	NC	NC	D10	V_{SS}	A	NC	A	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	A	A	A	V_{SS}	NC	NC	D1
P	NC	NC	Q17	A	A	QVLD	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

Figure 3. ODT enabled QDRII+ (x18 Pinout)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/144M	A	$\overline{WPS}$	$\overline{BWS_1}$	K	NC/288M	$\overline{RPS}$	A	A	CQ
B	NC	Q9	D9	A	NC	K	$\overline{BWS_0}$	A	NC	NC	Q8
C	NC	NC	D10	V_{SS}	A	NC	A	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	A	A	A	V_{SS}	NC	NC	D1
P	NC	NC	Q17	A	A	QVLD	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	ODT	A	A	A	TMS	TDI

[2] For more details regarding on-die termination; see the application note AN42468, On-Die Termination for QDRII+/DDRII+ SRAMs.

Figure 4. DDRII (x18 Pinout)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/72M	A	R/$\overline{W}$	$\overline{BWS_1}$	$\overline{K}$	NC/144M	$\overline{LD}$	A	A	CQ
B	NC	DQ9	NC	A	NC/288M	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	A	A0	A	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	A	A	C	A	A	NC	NC	DQ0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

Figure 5. Non ODT DDRII+ (x18 Pinout)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/72M	A	R/$\overline{W}$	$\overline{BWS_1}$	$\overline{K}$	NC/144M	$\overline{LD}$	A	A	CQ
B	NC	DQ9	NC	A	NC/288M	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	A	NC	A	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	A	A	QVLD	A	A	NC	NC	DQ0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

Figure 6. ODT enabled DDRII+ (x18 Pinout)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/72M	A	R/$\overline{W}$	$\overline{BWS_1}$	$\overline{K}$	NC/144M	$\overline{LD}$	A	A	CQ
B	NC	DQ9	NC	A	NC/288M	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	A	NC	A	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	A	A	QVLD	A	A	NC	NC	DQ0
R	TDO	TCK	A	A	A	ODT	A	A	A	TMS	TDI

Host Controller Changes

- Change of latency from 1.5 cycles to 2.0 and 2.5 cycles: In the QDRII+, the read latency is increased to 2.0 and 2.5 cycles from the QDRII where the read latency is only 1.5 cycles. The host controller should be able to support either 2.0 or 2.5 cycles of latency (it does not have to support both latencies because each part only supports one latency). The choice between the 2.0 and 2.5 cycles of read latency should be made early in the design definition phase, based on the bandwidth and the host controller capabilities.
- Echo clocks to latch read data: CQ if in the existing design, the design uses the K or the C clocks to latch the read data. This should be modified to use the CQ clocks to latch the data.

Board Changes

- Higher performance: The board should be designed to support speeds up to 550 MHz.
- Output valid indicator: The board should be modified to include the QVLD signal and to take advantage of it when QDR II+ is designed.
- No termination resistors: The board should not include termination resistors for QDR II+/DDR II+ devices with ODT.

Summary

65 nm QDR II+/DDR II+ devices provide the ability to achieve high performance with bandwidth by applying a few minor changes to existing boards as well as the ability to create new designs. By designing boards and host controllers to meet both QDR II/DDR II and QDR II+/DDR II+ devices requirements, systems can support high performance of up to 550 MHz or 80 Gbps bandwidth.

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Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1200303	NJY	01/27/2008	New application note.
*A	3132438	NJY	01/10/2011	No change. Updated as per application note template.
*B	3339197	NJY	08/10/2011	Changed title of application note. Modified the verbiage under the section “Description of QDRII+/DDRII+ SRAM” on page 1. Modified the verbiage under the section” Differences between QDRII/DDRII and QDRII+/DDRII+ Functionality and Timing.” Changed the clock frequency above which the CQ and CQb clocks are recommended for read data capture from 250 MHz to 200 MHz. Modified and corrected the frequency range in Table 1. Changed maximum frequency supported to 550 MHz and maximum bandwidth supported to 80 Gbps. Inserted Figure 1, Figure 2, Figure 4, Figure 5. Modified the description under the section “Conclusion”.
*C	3705807	PRIT	08/07/2012	Changed the title. Changed Differences between QDR II/DDR II and QDR II+/DDR II+ Functionality and Timing section. Changed table 1. Added footnote #1. Changed pinout changes section, and board changes section. Added Figure 3 and Figure 6.
*D	4290988	PRIT	02/25/2014	Updated in new template. Completing Sunset Review.

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