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THIS SPEC IS OBSOLETE

Spec Number: 001-60142

Spec Title: AN60142 – PowerPSoC® – Configuring LED Driver Circuits in Floating Load Buck-Boost Topology

Sunset Owner: MKKU

Replaced By: 001-52699

AN60142 – PowerPSoC® – Configuring LED Driver Circuits in Floating Load Buck-Boost Topology

AN60142

Associated Project: Yes
Associated Part Family: CY8CLED0xD/G01
Software Version: PSoC® Designer™ 5.0
Associated Application Notes: AN51012, AN52209, AN53781, AN53127, AN52699, AN61668

Application Note Abstract

AN60412 describes the use of PowerPSoC® to drive LEDs with constant current control in a floating load buck-boost topology.

PowerPSoC can be configured for constant current LED control in different types of power topologies such as floating load buck, boost or floating load buck-boost topologies. This application note describes the circuit operation of the floating load buck-boost topology for LED control along with design equations and describes the use of PowerPSoC in this topology. The attached code example shows the firmware flow using the PSoC® Designer™ environment.

For information on using PowerPSoC in other topologies, refer application note AN52699 and AN61668.

Introduction

High Brightness LEDs (HB-LEDs) are gaining a lot of importance as a replacement for incandescent and fluorescent lamps. Their reduced usage of energy for the same amount of light output, significantly longer life, and flexibility of use due to form factor are the driving factors for their adoption. However, HB-LEDs are unique amongst the light sources; they need a DC current to be regulated through them versus a constant voltage.

Switching regulators provide an efficient method of regulating current through a HB-LED load. The choice of topology to use depends on the relationship between the input voltage and the HB-LED load voltage. PowerPSoCsupports the floating load buck, boost and floating load buck-boost topologies. A ‘buck’ topology is used when the load voltage is lower than the input voltage; a ‘boost’ topology is used when the load voltage is higher than the input. However, there are certain systems powered through battery supplies whose voltages vary over time. An example is a system powered by a 12 V battery. When the battery is fully charged, its terminal voltage is around 14 V and when it is completely discharged, it is around 10 V. If the load consists of 3 white LEDs, their forward voltage at around 500 mA of drive current could lie at approximately 11 V. To regulate the current through the LED across the entire range of input voltages, a topology known as the buck-boost is necessary.

In this topology, the circuit operates when the input voltage is either higher than or lower than the load voltage. The PowerPSoC family of devices has the capability to implement such a circuit topology.

This application note addresses the design of a ‘floating load buck-boost circuit’ to drive High Brightness LEDs using PowerPSoC. The circuit topology is explained, followed by the design equations for the circuit, for choosing the external components. An example firmware project is included as an example of the implementation described.

In PowerPSoC, the classic PSoC core is combined with high performance power electronics. This results in an integrated intelligent power electronics solution in a single QFN package. This family of devices (CY8CLED04D01) combines up to four independent channels of constant current drivers. These drivers feature hysteretic controllers with the Programmable System-on-Chip (PSoC) which has an 8-bit microcontroller, configurable digital and analog peripherals, and embedded flash memory.

PowerPSoC is designed to operate at voltages from 7 V to 32 V, can drive up to 1 A of current using internal MOSFET switches, and higher than 1 A with external MOSFETs. For a detailed introduction to PowerPSoC and its features, refer to the application note “AN51012- Firmware Design Guidelines for PowerPSoC” and the device datasheet.

Buck-Boost Topology

The topology discussed here is the 'floating load buck-boost'. This topology can be used for systems where the input voltage varies over time to be either lower or higher than the load voltage.

Figure 1. Buck-Boost Regulator Using PowerPSoC

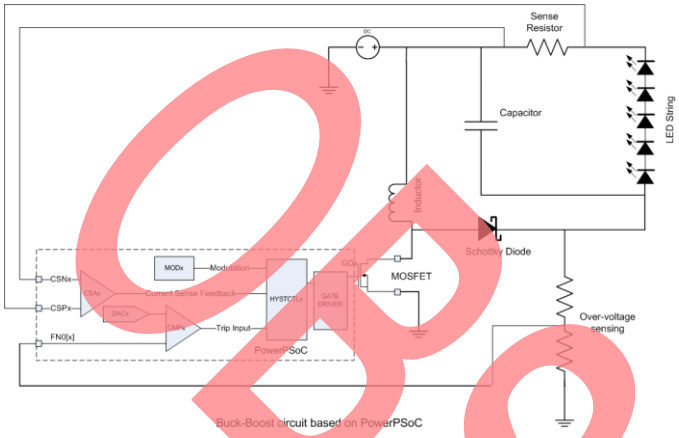


Figure 1 shows the simple schematic of a constant current buck-boost regulator using PowerPSoC. There are two main parts to this circuit:

- **The Power Converter:** The transistor, diode, inductor, and capacitor form the power converter part of the circuit.
- **The Control:** The combination of the sense resistor, the PWM block, and the hysteretic controller inside PowerPSoC form the control section.

This topology is referred to as 'floating load' because, the load which are the HB-LEDs are connected independent of supply or ground, that is, they are 'floating'.

Circuit Operation

The qualitative explanation is as follows.

- The PWM is a setup with a duty cycle higher than that required for a buck-boost (the calculation is explained later sections). Therefore, it constantly turns the switch ON and OFF periodically.
- When the switch is ON, the current through the inductor rises and the capacitor supplies current to the load. This is illustrated in Figure 2. Note that the FET and diode are present although not shown in the figure for the sake of simplicity.
- When the switch gets turned OFF, the current in the inductor continues to flow and therefore the inductor switches its polarity, and the magnitude of the voltage across its terminals increases until the diode's threshold voltage is crossed.
- When this occurs, the current flowing through the inductor flows into the capacitor and the load. The capacitor's voltage increases as the current flows into it. This is illustrated in Figure 3.
- The duty cycle of the PWM is chosen; therefore when the switch is turned ON, the increase in current through the inductor is larger than the decrease in current when the switch is turned OFF. As a result, the current through the inductor keeps increasing.

Figure 2. Equivalent Circuit When Switch is ON

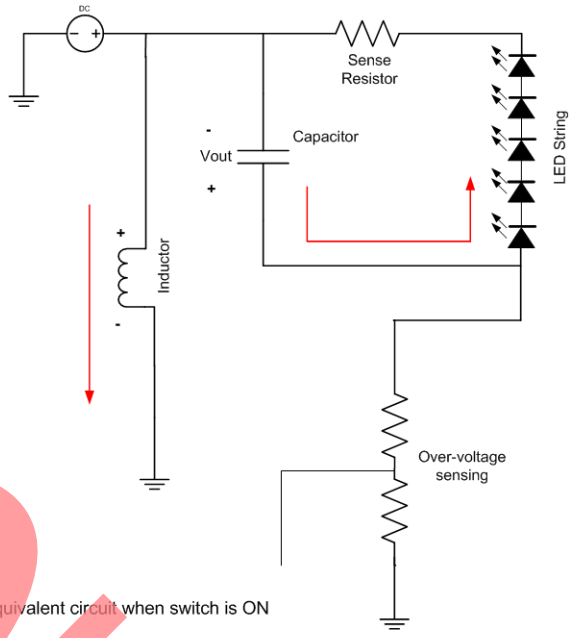
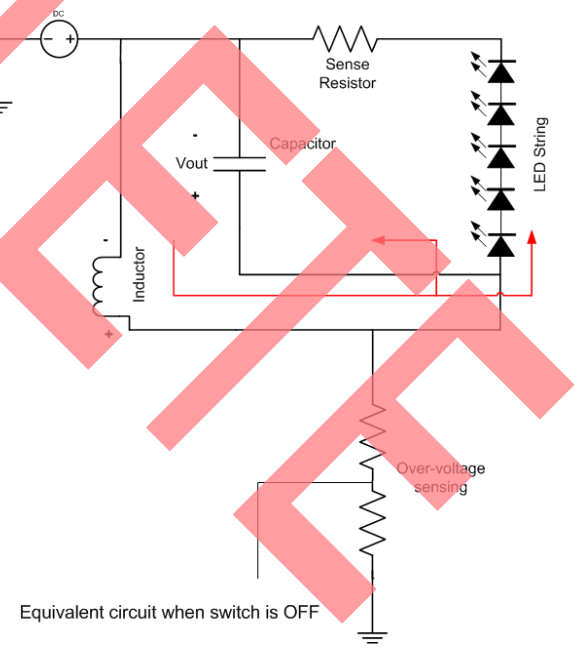


Figure 3. Equivalent Circuit When Switch is OFF



- This causes the capacitor voltage to keep increasing and results in an increase in the load current.
- When the load current crosses the upper threshold set in the hysteretic controller (sensed by a resistor), the hysteretic controller turns the switch OFF independent of the PWM's output.

- This causes the inductor to discharge completely into the capacitor after which the capacitor is the sole supplier of current through the load.
- The current gradually decreases as the capacitor discharges its energy into the load. When the load current crosses the lower threshold set in the hysteretic controller, the switch is allowed to operate again as per the PWM's output. The cycle then repeats.

Although the circuit acts as a buck and boost converter, it essentially is *always boosting* the input voltage to a higher voltage.

- Starting with the cathode of the schottky diode and applying Kirchoff's Voltage Law (KVL) in the direction of the inductor in a loop, you get **Vin + Vout + Vf(schottky)**.
- If the forward voltage of the schottky is ignored since it is relatively small, the voltage at the node common to the schottky's cathode and the HB-LEDs' anode is **Vin + Vout.**
- Therefore, the input voltage **Vin** is converted to **Vin + Vout**.

Hence, irrespective of whether the input is less than or greater than the load voltage, the circuit is performing a boost function.

Mathematical Model

This section describes the mathematical model for this topology.

Primary Circuit Parameters

These are the initial parameters of the system that need to be decided before the rest of the circuit components can be worked out. They are the following at a minimum:

1. **Input Voltage:** V_{in} (min and max)
2. **Load Voltage:** V_o (this depends on number of LEDs in the string)
3. **Load Current:** I_o (this is the current that needs to be regulated)

Secondary Circuit Parameters

These are parameters that are derived from the initial parameters.

1. Boost Ratio

The boost ratio is defined as the ratio of the boosted voltage to the input voltage. This must not be mistaken for Vo/Vin.

$$B = \frac{Vin + Vo}{Vin}$$

This follows from the fact that the voltage at the node where the cathode of the flyback diode and the anode of the LEDs meet with respect to ground has to be sufficient to drive the LEDs. The LED cathode end is itself connected to Vin making the requirement of the boosted voltage to be higher than Vin by the voltage Vo.

This also demonstrates that the input voltage always has to be boosted irrespective of whether the output voltage is greater than or less than the input voltage. This makes the boost ratio of this buck-boost circuit greater than the boost ratio of a grounded load boost circuit with the same system specifications.

For a Vin range of 13 V-20 V, using the minimum value of Vin, and Vout = 17 V, you get B = (13+17)/13 = 2.31

2. Duty Cycle

This is the duty cycle that the FET must be turned ON and OFF at (hence duty cycle of the PWM) to generate the required output voltage.

$$D = \frac{Vo}{Vin + Vo}$$

This is the standard duty cycle equation for a buck-boost topology. However, for the system to operate as intended, the PWM must be operated at a duty cycle greater than this value 'D' so that the capacitor voltage (load voltage) increases gradually. This increase in load voltage causes the current to increase, which then allows the system to regulate it. The highest duty cycle occurs at the lowest input voltage and that is the value that must be used in the final firmware to run the PWM.

For example, with Vin of 13 V-20 V, Vout of 17 V, duty cycle is 17/ (13+17) = 0.567. For example, a PWM with 6 bit resolution (period value of 63) can have a pulse width of 40 that translates to a D of 0.65.

3. Resolution of Modulator (R)

The modulator in this topology is used to run the boost function by switching the FET at a constant frequency and duty cycle. It is constantly running and is used to gradually increase the energy built up in the inductor and there by the boost voltage. The key here is to select the resolution (R in bit count) such that the change in current through the inductor during the 'ON' time and 'OFF' time is low (sub 100 mA). Otherwise, very large oscillations of current occur which is generally not good for the system in terms of noise/EMI and makes it very difficult to select component ratings.

Now, $Fout = \frac{Fin}{2^R}$

$$Tout = \frac{1}{Fout}$$

$$Ton = D \times Tout$$

$$Toff = (1 - D) \times Tout$$

With Fin = 48 MHz, a resolution R of 6 bits yields Fout = 750 KHz. The Duty Cycle sets Ton and Toff to less than 1 uS with which most systems are sufficient to ensure that the inductor does not have large changes in current across it while at the same time allowing it to build up energy.

Making the resolution higher than 6 bits, lowers the frequency and increases Ton and Toff.

4. Io(peak)

This is the peak of the load current as decided by the reference set on the upper DAC in the hysteretic controller

$$Io(peak) = Io + (\frac{Ru}{100} \times Io)$$

Where, Ru is the upper ripple in percentage. With Io = 0.35 A, and Ru = 10%, Io(peak0) = 0.385 A.

5. Io(valley)

This is the lower limit for the load current as decided by the reference set on the lower DAC in the hysteretic controller. Note that this is usually also greater than the desired average current Io. This is because, after the hysteretic controller is turned ON (subsequent to hitting the lower threshold), the capacitor continues to discharge while the inductor charges up enough to transfer energy sufficient enough to charge up the capacitor voltage.

$$Io(valley) = Io + (\frac{Rl}{100} \times Io)$$

Where Rl is the lower ripple in percentage. For example, with Io at 0.35 A and Rl = 5%, Io(valley) = 0.3675 A.

6. Iin(peak)

This is the max value of the inductor current that is reached just before the hysteretic controller is turned OFF (due to hitting the upper DAC threshold).

$$Iin(peak) = \frac{Io(peak) \times B}{\eta}$$

Here, η is the assumed efficiency of the system (pessimistic). The output current peak is scaled by the boost ratio to estimate input current. A typical value to assume for efficiency is 75%.

With Io(peak) = 0.385 A, B = 2.31 and efficiency = 75%, Iin(peak) works out to be 1.19 A.

7. Iin(valley)

This is the lowest value of input current while the system is operating right before the hysteretic controller is turned ON again.

$$Iin(valley) = Iin(peak) - \Delta(Iin)$$

Here, the final current Iin(valley) must be above 0A so that the inductor does not go into discontinuous mode of operation.

For example, with Iin(peak) being 1.19 A, assuming a Delta(Iin) of 1A, Iin(valley) = 0.19 A. Delta (Iin) is chosen such that there is some minimum current flowing through the inductor when the switch comes ON again.

8. V(cap)

This is the final voltage on the capacitor at the end of the period when the hysteretic controller has been off and just before it is turned on again.

$$V(cap) = Vo + \Delta(vcap)$$

The amount by which the voltage across the capacitor is increased ($\Delta(vcap)$) is the change in voltage allowed during the period while the hysteretic controller is off.

To keep the voltage across the capacitor more or less constant, delta (Vcap) is chosen to be 60 mV. That makes V(cap) = 17 + 0.06 = 17.06 V.

Circuit Component values

1. C – Load Capacitor Value

The equation to determine the capacitor value needed for the circuit comes from the basic capacitor equation,

$$i \times t = C \times V$$

Here,

i – The average current through the load.

t – Time period during which the capacitor is required to supply the current I at the load voltage.

V – Output voltage change during the time period t.

Now, the switching time period is given by,

$$Tout = \frac{1}{Fout}$$

The time period during which the capacitor is required to supply the load current is the time during which the switch is 'ON'. This is given by,

$$t = D \times Tout \Rightarrow t = \frac{D}{Fout}$$

During this time period, the voltage on the capacitor changes by a certain amount and you call this Vo(ripple).

Therefore,

$$i \times t = C \times V \Rightarrow C = \frac{i \times t}{V} \Rightarrow C = \frac{Io \times D}{Fout \times Vo(ripple)}$$

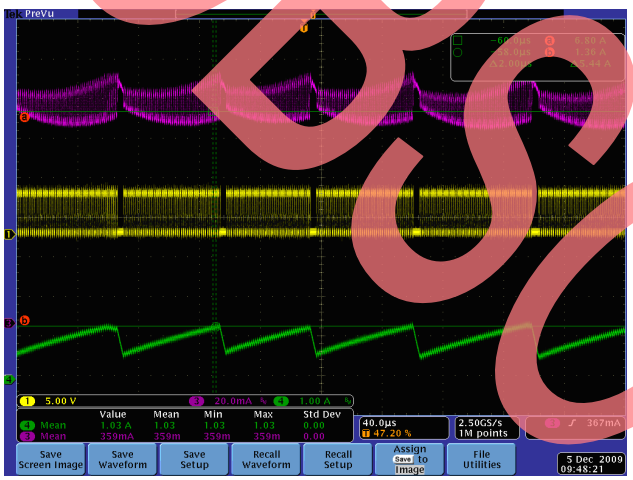
The duty cycle D, Output frequency Fout and Io are determined as shown previously. That leaves Vo(ripple) as a selectable value to determine C.
Using an example of 4 mV for Vo(ripple), D of 0.567, Fout of 750 KHz and Io of 350 mA, we get a C of 66.11 uF. The closest standard value is used which is 68 uF.

2. L – Inductance Value

The inductor is the other energy storage element. The inductor captures energy from the input at a certain voltage and current and transfers it to the output which is at a different voltage, making it the component of choice in many kinds of switching circuits used to transfer energy.

From the section Circuit Operation on page 2 and points Duty Cycle and Resolution of Modulator (R) on page 3 of this note, the FET is turned ON and OFF at a duty cycle greater than what is required to boost the voltage. Therefore, the increase in current through the inductor during Ton is greater than the decrease in current during Toff. This means the current through the inductor is gradually increasing. This causes the load current to constantly increase too.

Figure 4. Screen Capture of Buck-Boost Circuit in Operation



The previous figure shows the operation of the circuit captured from a real system. The green waveform at the bottom is the inductor current. The magenta signal at the top is the load current. The yellow signal is the FET gate drive signal.

When the load current hits the upper threshold of the hysteretic controller, the controller gets turned OFF which means the inductor is now continuously in the discharge cycle (FET is OFF).

During this period, the inductor is transferring its energy primarily into the bulk capacitor and some to the load. This transfer of energy into the capacitor causes its voltage to increase. The amount by which the capacitor voltage increases during this period is called Δ(vcap).

Therefore, repeating the V(cap) equation on page 4 here,

$$V(cap) = Vo + \Delta(vcap)$$

V(cap) denotes the final voltage on the capacitor. If the energy used to drive the load current is ignored (since the inductor current is significantly larger than load current) for simplicity's sake, then the energy discharged by the inductor during the hysteretic controller's OFF time is the energy gained by the capacitor.

Energy stored in inductor is,

$$E_L = \frac{L \times i^2}{2}$$

And energy stored in a capacitor is

$$E_C = \frac{C \times V^2}{2}$$

Now, equating the change in energy in the inductor to that of the capacitor, we get

$$\frac{L \times Iin(peak)^2}{2} - \frac{L \times Iin(valley)^2}{2} = \frac{C \times V(cap)^2}{2} - \frac{C \times Vo^2}{2}$$

Re-arranging this equation to denote L in terms of everything else,

$$L = C \times \frac{V(cap)^2 - Vo^2}{Iin(peak)^2 - Iin(valley)^2}$$

Using the value of C calculated before (66.11 uF), the inductance value becomes 98.67 uH. On the protoboard, two 47 uH inductors can be connected in series to achieve 94 uH which is the closest value to the required inductance.

Special Notes

From the equations for capacitor and inductor in section C – Load Capacitor Value on page 4 and L – Inductance Value respectively, increasing Vo(ripple) decreases the capacitance needed. A smaller capacitor also results in a smaller inductor value.

This leads to the thought that one could make the Vo(ripple) as large as possible to have very small capacitor and inductor values. There are two ways in which this can come back and create problems for the designer.

- Increasing the allowed ripple beyond a certain point causes large oscillations in the output (load) voltage which LEDs are quite sensitive to. For instance, if the required forward voltage for a certain drive current is not available, the drive current has to decrease which misses the point of this exercise.
- When the inductor value decreases, the following is the implication using the equation,

$$V_L = L\, di/dt \Rightarrow \frac{di}{dt} = \frac{V_L}{L}$$

From this equation, when the inductor value reduces, the rate of change of current through the inductor increases. For a given modulator resolution and frequency, during Ton and Toff (calculated previously in section Resolution of Modulator (R) on page 3) the change in current is larger. This follows from the fact that dt is constant and hence, di has to increase for increasing the $\frac{di}{dt}$ for a corresponding decrease in inductance. To counter this, the modulator resolution can be decreased further, (to increase output frequency) but this results in poor control of the duty cycle.

To summarize, while attempting to increase Vo(ripple) in the quest to decrease the C and L values, the change in current must be calculated. If this change is larger than approximately 150 mA (as a thumb rule) for a given time period, the ripple should be reduced to increase the C and L values.

Ultimately, the tolerance to the oscillations in current through the inductor is the choice of the designer but having large current oscillations results in two undesirable results.

1. Increased noise and EMI
2. Potentially higher saturation current ratings for the inductor increasing its package size – which ultimately defeats the purpose of trying to reduce the inductance size.

Component Selection

In a power system, there is more to component selection than determining its electrical value. For example, an inductor needs to have a certain saturation current rating or a capacitor needs to have a certain voltage rating.

There are five external components apart from the load

Sense Resistor

Value: The sense resistor is in the path of the load current. The value needs to be chosen such that the current flowing through it (load current) produces a voltage across it approximately in the range of 100 mV. This translates to a CSA output of 2.0V (CSA gain is 20). If there are a range of currents, sizing the sense resistor such that the differential voltage is between 30 and 100 mV is a good practice.

Package: The resistor has to be able to dissipate the power generated by the current flowing through it. $P = I^2 \times R$. Usually, packages such as 1206, 1210, 2010 or 2512 suit the power requirements. The power rating should be higher than the expected power dissipation.

Inductor

Value: The equation under section L – Inductance Value on page 5 generates an inductor value. Determine the closest standard value available and use that as shown in the example.

Saturation Current Rating: As inductors saturate, their inductance value decreases. They are usually rated at a certain percentage drop in inductance such as 20-30% at a particular current (Isat). The value calculated as Iin(peak) is a deciding factor. The saturation current rating of the chosen inductor should approximately be 1.5 to 2 times the value of Iin(peak). This is to have a safe margin and to account for the fact that inductor current is very high at startup.

DCR: The equivalent DC resistance of the inductor plays a role in the power loss when current flows through it. This should be as low as possible to increase efficiency.

MOSFET (Switch)

VDS(max): The maximum drain to source voltage rating is the maximum voltage that the MOSFET can block when it is OFF without breaking down. In the buck-boost circuit, the voltage at the drain node when the switch is OFF is (Vin(max) + Vout + Vf(diode)). There is usually also a 15-20% overshoot when the MOSFET turns OFF and the diode turns ON. The selected MOSFET must have a VDS(max) rating of at least 1.5 times the expected voltage on the drain.

If(max): The current flowing through the MOSFET when it is ON is the current flowing through the inductor and its maximum value is calculated with the equation in section Iin(peak). As mentioned earlier, the inductor current at startup is usually higher than this by at least 50-100%. Therefore, the selected MOSFET's current rating must be at least twice the expected value.

RDS(on): Every MOSFET has some ON resistance when it is in saturation mode and conducting mode. The selected MOSFET should obviously have a low RDS(on) so that the power loss through the MOSFET is reduced. This is important since the MOSFET is switching in the range of 100s of KHz and the power loss through the FET is directly proportional to the frequency of switching.

Diode

Schottky diodes are preferable for this since they have low Vf and low reverse recovery times.

Reverse Voltage (peak): When the MOSFET is ON, this diode is required to block the voltage at the capacitor (with respect to ground). This is given by (Vin + Vout). Therefore, the reverse voltage rating of the selected diode should be at least 1.5-2 times to allow some variation in input and output.

Average Rectified Forward Current: The current that flows through the diode when it is ON is the current through the inductor. This is generally given by Iin(peak) but the startup current is higher by about 50-100%. The selected diode must have a forward current rating of at least 2 times of the maximum inductor current.

Forward Voltage: The chosen diode should also have the lowest possible forward voltage. This is to ensure reduction in power loss through the diode. $P = V_F \times I_F \times (1 - D)$

Load Capacitor

Voltage Rating: The capacitor is expected to work at the load voltage. Therefore, its voltage rating should be at least 1.5 times of the maximum expected load voltage.

Type: Usually, electrolytic capacitors are acceptable for this application and are cheaper than ceramic equivalents.

Firmware Design

The main aspect about firmware design for this buck-boost topology is the configuration of the user modules in a safe operating state.

Potential dangerous conditions that the firmware can help protect against are:

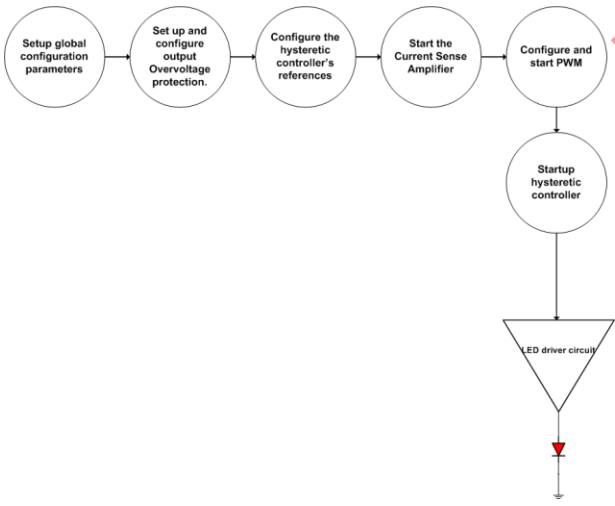
- Continuous switching of MOSFET and turning it ON without any control could result in constant increase in load voltage and hence the load current. This can also cause increase in inductor current beyond its saturation value.
- Open circuit of load due to damage to load or loose connector can cause rapid buildup of very high voltage on the capacitor. This crosses the absolute maximum ratings of the Current Sense Amplifier pins and result in permanent damage.

The following simplified flow diagram illustrates the order and list of things to configure in firmware. This application note assumes that you are familiar with the PSoC Designer environment which is the IDE, used to configure, write firmware for and program the PowerPSoC device. For an introduction to PSoC Designer, refer to the On-Demand training on the web.

PSoC Designer and PSoC Programmer can be downloaded from the web.

Refer to the application note AN51012 – Firmware Design guidelines for PowerPSoC for a detailed description on configuring PowerPSoC using PSoC Designer however it describes a floating load buck circuit.

Figure 5. Firmware Flow Diagram



1. The device is first configured using the 'chip view' which enables global configuration of the device, picking and placing pre-made user modules, connecting them as desired and configuring them.

   Figure 6 shows the snapshot of the global resources tab in the chip view that is suitable for this project.

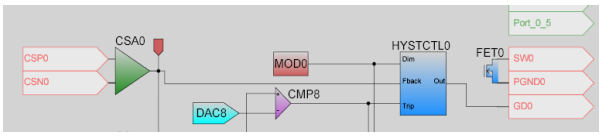
   Figure 7 shows the snapshot in the chip view of the user modules that are placed and connected to each other.

Figure 6. . Global Resources Configuration

Global Resources - buck_boost_basic

Power Setting [Vcc / S	5.0V / 24MHz
CPU_Clock	SysClk/1
Sleep_Timer	512_Hz
VC1= SysClk/N	12
VC2= VC1/N	16
VC3 Source	VC2
VC3 Divider	256
SysClk Source	Internal
SysClk*2 Disable	No
Analog Power	SC On/Ref Low
Ref Mux	(Vdd/2)+/-(Vdd/2)
Op-Amp Bias	Low
A_Buff_Power	Low
Trip Voltage [LVD]	4.81V
LVDThrottleBack	Disable
AINX Connection	CSA0
AINX Mode	IREF
MOD Clock	SysClk*2
Bias Generator	Enable
Switching Regulator	Enable

Figure 7. Chip View of Placed User Modules



- ❑ The Current Sense Amplifier CSA0's output is the feedback to the hysteretic controller.
- ❑ MOD0's output (PWM) feeds the modulator input to the hysteretic controller.
- ❑ CMP8 is the hardware trip comparator whose output forms the trip input to the hysteretic controller. This comparator is responsible for turning the system off in case of over voltage.
- ❑ CMP8's reference on its negative input is supplied by DAC8 and its other input comes from pin FN_0_1 which carries the load voltage signal on it.
- ❑ Refer to the attached PSoC Designer project for a reference on the properties of each module.

2. After the modules are connected and their properties defined, generate the project using the 'generate' option from the build menu.
3. In the *main.c* file, the following is the order of code
   - ❑ The digital code for DAC8 (that supplies the reference to CMP8) is written using an API. The module is then started, followed by the trip comparator CMP8. This in effect sets up the protection feature first.
   - ❑ The hysteretic controller's DAC voltage range is setup and the digital codes for the 2 DACs are configured. These two represent the high and low level of the load current.
   - ❑ The Current Sense amplifier is then started. Note that this module ***must*** be started before the hysteretic controller, since it is the feedback element.

- The modulator (PWM) is configured (period and pulse width) and subsequently started. The period is set according to the desired output frequency and resolution of the PWM. Refer to the equations described earlier in this note on how to decide these values. The pulse width is initially set to 0. There is a loop later in the firmware to soft-start the PWM. If the PWM is started directly with its final pulse width value, the current in the inductor rises to very large levels rapidly. In the first few periods of switching as soon as the system is turned ON, the load voltage is very close to 0. This ensures that the inductor hardly discharges its energy in the time that the switch remains OFF (since the energy discharge depends on the voltage).
- The hysteretic controller (which controls the switch) is now started after all other modules are started.
- A loop starting with the starting pulse width to the final pulse width is run in which:
  - The PWM's pulse width is set to the current value of the loop.
  - A delay is executed to let the PWM run at that pulse width for that delay.

At the end of this, for basic buck-boost functionality, the program runs in an infinite loop. The hardware controls itself.

Additional Firmware Options

A buck-boost system is defined as one where the input voltage varies over time gradually. This also means that the frequency of switching (when the PWM pulse is high) changes accordingly. Additionally, because of tolerances in the load capacitor, it can charge to slightly different voltages and drive slightly different current into the load.

In cases where the load current needs to be controlled tightly, an Analog-to-Digital (ADC) converter can be configured inside the device to have a closed loop feedback system to drive the desired current through the load.

As shown in the example project attached, a simple incremental ADC can be placed. Its positive input is setup to be connected to the 'AINX' Multiplexer. This multiplexer's output can be the output of any of the four Current Sense Amplifiers in the device and is setup in the global resources menu shown in Figure 6.

The ADC is setup as an 8-bit output. In the code, the ADC is initialized and started to sample continuously. This initialization is not critical to the operation and safety of the circuit and can be performed anywhere in the process described earlier.

In the infinite while loop, at the end of all the initializations, the program execution waits for the next ADC sample. This is stored in a temporary variable and the ADC proceeds to gather the next set of samples. As shown in the project, an average of a certain number of samples can be performed to filter out short-term fluctuations.

If this final result (average of the current measured over a period) is away from the desired load current by more than the accepted tolerance, the DAC references of the hysteretic controller are changed.

- If the current is to be increased, the upper reference should be increased first followed by the lower reference.
- If the current is to be decreased, the lower reference should be decreased first followed by the upper reference.

Note that although the attached project implements an ADC to measure the load current, it does not implement any function based on the measured value. It is left to you to implement this part based on the desired behavior.

To ensure a gradual change of current, it is recommended to change the references' (for the hysteretic controllers) one value at a time.

In order to enable a convenient method to monitor the measurement of the ADC real time, an EzI2C user module (that is an I2C slave) is also configured in the firmware project. This can be used in conjunction with the CY3240 I2C-USB bridge to watch the graphical movement of the ADC output on a PC using the GUI that comes with the kit.

Other Considerations

In a high-power system like this circuit is bound to be used in, the PCB layout is of prime importance. Some of the important aspects to take care of are,

- Kelvin and differential connections for the sense resistor (that feeds the load current back to the controller).
- Short loops for de-coupling capacitors connected to the gate drive VDD pins on the device.
- Short loops between the gate driver on the controller and the MOSFET (if an external one is used).
- Use of a 4-layer board to enable good power and ground connections.

For detailed recommendations on layout, follow the application note AN52209 – PCB Guidelines for PowerPSoC as a LED Driver.

Summary

This application note and the firmware presented along with it provide sufficient information on implementing a buck-boost constant current regulator using PowerPSoC. However, like in many power systems, the final circuit might require minor modifications in component values or firmware configuration for PWM pulse width or the current thresholds, to perform exactly to the expectations.

PowerPSoC presents a powerful new standard of designing high-power systems together with intelligence using software tools. The combination of the well established PSoC core along with high performance power electronics enables highly integrated, low cost, small designs that differentiate products using it from ones that use conventional methodologies.

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2891357	UKK	03/12/10	New Application Note.
*A	3201404	SNVN	03/21/11	Title update. Abstract update. Minor corrections to the content. Removed references to the author. Updated attached code example to work with PSoC® Designer™ 5.1 and ImageCraft Pro.
*B	3933278	MKKU	03/15/2013	Obsolete spec.

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone: 408-943-2600
Fax: 408-943-4730
http://www.cypress.com/