DEMO SENSE2GOL PULSE

XENSIV™ 24 GHz radar system platform

Board version V3.0

About this document

Scope and purpose

This application note describes the key features of Infineon's BGT24LTR11 Pulsed-Doppler shield, part of DEMO SENSE2GOL PULSE radar system platform, equipped with the XENSIV™ 24 GHz BGT24LTR11 low-power MMIC, and helps the user quickly get started with the demonstration board.

1. The application note describes the hardware configuration and specifications of the sensor module in detail.
2. The document also provides a guide to configure the hardware and implement simple radar applications with the firmware/software developed.

Intended audience

The intended audience for this document are design engineers, technicians, and developers of electronic systems, working with Infineon's XENSIV™ 24 GHz radar sensors.

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1 Introduction

The DEMO SENSE2GOL PULSE is a demonstration platform for Infineon’s 24 GHz silicon-germanium (SiGe) BGT24LTR11 radar chipset. It consists of two boards – the microcontroller board: Radar Baseboard MCU4, and a radar front-end board: BGT24LTR11 shield. This document focuses on the BGT24LTR11 shield for a Pulsed Doppler implementation.

The system is designed to allow customers to carry out prototyping and system integrations, as well as initial product feature evaluations. The platform is a low-power solution for detecting speed and direction of movement (approaching or retreating) of a human. These features of the board make it suitable for various applications such as motion detection, presence sensing, etc. These use cases target applications such as smart lighting, smart doors, smart devices, etc.

The main radar technique used on the platform is Continuous Wave (CW/Doppler) radar for velocity estimation. The principle of the Doppler effect is used. The radar transmits a constant-frequency signal continuously and receives the echo signal from the moving target. The change in phase between the transmitted and received signal is used to calculate the target’s velocity.

Sample and Hold (S&H) circuitry is implemented for low-power consumption. Two-stage low-noise baseband amplification stages are used for enhanced target detection. The baseband section can be configured by re-soldering for different cut-off frequencies and gain requirements of different applications. The module also offers the possibility of using a battery for operation.

The module provides a complete radar system evaluation platform including demonstration software and a basic graphical user interface (GUI) which can be used to display and analyze acquired data in time and frequency domain. An onboard debugger with licensed firmware from SEGGER enables easy debugging over USB. Infineon’s powerful, free-of-charge toolchain DAVE™ can be used for programming the XMC4700 microcontroller. The system also features integrated micro-strip patch antennas on the PCB with design data, thereby eliminating antenna design complexity at the user end.

This application note describes the key features and hardware configuration of the BGT24LTR11 shield in detail.

1.1 Key features

The primary features of the Sense2GoL Pulse radar system are as follows:

- Detects motion, speed and direction of movement (approaching or retreating) for a human
- Extremely low power consumption (using S&H circuitry)
- Two-board topology for RF section and microcontroller sections
- Two configurable analog amplifier stages for the RX channel
- Micro-strip patch antennas with 10 dBi gain and 29 x 80 degrees Field of View (FoV)
- Multiple power supply possibilities – micro-USB, external power supply or LiPo battery
- Compatible with Arduino for ease of use and prototyping
- Operates in different weather conditions including rain, fog, etc.
- Can be hidden in the end application as it detects through non-metallic materials

1.2 Overview

The platform is a stack-up of two boards – BGT24LTR11 shield (radar front-end) and Radar Baseboard MCU4 (for signal processing). The Sense2GoL Pulse radar system consists of the following key components:

- BGT24LTR11 – highly integrated 24 GHz transceiver MMIC with one transmitter (TX) and one receiver (RX)
- XMC4700 – 32-bit Arm® Cortex®-M4 based microcontroller for signal processing
- TS5A4596 – SPST S&H switches for low power consumption
- IRLHS2242 – MOSFET for duty-cycle operation
- INA226 – current shunt and power monitors for current consumption estimation
- MCP73831T – battery manager for charging and using the battery
- CW1280T – EEPROM to store board identifier information
- MOLEX 047571001 – SD card reader for storing raw data
- XMC4200 – 32-bit Arm® Cortex®-M4 based microcontroller for debugging

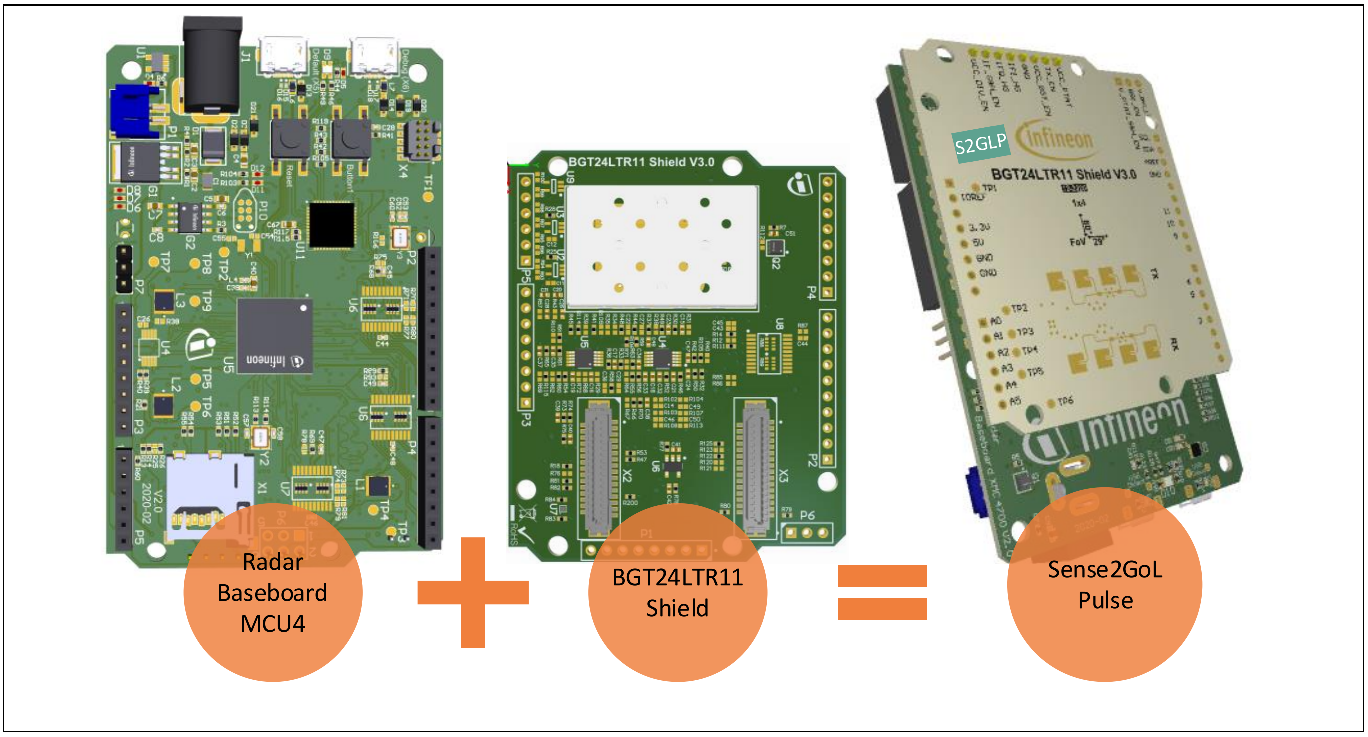


Figure 1 Sense2GoL Pulse demo board

Note: The BGT24LTR11 shield in Sense2GoL Pulse platform is assembled for Pulsed Doppler operation.

The circuitry for the BGT24LTR11 shield (Pulsed Doppler) is designed to carry out Doppler detection with low power consumption. The analog I/Q signals from the MMIC act as inputs to the S&H circuitry. When the switch is closed (sample mode), the hold capacitor follows the I/Q analog signal of the MMIC and charges to its peak value. When the switch is opened (hold mode), the hold capacitor holds the sampled voltage.
This implementation allows us to turn the BGT24LTR11 off during the “hold time” and hence save power.
The S&H_EN signal from the Radar Baseboard MCU4 controls the on/off timing of the switches. The output of the S&H circuitry is amplified and filtered by the baseband section. These amplified I/Q signals are then routed to the Radar Baseboard MCU4 via connectors for signal processing. It also provides the control signals for the BGT24LTR11 shield board via connectors.

2 System specifications

Table 1 gives the specification of the Sense2GoL Pulse (Pulsed Doppler) radar system.

Table 1 Sense2GoL Pulse demo board specifications

Parameter	Unit	Min.	Typ.	Max.	Comments
System performance					
Detection speed	km/h	0.3	5	10	Configurable by re-soldering the baseband section (Table 3) and considering the sampling frequency as well as the number of samples
Detection distance	m	0.1	15	20	Human target
Power supply					
Supply voltage	V	3.3	5	5.5	Supplied via the baseboard
Supply current	mA		50		All blocks on (only the shield)
Transmitter characteristics					
Transmitter frequency	GHz	24.05	24.125	24.25	
Effective Isotropic Radiated Power (EIRP)	dBm		+14		Conditions: BGT P_{OUT}: +6 dBm Loss (TX_{OUT} to ant. input = 2 dB) Simulated ant. gain = +10 dBi
Receiver characteristics					
Receiver frequency	GHz	24.05	24.125	24.25	
IF conversion gain – (stage 1)	dB		30		Configurable by re-soldering the baseband section (Table 3)
IF conversion gain – (stage 1 + stage 2)	dB		59		Configurable by re-soldering the baseband section (Table 3)
-3 dB bandwidth – (stage 1 + stage 2)	Hz	16		420	Configurable by re-soldering the baseband section (Table 3)
Antenna characteristics (simulated)					
Antenna type			1 x 4		
Horizontal – 3 dB beamwidth (HPBW)	Degrees		80		
Elevation – 3 dB beamwidth (HPBW)	Degrees		29		
Horizontal sidelobe level suppression	dB	13			
Vertical sidelobe level suppression	dB	13			

Note: The above specifications are indicative values based on typical datasheet parameters of BGT24LTR11 and simulation of several other parameters (antenna characteristics and baseband section) and can vary from module to module. The numbers above are not guaranteed indicators for module performance for all operating conditions.

3 Hardware description – BGT24LTR11 shield

This section presents a detailed overview of the BGT24LTR11 shield hardware specifications, including the MMIC considerations, power supply and board interfaces.

3.1 Overview

The radar shield is shown in Figure 2. It contains the following sections:

- RF part – consists of the Infineon 24 GHz radar MMIC – BGT24LTR11 and includes micro-strip patch antennas for the TX and RX sections
- S&H part – consists of SPST switches and hold capacitors to sample and hold the analog I/Q signals from the MMIC using the control signal S&H_EN
- Analog amplifier part – smoothens the sampled I/Q signals from the S&H circuitry and amplifies them for the digital part
- EEPROM part – stores data such as board identifier

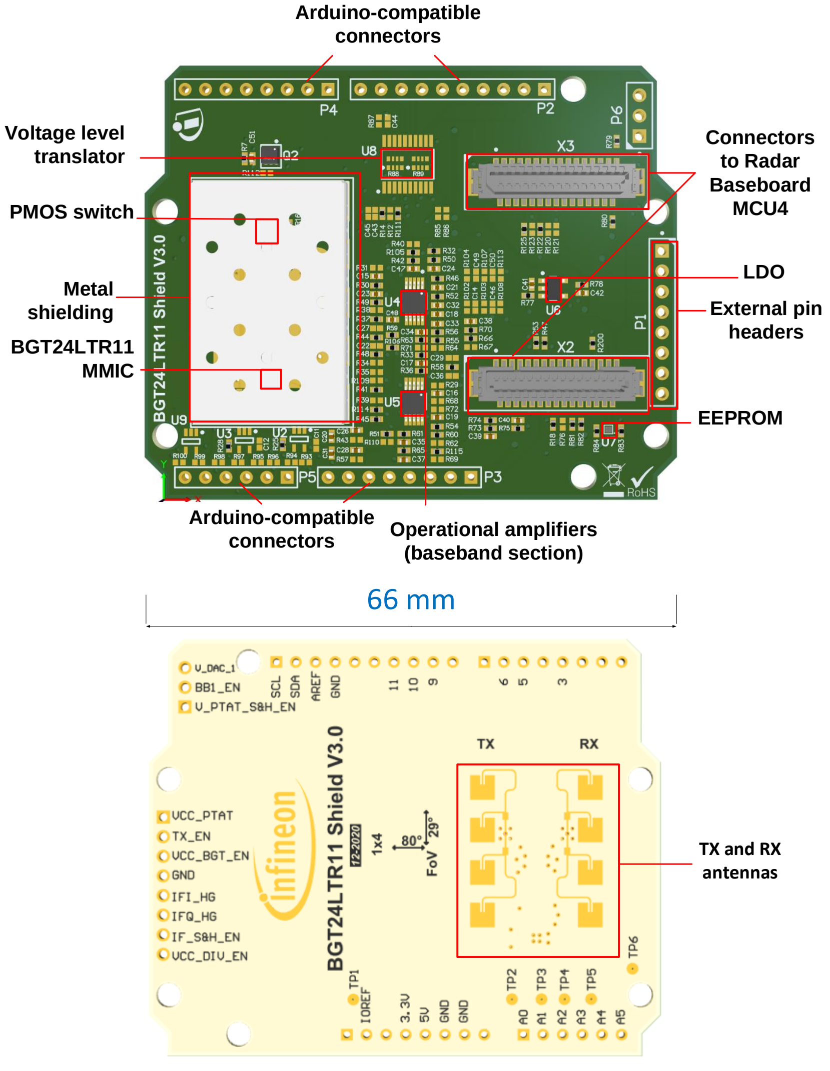


Figure 2 BGT24LTR11 shield with main components

The radar shield demonstrates the features of the BGT24LTR11 RF front-end chip and gives the user a customizable radar solution. The board gives possibilities to implement different baseband settings, VCO control, etc. to get closer to a custom-fit solution for the use case. It also makes it possible to quickly gather sampled radar data that can be used to develop radar signal processing algorithms on a PC or implement target detection algorithms directly on the microcontroller using DAVE™.

3.2 Block diagram

Figure 3 shows the block diagram of the Sense2GoL Pulse system. It consists of the highly integrated 24 GHz transceiver MMIC BGT24LTR11 with 1 TX and 1 RX. The built-in voltage source Proportional-to-Absolute-Temperature (PTAT) delivers a VCO tuning voltage. When connected to the VCO tuning pin it compensates for the inherent frequency drift of the VCO over-temperature, thus stabilizing the VCO within the ISM band and eliminating the need for a PLL/microcontroller.

The I/Q outputs from the BGT24LTR11 are connected with the SPST switches to perform a S&H operation. During the sample time, C_{hold} charges to its peak value, following the input analog signal. During the hold time, it holds the value and allows us to turn the BGT24LTR11 off. The S&H_EN control signal is provided by the Radar Baseboard MCU4 via the connectors.

The output of the S&H circuitry is routed to the baseband section to provide the required gain to the IF signals. The baseband is also duty cycled in order to save current consumption. The outputs of the baseband section are connected with ADC inputs of the XMC4700 on the radar baseboard.

The system is powered through the Radar Baseboard via the micro-USB plug. It is also possible to power it via external 7 V power supply or with a LiPo battery. A low-noise voltage regulator (U6) is used to provide a regulated power supply to the different building blocks of the RF shield.

BGT24LTR11 is supplied over a PMOS, which enables turning the MMIC on/off during S&H timings. Pin headers on the PCB allow for interfacing the sensor module with an external processor.

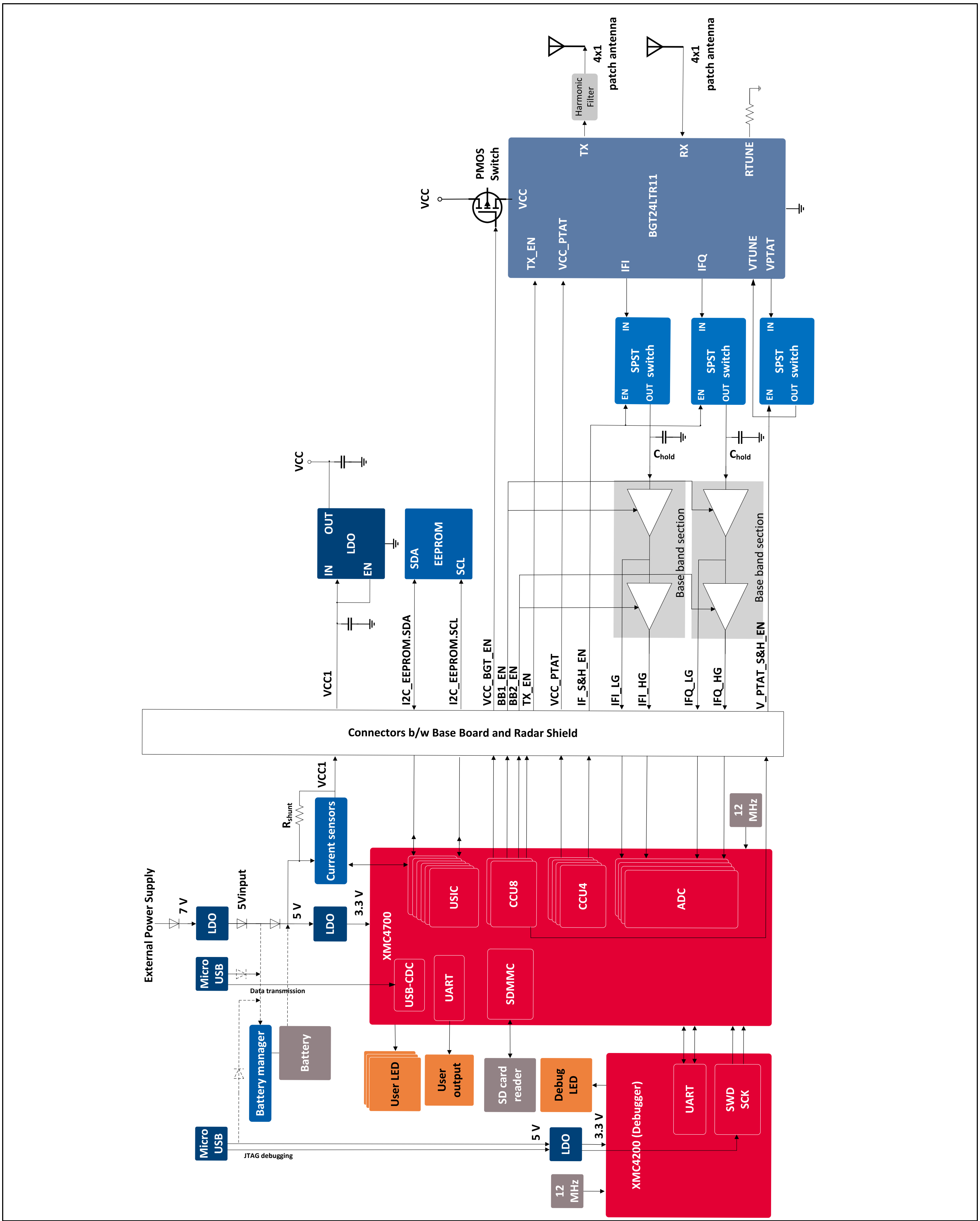


Figure 3 Sense2GoL Pulse block diagram

3.3 Power supply

The Radar Baseboard MCU4 is powered via micro-USB connector, external 7 V power supply or LiPo battery. It also provides the supply for the BGT24LTR11 shield via the connectors. A LDO (U6) is used on the BGT24LTR11 shield to supply all the components. Figure 4 shows the power supply concept used in the system.

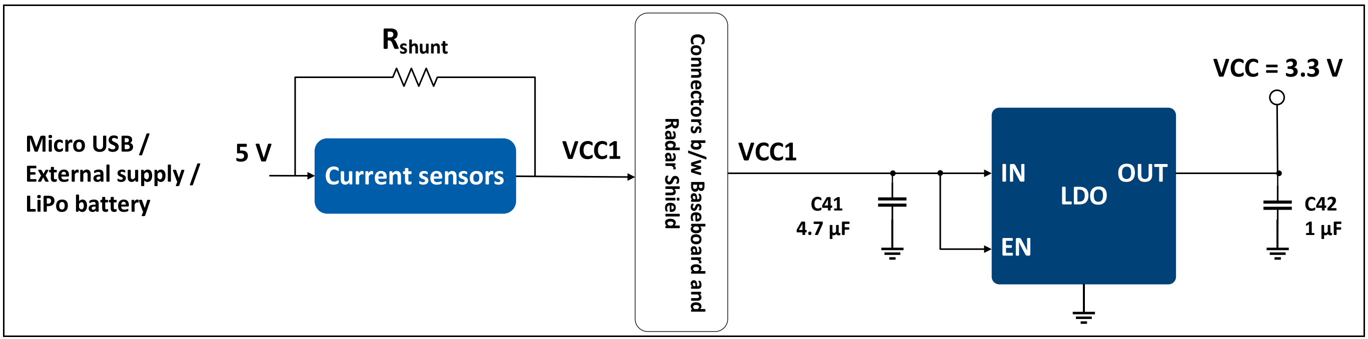


Figure 4 Power supply block diagram

3.4 EEPROM

The BGT24LTR11 shield contains an EEPROM (U7) to store data such as a board identifier. The Serial Data (SDA) is a bi-directional pin that is used to transfer addresses and data into and out of the device. The Serial Clock (SCL) is an input that is used to synchronize the data from and to the device.

When the shield is plugged into the Radar Baseboard MCU4, the sensor's supplies are initially deactivated. Only the EEPROM is powered. The MCU reads the content of the EEPROM's memory to determine which shield is plugged into the interface. Only when the board has been correctly identified are the sensor's supplies activated.

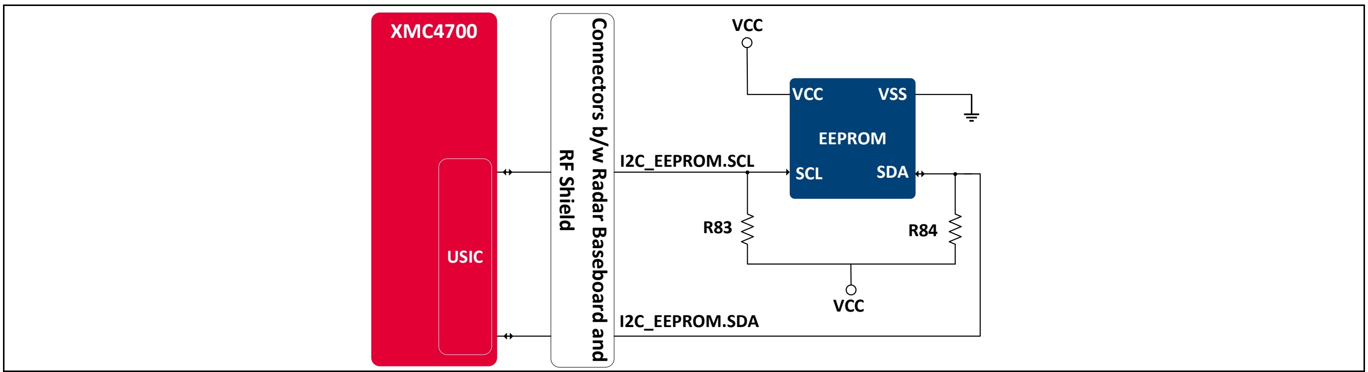


Figure 5 EEPROM block diagram

3.5 RF front-end

Figure 6 shows the top view of the RF front end. The RF front-end can be shielded with a cover and absorber material to get the best RF performance. The transmitter and receiver inputs of the BGT24LTR11 are single ended. The TX output and RX input are connected over a matching structure, a DC block and a feed-through via to the antennas on the other side of the board. The isolation between the RX and TX ports is improved by adding a grounded length of line at the ground pins next to the TX output pin.

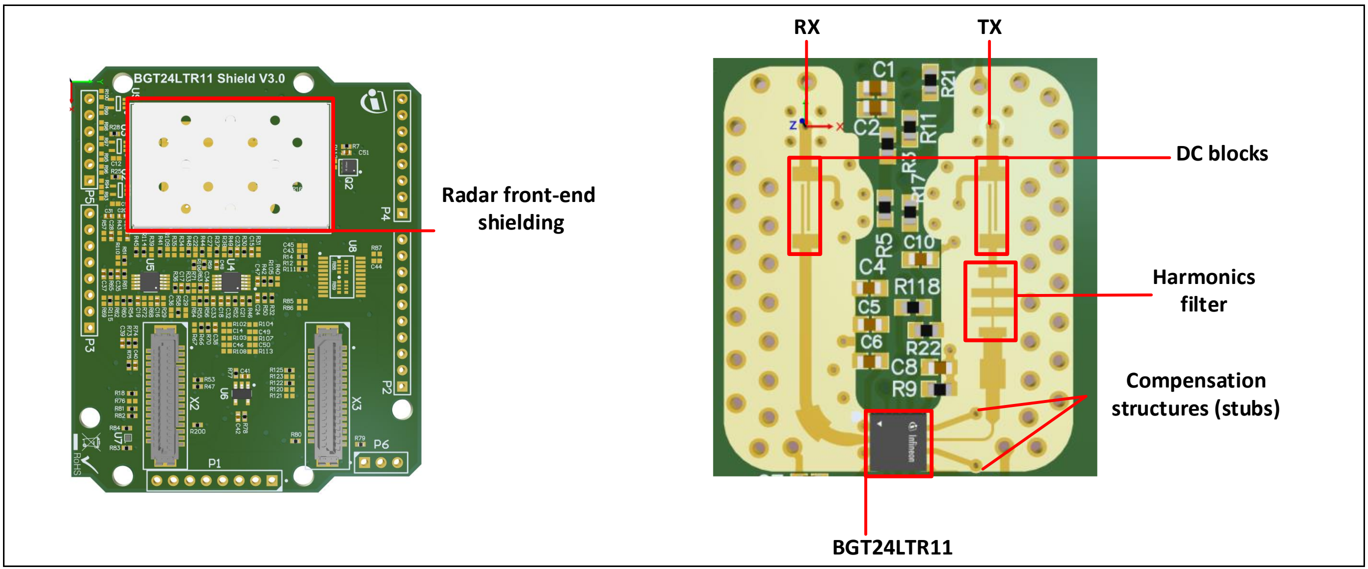


Figure 6 RF front-end top view

3.6 BGT24LTR11 MMIC

The heart of the sensor module is the highly integrated BGT24LTR11 24 GHz transceiver MMIC. Figure 7Figure 7 shows the detailed block diagram of the MMIC. BGT24LTR11 is a radar MMIC for signal generation and reception, operating in the 24.000 GHz to 24.250 GHz ISM band. It is based on a 24 GHz fundamental Voltage Controlled Oscillator (VCO).

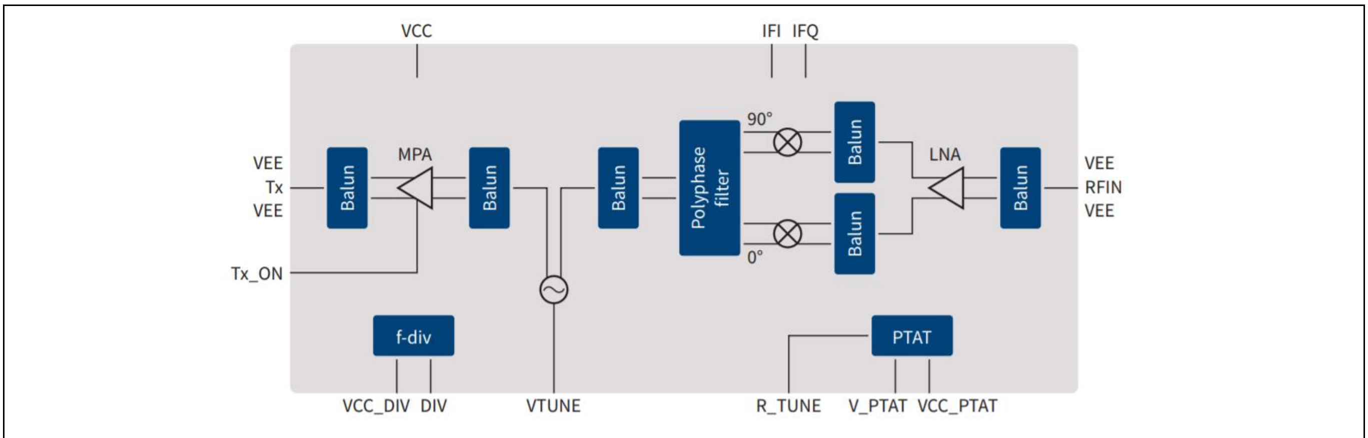


Figure 7 BGT24LTR11 block diagram

A built-in voltage source delivers a VCO PTAT tuning voltage. When connected to the VCO tuning pin it compensates for the inherent frequency drift of the VCO over-temperature, thus stabilizing the VCO within the ISM band and eliminating the need for a PLL/microcontroller. The PTAT is also duty cycled and voltage at VCO tuning pin stabilized via S&H circuitry to further minimize power consumption.

The receiver section uses a Low Noise Amplifier (LNA) in front of a quadrature homodyne down-conversion mixer in order to provide excellent receiver sensitivity. Derived from the internal VCO signal, a RC Poly-Phase Filter (PPF) generates quadrature LO signals for the quadrature mixer. I/Q IF outputs are available through single-ended terminals.

3.7 Antennas

The BGT24LTR11 shield features a 4 x 1 array antenna for the transceiver and receiver sections. The antenna has a gain of 10 dBi and a Half-Power Beam Width (HPBW)of 29 x 80 degrees. Figure 8 shows the simulated 2D and 3D radiation pattern.

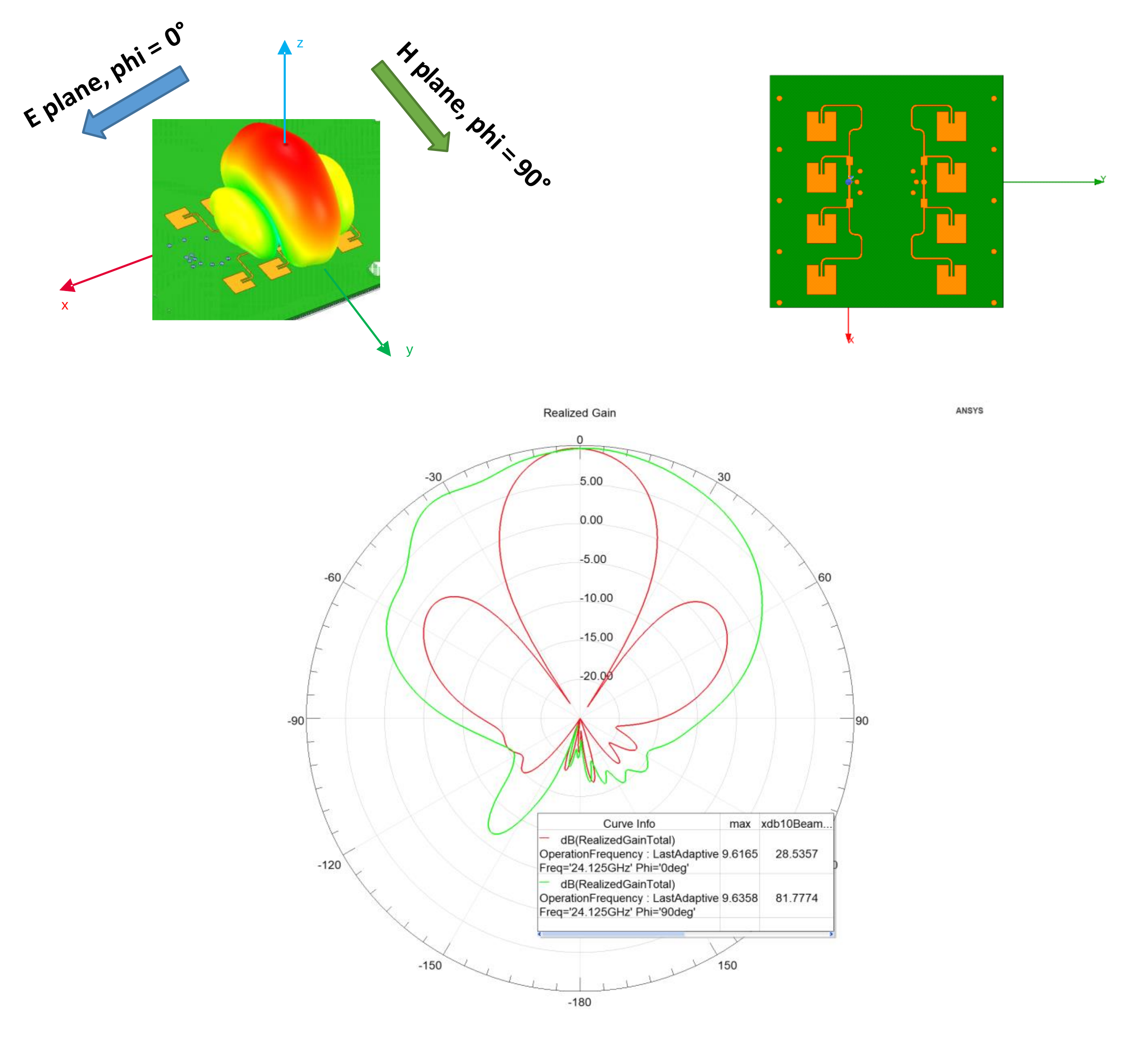


Figure 8 2D radiation pattern for array antennas

3.8 Sample and Hold (S&H) circuitry

The BGT24LTR11 shield has S&H circuitry between the MMIC and the baseband section. The I/Q signals from the BGT24LTR11 are connected to the inputs of SPST switches. The control signal S&H_EN is generated by the MCU on the radar baseboard and routed via connectors to the RF shield. When the switch is closed (sample mode), the hold capacitor (C_{hold}) follows the I/Q analog signal of the BGT and charges to its peak value. When the switch is opened (hold mode), the C_{hold} holds the sampled voltage. This implementation allows us to turn the

BGT24LTR11 off during the "hold time" and hence save power. The output of the S&H circuitry is amplified and filtered by the baseband section. It is important to follow the Nyquist criteria for the analog input signal (I/Q) and the control signal, S&H_EN. The frequency of the control signal should be at least twice the frequency of the input signal. Figure 9 shows the block diagram of the circuitry and Figure 10 shows the corresponding signals.

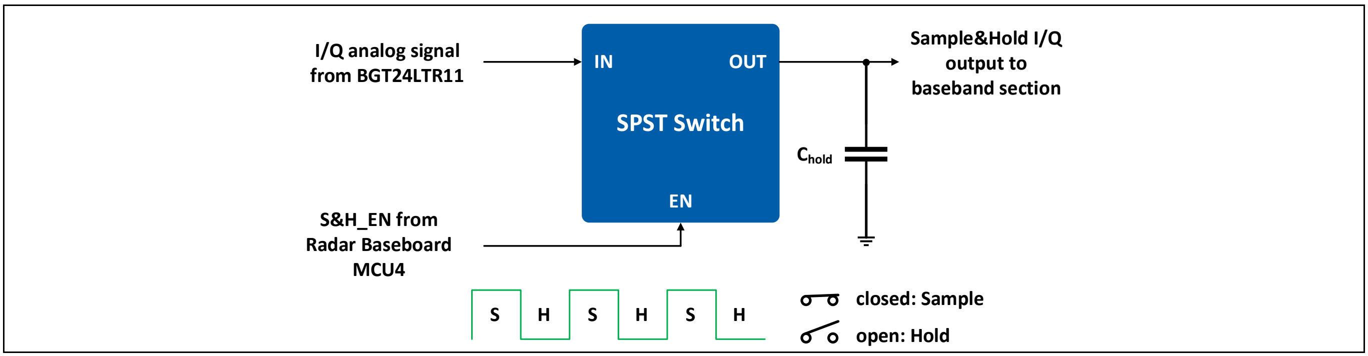


Figure 9 S&H circuitry

The sample time is a portion of the "pulse width". The pulse width can vary from 1 to 10 µs. Short pulse widths reduce the sample time of the MMIC's output signals, saving more power. However, the time might not be enough to charge to the peak value, and so reduce the final signal strength at the output.

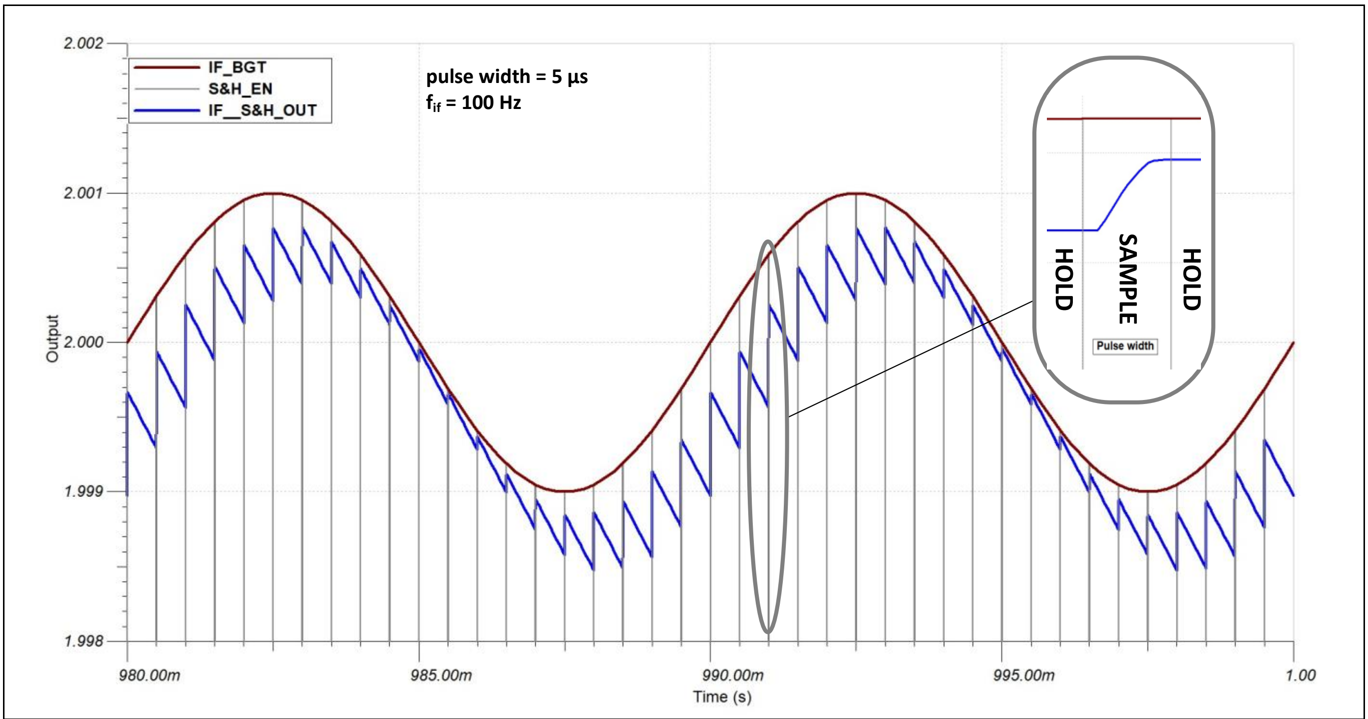


Figure 10 S&H circuitry signals

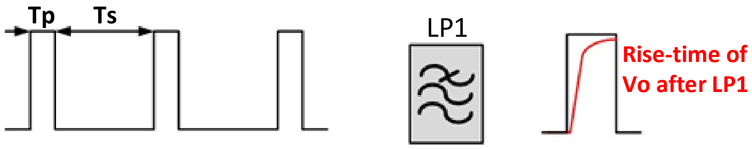
The hold capacitor value is also a critical point of the circuit. It is a trade-off between current saving capability, preserving the S&H voltage and low-pass filter performance. S&H capacitor leakage must be exceptionally low.

For the S&H switch, the leakage current performance is also important. Leakage in the S&H structure will cause a severe periodic decline in the S&H voltage at sample rate (as shown in Figure 10). This is also visible as an unwanted interferer frequency at sampling frequency at the output of the baseband circuitry. In critical cases, it can block the baseband amplifier. The S&H switch used has an extremely low leakage current and it is therefore not recommended to change it. Another S&H switch is added between V_PTAT output and V_TUNE input of the MMIC. This further reduces the current consumption by allowing duty cycling of the V_PTAT.

During the S&H process, the entire MMIC (BGT24LTR11) is switched on and off periodically (pulsing). Therefore, the I and Q mixer output from the MMIC will produce short pulses periodically. Each pulse is a discrete, very short sample of the mixer's DC bias voltage superimposed by the actual AC Doppler swing. In BGT off-state, the mixer output becomes zero. The S&H circuit after the mixer output converts a discrete time signal into a continuous time signal by preserving the entire mixer voltage during the pulse off-time.

Switching on the BGT and the S&H switch, the S&H capacitor shows the same DC voltage as the mixer output, because the total voltage (DC + AC) is preserved in the S&H capacitor from the previous pulse. Therefore, only the superimposed AC voltage must be updated without the need to recharge the S&H capacitor for the DC bias voltage.

The required time for updating the AC voltage depends on the mixer output frequency (Doppler frequency) and the time constant of the RC LP1 filter formed by the mixer output impedance and the S&H capacitor. For a given S&H time, the S&H capacitor must be selected to enable an update of the actual S&H voltage.



RC LP_ BW-3dB = 0.22/t_r Hz (start: 20% / end: 80%)
RC LP_ BW-3dB = 55 kHz
RC LP_ BW-3dB = 1/(2π*R*C)
t_r = 4 µs (S&H ON time)
R = 500 Ω (mixer output impedance)
➔ C = 5.7 nF (Hold capacitor)

Figure 11 Hold capacitor calculation

The target is to use a RC capacitor with high capacitance although the AC voltage is not fully recharged (20 percent to 80 percent rise-time calc.). A higher capacitor value will reduce noise folding but leads to a slightly lower magnitude of the baseband Doppler signal.

3.9 Analog baseband section

The BGT24LTR11 provides both in-phase and quadrature-phase Intermediate Frequency (IF) signals from its receiver. Depending on the target in front of the radar antennas, the analog output signal from the BGT24LTR11 chipset can be very low in amplitude (µV to mV range). To process these low amplitude signals it is necessary to amplify the IF signals.

The BGT24LTR11 shield offers two stages of signal amplification using low-noise operational amplifiers. As shown in Figure 12 and Figure 13, the I/Q outputs of the S&H circuit are filtered and amplified in the first gain stage. The second gain stage consists of a DC block operating as a high-pass filter and a multiple feedback active filter topology which provides additional gain and bandpass filtering to the output of the first gain stage. The low-gain and high-gain output signals are low-pass filtered to avoid aliasing. A voltage divider is used to create the 1.65 V reference voltage.

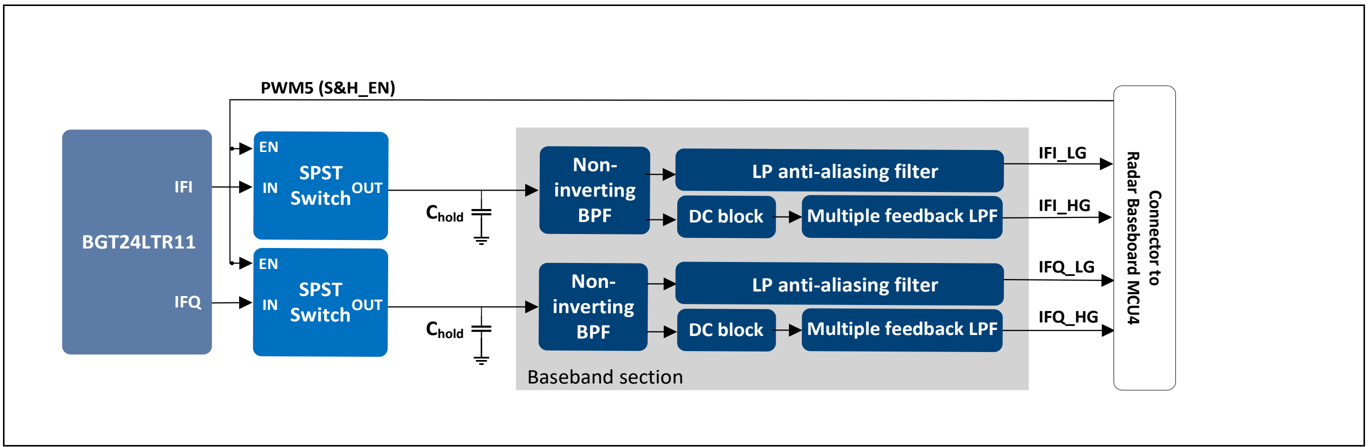


Figure 12 **Baseband amplifier chain block diagram**

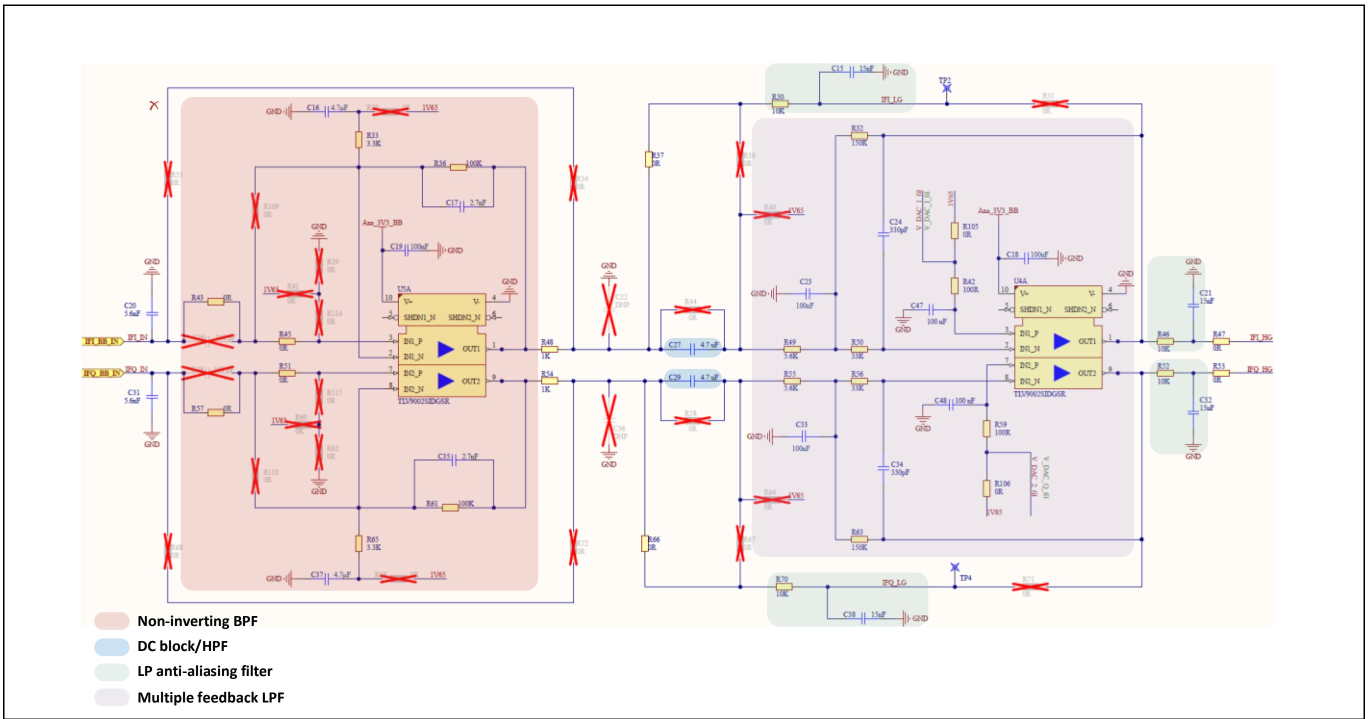


Figure 13 **Baseband amplifier chain schematics**

Figure 14 shows exemplary IF low-gain and high-gain signals. The offset of the low-gain signal equals the static offset of the BGT output signals. Due to the DC block at the beginning of the second stage, the offset of the high-gain signal matches the reference voltage of 1.65 V.

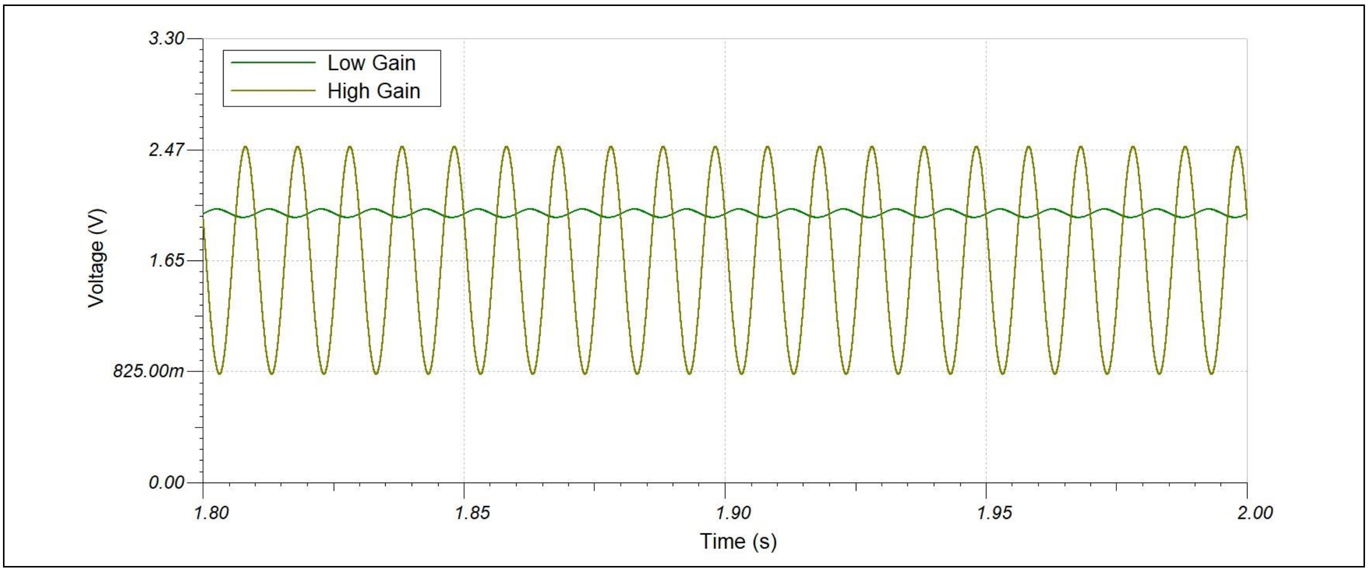


Figure 14 IF low-gain and high-gain signals for an input of 100 Hz, 1 mV input signal

As shown in Figure 15, the first gain stage provides a gain of 29.62 dB (low-gain stage) and both the stages together provide a gain of 59.31 dB (high-gain stage). The 3dB cutoff frequencies are also marked in this figure.

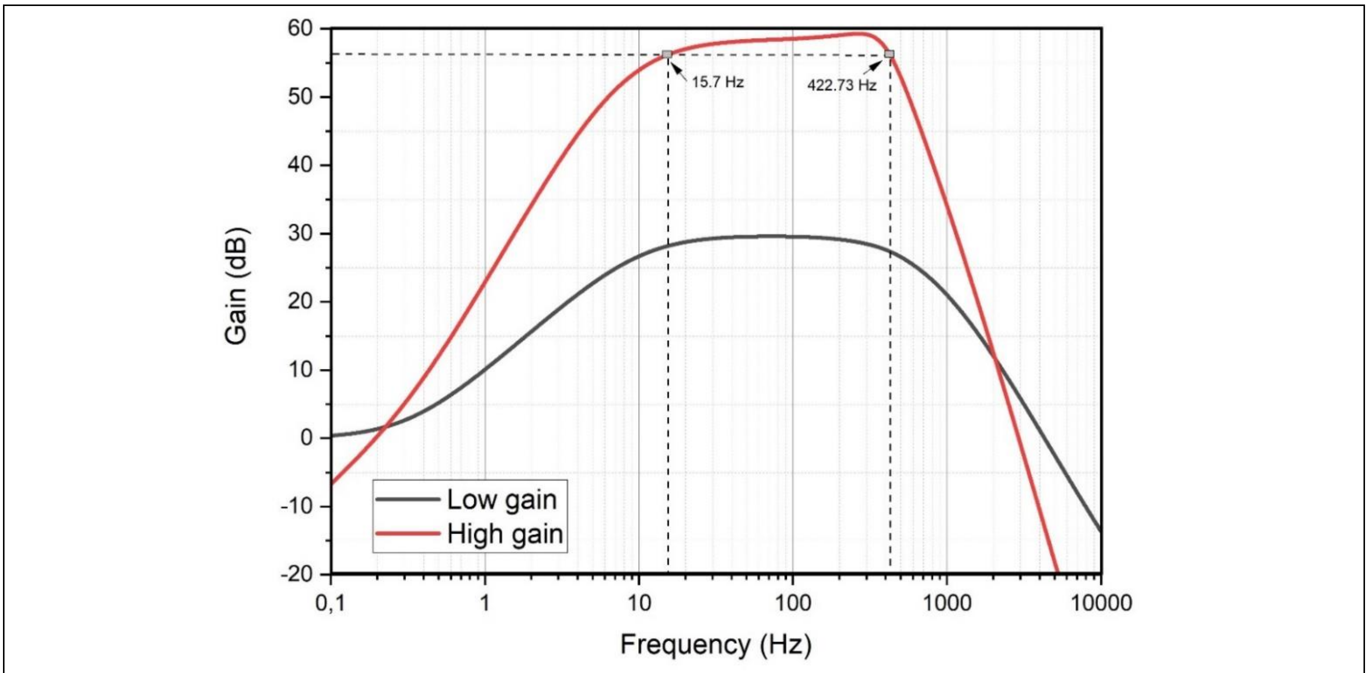


Figure 15 Baseband frequency response for low-gain and high-gain stages

Figure 15 shows the frequency response of the low- and high-gain stages. The BGT24LTR11 shield allows the user to select either the low-gain (first stage only) or high-gain (first stage + second stage) mode depending on the target RCS and distance to be detected. The low-gain output is referenced to the individual mixer output bias voltage (1.6 to 2.0 V), and the high-gain stage is AC coupled and referenced to VCC/2 = 1.65 V.

Table 2 lists the MCU pins (on the Radar Baseboard MCU4) associated with each of the gain stages. Use the graphical pin select tool in the DAVE™ software to select the appropriate pins for signal processing.

Table 2 Baseband amplifiers to MCU pin connections

XMC4700 – port pin	Pin label	Pin function
P14.6 (VADC.G0CH6)	IF.I1	IFI – high gain
P14.7 (VADC.G0CH7) / P14.3 (VADC.G1CH3)	IF.Q1	IFQ – high gain
P14.14 (VADC.G1CH6) / P15.3 (VADC.G2CH3)	IF.I2	IFI – low gain
P14.15 (VADC.G1CH7) / P15.9 (VADC.G3CH1)	IF.Q2	IFQ – low gain

The gain and bandwidth of the IF stages are fixed and can be manually configured by the user by changing the resistor and capacitor values specified in Table 3. In addition to Table 3, AC coupling by C27 and the input impedance of the I_multiple feedback filter (MFB LP by the second stage) form the second high-pass for the I-channel. For the Q-channel contributors are C29 and the input impedance (Q_MFB low-pass).

Table 3 Baseband amplifier components and settings

IF stage	Designator	Gain	Configurable components – I section	Configurable components – Q section
Stage 1 (Low gain)	U5A	29.66 dB	C16, R33, C17, R36	C37, R65, C35, R61
Stage 1 + Stage 2 (High gain)	U5A + U4A	59.28 dB	All components as mentioned for Stage 1 + R49, R50, R32, C23, C24	All components as mentioned for Stage 1 + R55, R56, C34, R63, C33

The baseband section should be configured accordingly to provide sufficient gain at these frequencies. The cut-off frequencies of the baseband section are 15 to 420 Hz.

The Doppler frequency $f_{Doppler}$ is calculated using the following formula:

$$f_{Doppler}(Hz) = \frac{2v}{\lambda}$$

Where v = speed of the target (m/s)

λ = wavelength (m)

Table 4 shows the calculated Doppler frequency values for different target speeds for the 24 GHz radar module.

Table 4 Doppler shift frequencies for different speeds using 24 GHz radar

Speed (km/h)	0.5	1	2	4	6	8	10	12
Doppler shift (Hz)	22	44	89	178	268	357	446	536

Figure 16 shows the configuration of a frame. Each frame is a series of pulses, followed by a frame off-time.

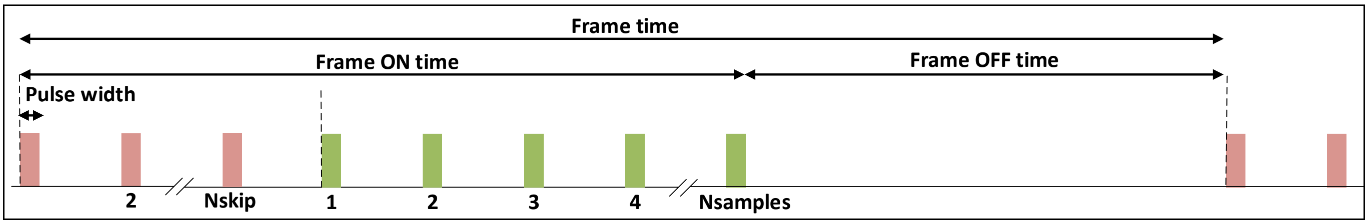


Figure 16 Frame structure and terminology

The steps below explain the design and calculations for the system:

$$f_{Doppler} = 2 \times v_{moving\ target} \times \cos(\varphi) \times \frac{f_{Transmitted}}{c}$$

$$\frac{1}{\lambda} = \frac{f_{Transmitted}}{c}$$

1. Select v_{max} (m/s) to determine maximum Doppler frequency:

$$f_{IFmax} = f_{Dopplermax} = \frac{2 \times v_{max}}{\lambda}$$

2. Select v_{min} (m/s) to determine minimum Doppler frequency :

$$f_{IFmin} = f_{Dopplermin} = \frac{2 \times v_{min}}{\lambda}$$

These f_{IFmin} and f_{IFmax} values are the cut-off frequencies for the baseband section.

3. Determine the minimum sampling frequency and Pulse Repetition Time (PRT).

The required sampling frequency ($f_{sampling}$) depends on the maximum targeted baseband frequency and on the required over-sampling (minimum factor 2) to get more headroom for the real anti-aliasing filter.

$$f_{sampling} \geq 2 \times f_{IFmax}$$

$$PRT = \frac{1}{f_{sampling}}$$

4. Determine the minimum number of samples per frame ($N_{samples}$):

$$N_{samples} \geq \frac{f_{sampling}}{f_{IFmin}} \quad , rounded\ to\ the\ next\ power\ of\ 2$$

5. Determine the minimum $Frame\ ON\ time$:

Sample skip count (N_{skip}) is the number of samples to be skipped at the beginning of each frame to get rid of the DC offset in the I/Q signals generated in the pulse interval time. These samples are completely disregarded in the signal processing chain. Therefore, total number of samples per frame (N_{total}) are:

$$N_{total} = N_{skip} + N_{samples}$$

$$Frame\ ON\ time = \frac{N_{total}}{f_{sampling}} = N_{total} \times PRT$$

6. Select frame time or update rate:

$$\frac{1}{Frame\ rate} = Frame\ time \geq Frame\ ON\ time$$

Table 5 **System parameters, symbols, and units**

Symbol	Parameter	Unit
$\boldsymbol{\lambda}$	Wavelength	mm
$\boldsymbol{f_{Transmitted}}$	Transmit frequency	GHz
$\boldsymbol{c}$	Speed of light	m/s
v_{max}	Maximum speed to be detected	m/s
v_{min}	Minimum speed to be detected	m/s
f_{IFmax}	Max. IF freq. (max. Doppler frequency)	Hz
f_{IFmin}	Min. IF freq. (min. Doppler frequency)	Hz
$f_{sampling}$	Sampling frequency	Hz
PRT	Pulse repetition time	µs
$N_{samples}$	No. of samples per frame	–
N_{skip}	No. of samples to be skipped per frame	–
N_{total}	Total number of samples per frame	–
$Frame\ ON\ time$	Duration in which pulses are generated	ms
$Frame\ time$	Total frame time	ms
$Frame\ rate$	No. of frames per second	Hz
$Pulse\ width$	Width of each pulse	µs

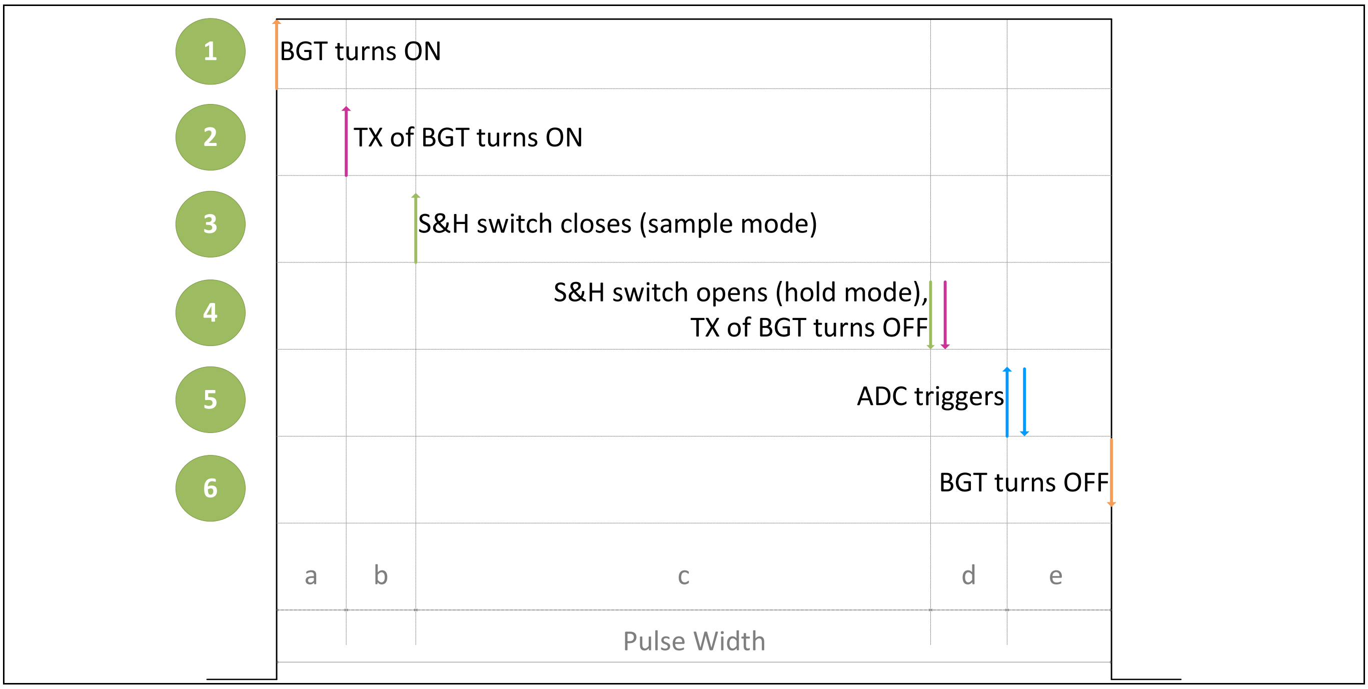


Figure 17 Pulse timing configuration

Figure 17 shows the pulse timing configuration and the steps in which the actions occur. The timings (a), (b), (d), and (e) remain fixed. If the pulse width is increased or decreased, the S&H time (c) is increased or decreased, which in turn affects the on-time of the BGT24LTR11 MMIC. For more timing information, refer to Sense2GoL Pulse the Software Guide.

4 Power consumption analysis

The BGT24LTR11 shield is designed for low-power consumption.

- The MMIC is turned on only during the 'pulse width of MMIC (t_{MMIC})' duration and remains off for the remaining time in the frame.
- The PTAT of the MMIC is turned on 1 ms before the start of the frame .This is done to make sure the V_PTAT voltage settles to keep the VCO at the center frequency before the pulses start. It is a key step to avoid out-of-band emissions. The PTAT of the MMIC consumes extra current when on. Therefore, for each pulse in the frame, the PTAT is duty cycled as per the 'pulse width of PTAT (t_{PTAT})'.
- The baseband section consists of the two stages of operational amplifiers and the voltage divider to generate 1.65 V. In order to save current consumption, the baseband section is also duty cycled and turned on 20 ms before the first sample of a frame and turned off shortly after the last sample of the frame.

As shown in Table 6, the major contributors to the power consumption are BGT24LTR11 and PTAT. The overall power consumption can be optimized by varying $N_{samples}$, pulse width and frame time.

Table 6 Power consumption overview

Component	Current consumption (mA)	On-time
BGT24LTR11 (MMIC)	45	$N_{total} \times t_{MMIC}$
PTAT	1.5	$(N_{total} \times t_{PTAT}) + 1ms$
Baseband section (Op-amps and voltage divider)	0.335	$(N_{total} - 1) \times PRT + 22ms$

In default settings, (frame time: 150 ms, t_{MMIC}: 5 µs, t_{PTAT}: 20 µs, $N_{samples}$: 128, N_{skip}: 40), the current consumption is 0.49 mA. Figure 18 shows the logic analyzer plot for the default settings.

Figure 18 On/Off timing diagram – Saleae Logic analyzer plot

5 External pin header connectors

The BGT24LTR11 shield has the provision to connect multiple headers on the edge of the board. Figure 19 shows the pin headers on the PCB, and Table 7, Table 8, Table 9, Table 10, and Table 11 describe the pins.

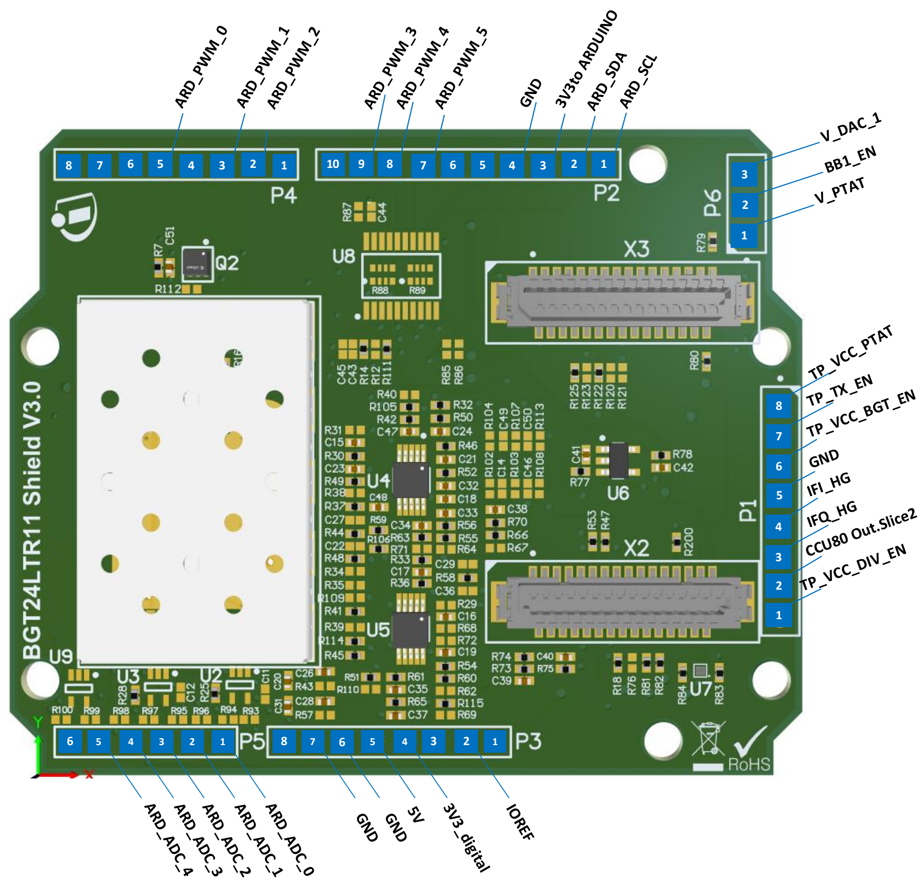


Figure 19 External headers – P1, P2, P3, P4,P5 and P6

Table 7 External headers (P1) – pin description

Pin no.	Signal name	Pin description
1	TP_VCC_DIV_EN	Control signal for VCC_DIV pin of MMIC
2	CCU80_Out.Slice2	Control signal for S&H (SPST) switches
3	IFQ_HG	Second baseband amplifier stage output for IFQ signal
4	IFI_HG	Second baseband amplifier stage output for IFI signal
5	GND	Ground
6	TP_VCC_BGT_EN	Control signal for Q1 PMOS switch to turn MMIC on/off
7	TP_TX_EN	Control signal for TX_ON pin of MMIC
8	TP_VCC_PTAT	Control signal for VCC_PTAT pin of MMIC

Table 8 External headers (P2) – pin description

Pin no.	Signal name	Pin description
1	ARD_SCL	(I2C_EEPROM.SCL) serial clock input of the EEPROM
2	ARD_SDA	(I2C_EEPROM.SDA) serial data pin of the EEPROM
3	3V3	3.3 V power supply to Arduino
4	GND	Ground
7	ARD_PWM_5	Control signal to turn on/off the 1st stage of baseband amplification
8	ARD_PWM_4	Control signal for V_PTAT
9	ARD_PWM_3	Control signal for IFI and IFQ

Table 9 External headers (P3) – pin description

Pin no.	Signal name	Pin description
2	IOREF	Voltage reference at which the external board interfacing with the Radar Baseboard MCU4 is operating
4	3V3_digital	3.3 V power supply to Arduino
5	5V	5 V power supply to Arduino
6	GND	Ground
7	GND	Ground

Table 10 External headers (P4) – pin description

Pin no.	Signal name	Pin description
2	ARD_PWM_2	VCC_PTAT_On control signal to turn PTAT on/off
3	ARD_PWM_1	TX_ON control signal for turning the TX of BGT24LTR11 on/off
5	ARD_PWM_0	VCC_ON control signal for turning the BGT24LTR11 on/off (via Q1 PMOS)

Table 11 External headers (P5) – pin description

Pin no.	Signal name	Pin description
1	ARD_ADC_0/IFI_LG	IFI_HG signal from the second baseband stage. Place R94 (0 Ω) and remove R93 to see IFI_LG signal from the first baseband stage.
2	ARD_ADC_1/IFQ_LG	IFQ_HG signal from the second baseband stage. Place R96 (0 Ω) and remove R95 to see IFQ_LG signal from the first baseband stage.
3	ARD_ADC_2	VTUNE_St_FMCW signal for stepped FMCW implementation
4	ARD_ADC_3	DIVOUT_St_FMCW signal for stepped FMCW implementation
5	ARD_ADC_4	V_PTAT output from BGT24LTR11
6	ARD_ADC_5	

Table 12 External headers (P6) – pin description

Pin no.	Signal name	Pin description
1	CCU80_Out.Slice3 (V_PTAT_S&H_EN)	Control signal for V_PTAT
2	BB1_EN	Control signal for first baseband stage.
3	V_DAC_1	Control signal for V_DAC

Note: *Pins 5, 6 of header P2 are not connected to any signal.*
Pins 1, 3, and 8 of header P3 are not connected to any signal.
Pins 1, 4, 6, 7, and 8 of header P4 are not connected to any signal.
Pin 6 of header P5 is not connected to any signal.

The pin headers enhance the functionality of the module significantly. They enable probing the analog outputs of the sensor module and probing various other signals provided to the MMIC. In principle, the accessibility of several pins on the radar MMIC and the IF signals available via the external pin headers enable interfacing the module with an external signal processor.

6 Use cases and applications

The system is capable of detecting a single target walking in front of the radar within a distance of 15 m. This can address various indoor and outdoor applications, including:

- smart door openers based on direction of movement (Figure 21)
- security camera activation when a human is approaching
- smart device activation when a human is approaching
- smart toilet automatic flushing when a human is departing.

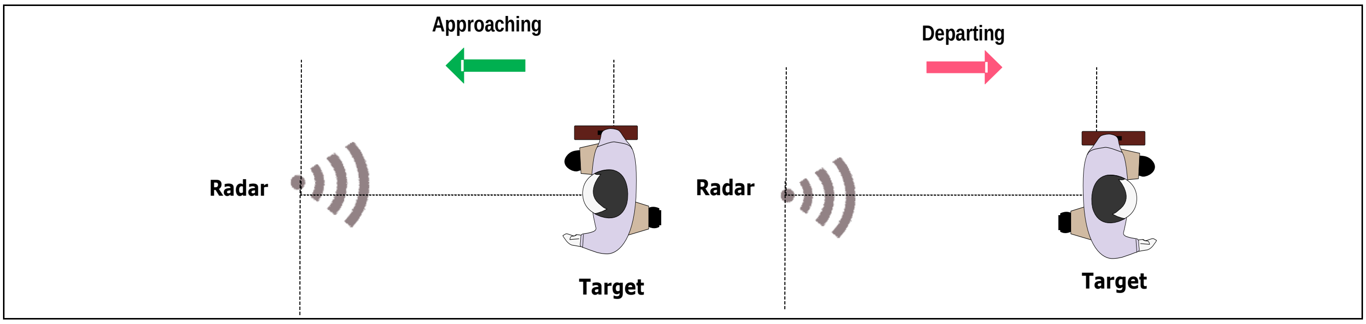


Figure 20 Human walking use case

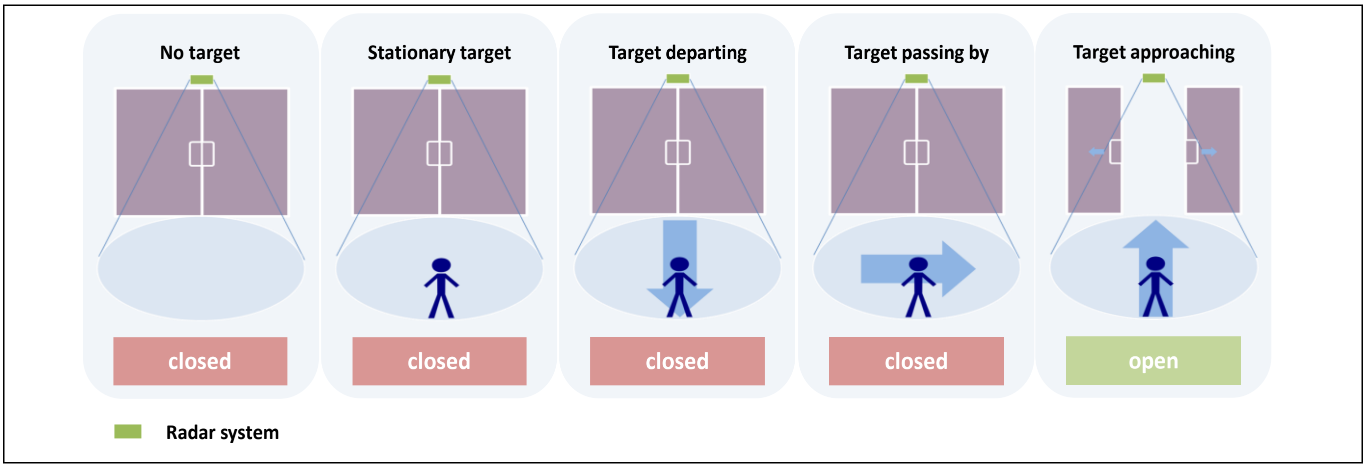


Figure 21 Smart door opener use case

Since the sensor can determine the direction of movement, it reduces the false alarms caused by regular motion triggered sensors (like PIR). Moreover, it can be hidden in the end application as it senses through non-metallic materials.

Table 13 Recommended settings for human motion detection

Parameter	Value	Comment
No. of samples per frame	≥ 128	Power of 2
Sampling frequency	≥ 1000 Hz	Based on max speed
Pulse width	≥ 4 µs	-
Frame rate	≥ 2 Hz	i.e., Frame time ≤ 500 ms

7 Measurement results

7.1 Velocity detection

Speed measurements were performed using a Doppler simulator and the Sense2GoL Pulse system for both approaching and departing configurations. The results can be seen in Figure 22.

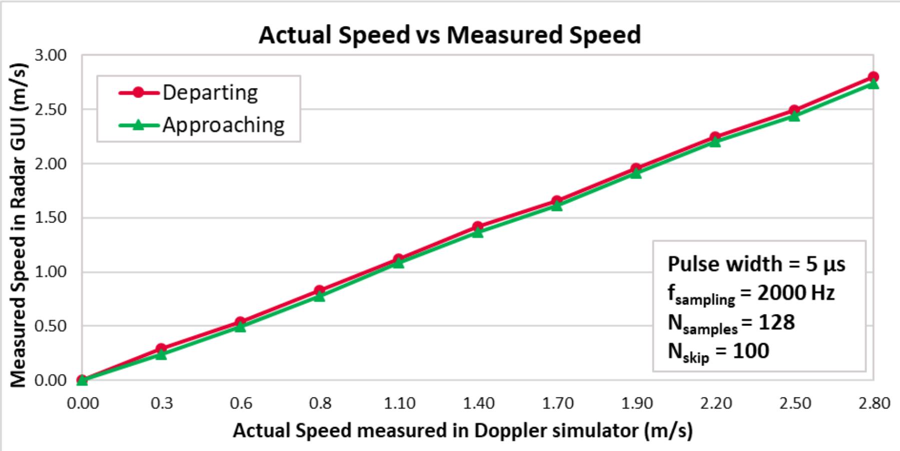


Figure 22 Speed measurements (Doppler simulator vs. radar)

The system is able to detect speeds between 0.1 and 3 m/s for the settings mentioned. For human targets, the module can detect movement up to 18 m range.

7.2 Human motion detection

The system is designed for use cases like presence detection, motion, and direction of movement detection for a single human target. It enables detection of a human walking within a distance of 20 m in an indoor or outdoor environment. Figure 23 shows the detection area for a human target.

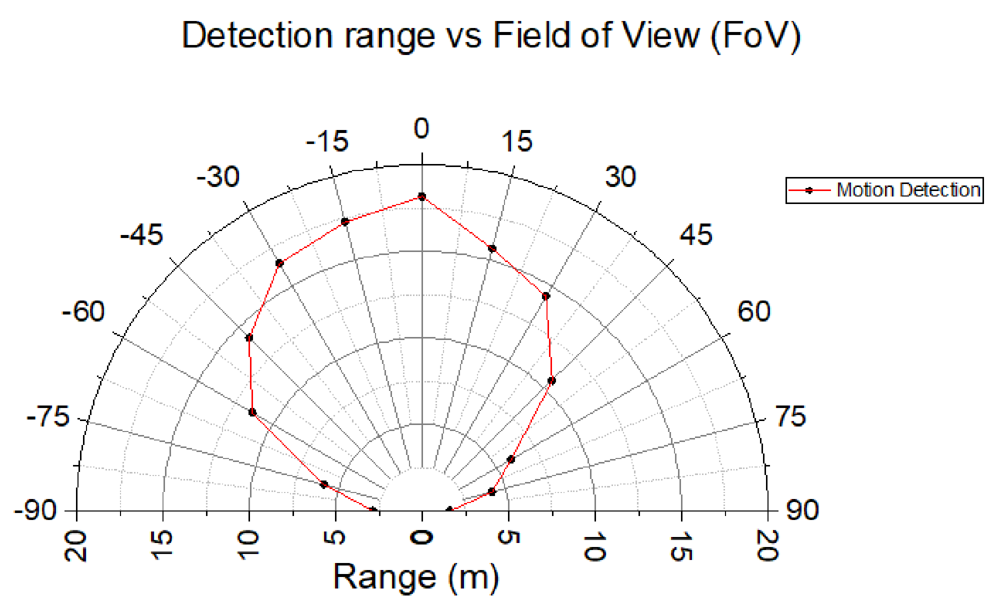


Figure 23 Motion detection area for a human target area

8 Frequency band and regulations

8.1 24 GHz regulations

Infineon's BGT24LTR11 radar sensor operates in the globally available 24 GHz bands. There is an Industrial, Scientific, and Medical (ISM) band from 24 to 24.25 GHz. However, each country may have deviating regulations in terms of occupied bandwidth, maximum allowed radiated power, conducted power, spurious emissions, etc. Therefore, it is highly recommended checking the local regulations before designing an end product.

8.2 Regulations in Europe

In Europe, the European Telecommunications Standards Institute (ETSI) defines the regulations. For more details on the ETSI standards, please refer to the document EN 300 440 V2.2.1. Please note that some countries do not follow harmonized European standards. Thus, it is recommended to check national regulations for operation within specific regions and monitor regulatory changes.

8.3 Regulations in the United States of America

In the USA, the Federal Communications Commission (FCC) defines standards and regulations. The ISM band covers 24 to 24.25 GHz and one can operate field disturbance sensors anywhere within this band within allowed power limits for certain applications. For details, please refer to FCC section number 15.245 or 15.249.

References

[1] Infineon Technologies AG. BGT24LTR11N16 MMIC Datasheet

[2] Infineon Technologies AG. XMC4700 32-bit Arm® Cortex®-M4 microcontroller Datasheet

[3] Infineon Technologies AG. BGT24LTR11N16 Product Brief

[4] Infineon Technologies AG. AN472: User's guide to BGT24LTR11N16

[5] Infineon Technologies AG. AN602: Radar Baseboard MCU4

[6] ETSI regulations. EN 300 440 V2.2.1

[7] FCC regulations. 15.245, 15.249

Revision history

Document revision	Date	Description of changes
1.00	2020-02-12	Initial version
2.00	2021-08-13	Updated HW design to V3.0
2.10	2023-02-14	Miscellaneous document cleanup updates
2.20	2023-11-07	Fixed reversed external pin header connector P1 (Figure 19 and Table 7)

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