THIS SPEC IS OBSOLETE

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Spec Title: CYPRESS POWERLINE COMMUNICATION PERFORMANCE ANALYSIS

Sunset Owner: Sree Harsha Angara (SREH)

Replaced by: None

Cypress Powerline Communication Performance Analysis

AN59464

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CY8CLED16P01
Associated Application Notes: AN55427

Application Note Abstract

Cypress's Powerline Communication (PLC) solution enables implementation of robust and reliable communication over AC and DC Powerlines. Cypress's PLC solution accelerates time-to-market by providing FCC and CENELEC compliant boards and a complete network protocol implementation. This application note describes performance tests conducted on the Cypress PLC solution to show its capability in environments characteristic of real world scenarios. The test results are useful to estimate the potential of the solution.

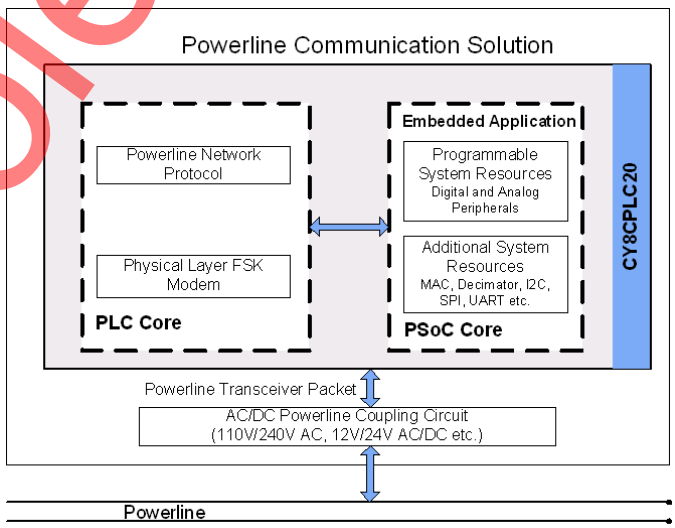
Introduction

Powerlines are a widely available communication medium all over the world for PLC technology. The pervasiveness of Powerline also makes it difficult to predict the characteristics and operation of PLC products. Because of the variable quality of Powerlines around the world, implementing robust communication over Powerline has been an engineering challenge for years. The Cypress PLC solution enables secure and reliable communication over Powerline. Cypress PLC features include:

- Integrated Powerline PHY modem with optimized filters and amplifiers to operate with high voltage and low voltage Powerlines.
- Powerline optimized network protocol that supports bidirectional communication with optional acknowledgement based signaling. In case of data packet loss due to louder noise on the Powerline, the transmitter has the capability to retransmit the data.
- The Powerline network protocol also supports 8-bit CRC for error detection.
- A Carrier Sense Multiple Access (CSMA) scheme is built into the data link layer. It avoids collision between packet transmissions from different nodes on the Powerline, supports multiple masters, and enables reliable communication on a bigger network.

A block diagram of the PLC solution with the CY8CPLC20 programmable PLC chip is shown in Figure 1.

Figure 1. Cypress PLC Solution Block Diagram



The following kits are available to evaluate the Cypress PLC solution:

- CY3272 High Voltage PLC Evaluation Kit (EVK)
- CY3273 Low Voltage PLC Evaluation Kit (EVK)
- CY3274 High Voltage Programmable PLC Development Kit (DVK)
- CY3275 Low Voltage Programmable PLC Development Kit (DVK)
- CY3276 High Voltage Programmable PLC + HB LED Control Development Kit (DVK)
- CY3277 Low Voltage Programmable PLC + HB LED Control Development Kit (DVK)

The high voltage kits CY3272, CY3274, and CY3276, are designed with the filtering and power supply circuitry to operate on 110V to 240V AC Powerlines. They are compliant to the following CENELEC and FCC standards.

- Powerline Signaling (EN50065-1:2001, FCC Part 15)
- Powerline Immunity (EN50065-2-1:2003, EN61000-3-2/3)
- Safety (EN60950)

The low voltage kits CY3273, CY3275, and CY3277, are designed to operate on 12V to 24V AC/DC Powerlines. All three low voltage kits are designed with the filtering and power supply circuitry.

The CY3272 and CY3273 kits are used to evaluate the CY8CPLC10 PLC fixed function device, which has an I^2C port for interfacing to an external host microcontroller.

The CY3274 and CY3275 kits are used to develop an embedded powerline networking application on the CY8CPLC20 programmable PLC device. They contain user interface options such as I^2C, RS232, GPIO, analog voltage, LCD display, and LED to develop a full application.

The CY3276 and CY3277 kits are used to develop a powerline controller and embedded host application with High Brightness (HB) LED control on the CY8CLED16P01 Programmable PLC + HB LED Control device. They also contain many user interface options such as I^2C, RS232, GPIO, analog voltage, LCD display, and LED to develop a full application. They have the added feature of a HB RGB LED daughter card to evaluate lighting control with powerline communication by the CY8CLED16P01 device.

The following sections describe the performance tests conducted on the Cypress PLC Solution. They are:

- Conducted Emissions, a standard test used to test the levels of communicating equipment on a public supply system.
- Noise Immunity, shows resistance to the various types of noise present on the Powerline.
- Filter Response, characterizes the transmit and receive filter used on the reference designs.
- Transmit Attenuation, shows the solution's capabilities of overcoming high attenuation.
- Power Consumption, shows the minimum current to be sourced for the power supply.

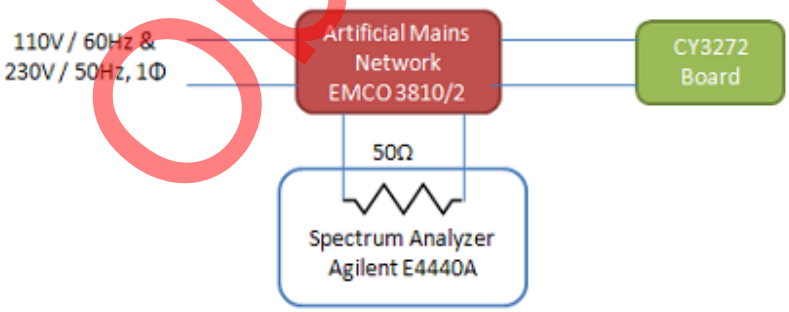
PLC Performance Tests

Conducted Emissions

This test shows how the CY3272 Board Reference Design complies with the EN50065-1:2001 standard for "signaling on low voltage installations in the frequency range 3 kHz to 148.5 kHz - Part 1: General requirements, frequency bands, and electromagnetic disturbances". This standard limits the interference caused by communication equipment to sensitive electronic equipment that operates on the same powerline.

Setup and Procedure

Figure 2. Conducted Emissions Test Setup



The EN50065-1:2001 standard describes the test setup and procedure for the Conducted Emissions test.

This test is performed using passive networks called LISNs, Line Impedance Stabilization Network, connected in series with the power lines to the equipment. The LISN establishes a consistent impedance to allow for repeatability of test results. Conducted emissions are measured using a Spectrum Analyzer connected to the measurement port on the LISN.

The spectrum analyzer is set to a resolution bandwidth of 3 kHz. This is higher than the measured spectral width of the output signal, which is 2.83 kHz. The spectrum analyzer performs a quasi-peak measurement, taken over a period of one minute and an average measurement. The test is conducted with both 110V and 230V AC mains. The summary of measurements is presented in the next section.

The modem of CY8CPLC10 chip on the CY3272 board has the following settings:

- The transmit gain is set to 125 mV_{p-p}.
- The clocking mode is set to external oscillator.
- The baud rate is set to 2400 bps and the bandwidth used is 1.5 kHz.

The CY8CPLC10 chip is then used in an internal test mode to continuously transmit packets. The external I^2C connection is not used to initiate transmissions because the unshielded connecting cable can generate excessive noise. In normal customer applications, the I^2C connection is usually on the same board and the system is in an enclosure. The graph in Figure 3 shows the results of the conducted emissions test of the CY3272 Board.

Figure 3. Conducted Emission Test Results

The dark red and blue lines show the output spectrum from 10 kHz to 24 MHz based on the quasi-peak and average measurements taken at the mains terminals of the device respectively. The light red and blue lines show the allowed limit of the spectrum as given in the EN50065-1:2001 Standard for quasi-peak and average measurements respectively.

The peak output level is measured as 119.04 dBµV on the mains output of the board. The limit of devices that transmit in the frequency range 95 kHz to 148.5 kHz is 122 dBµV. The peaks of the first and second harmonics are 57.67 dBµV and 39.59 dBµV, respectively.

Noise Immunity

The following tests show the CY3272 Board Reference Design's immunity to white noise and narrowband interference in the Cypress PLC communication frequency band. The interfering signals are chosen as they are known to be critical to the functioning of the Cypress boards. The following types of interference are used:

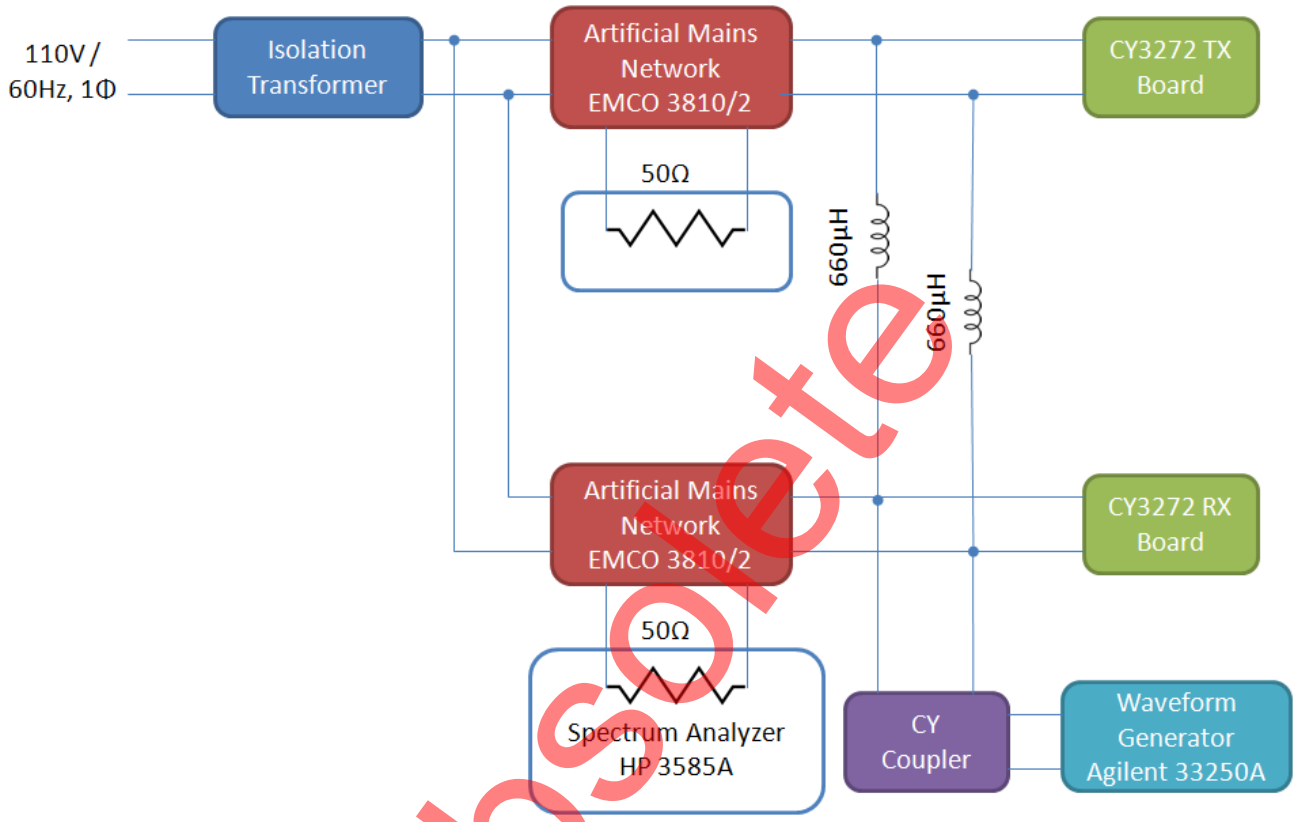
- White Noise
- Single Tone Continuous
- Single Tone Burst
- AM Modulated

These tests also show that the Cypress boards have a strong immunity against other communicating equipment and maintain electromagnetic compatibility (EMC) in residential, commercial, and light industrial environments. The goal of EMC is the correct operation, in the same electromagnetic environment, of different equipment and the avoidance of any interference effects.

Test Setup and Procedure

The setup for the test is shown in Figure 4. It is based on two CY3272 board communicating across an 110V/60 Hz, single phase power line.

Figure 4. Noise Immunity Test Setup



The CY8CPLC10 device on the CY3272 TX board is set to have a TX gain of125 mV_{p-p} and each test is conducted for two RX gains, 5 mV and 125 µV.

Packets are continuously sent in unacknowledged mode and verified using an instance of the Control Panel GUI attached to the receiver. The received signal and noise level are measured with a spectrum analyzer at the measurement port of the artificial mains network. The noise level is measured in absence of the transmitted signal.

Procedure and Results

White Noise

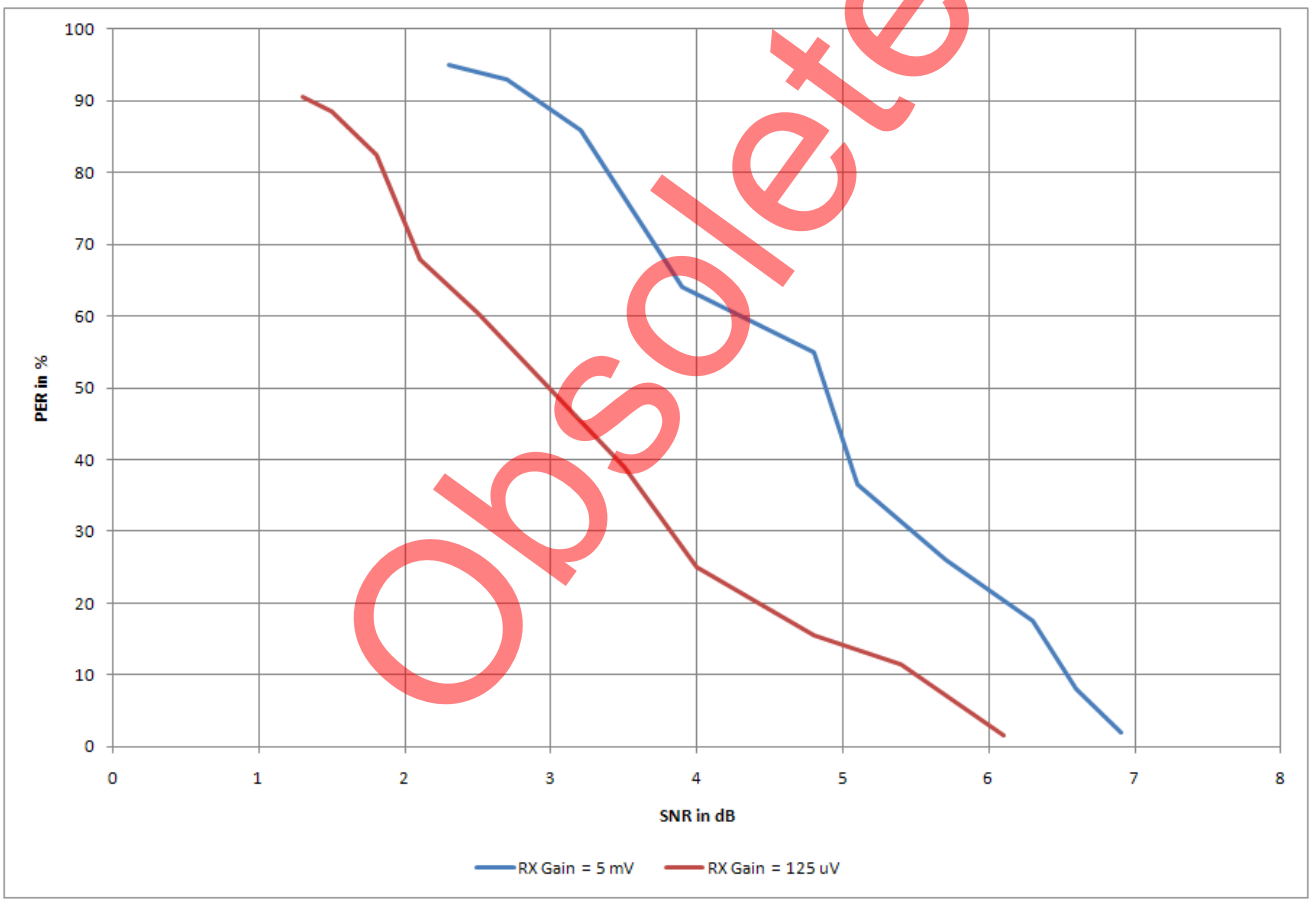
A large white noise level is injected into the Powerline from the Waveform Generator such that the number of received packets became zero. Transmission is then stopped. The largest noise level near the PLC communication frequency band is noted using the Spectrum Analyzer in the maximum amplitude measurement mode. The analyzer is then reset and kept in the same mode. Then a specific number of packets are sent from the TX to the RX board and the Packet Error Rate (PER) is noted. The PER is the total number of failed packets divided by the total number of packets sent, represented as a percentage. The received signal level is noted from the analyzer. The Signal to Noise Ratio (SNR) is now calculated. The Waveform Generator level is reduced and the test is repeated until the PER is 0%. For each level, the SNR and PER is calculated for different values of white noise in the system. The results are shown for the two RX gain values in the following graph. Note that PER is a stricter parameter than bit error rate (BER) since every bit in a packet must be correct in order for it to be successful. In these tests, an 80 bit packet is transmitted. Assuming that bit errors occur randomly, the PER can be related to the BER by the following equation:

$$PER = 1 - (1 - BER)^{Packet\_Length}$$

$$= 1 - (1 - BER)^{80}$$

For a PER of 1%, the equivalent BER would be ~10^{-4}.

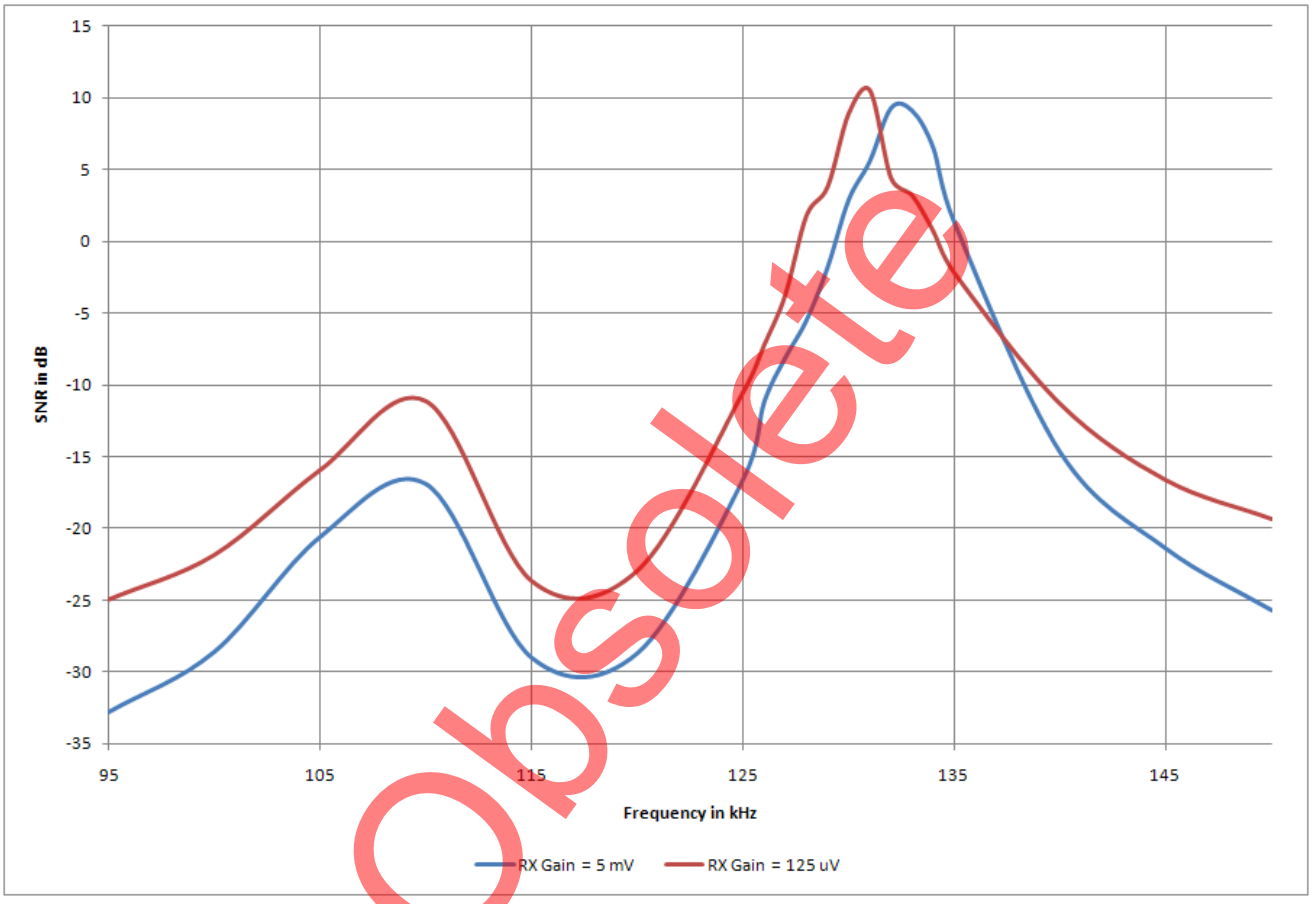
Figure 5. White Noise Test Results



Single Tone Continuous

For this test, the Waveform Generator is used to inject a sine wave into the system. For a particular frequency value, packets are continuously sent in unacknowledged mode and verified using an instance of the Control Panel GUI attached to the receiver. The amplitude of the interference is adjusted such that a PER of 1% is attained. The signal level is noted using the Spectrum Analyzer in the maximum amplitude measurement mode. Transmission is then stopped and the analyzer is reset and used to measure the noise value. For each level, the SNR is calculated for different values of the sinusoidal interference. The results are shown for the two RX gain values in the following graph.

Figure 6. Single Tone Continuous Test Results



Single Tone Burst

Burst noise is associated with other communicating equipment on the Powerline, appliances with a motor or inverter, and so on. It consists of sudden step-like transitions between two or more voltage or current levels at random and unpredictable times. To simulate this type of noise, a Waveform Generator is used to output a sine wave in bursts as 132 kHz. This is the center frequency used by Cypress's PLC solution and interference at this frequency impairs the performance of the solution. Packets are continuously sent in unacknowledged mode and verified using an instance of the Control Panel GUI attached to the receiver. Both the transmitter and the receiver use the default modem options, i.e., 1.55 V_{p-p} TX Gain, 5 mV RX Gain and a bandwidth of 3 kHz. Using the Waveform Generator, an interfering signal at the communication frequency 132 kHz is continuously increased from 0 mV to a level where a 100% PER is achieved. The level of the interfering signal is then increased by 10 dB. The Waveform Generator is then changed to the Burst mode and the number of cycles is set to 100 Hz. The Burst Period is adjusted to achieve a PER of 1%. The test is repeated for two baud rates, 2400 bps and 600, and two cycle frequencies, 100 Hz and 120 Hz. The results for the test are given as follows.

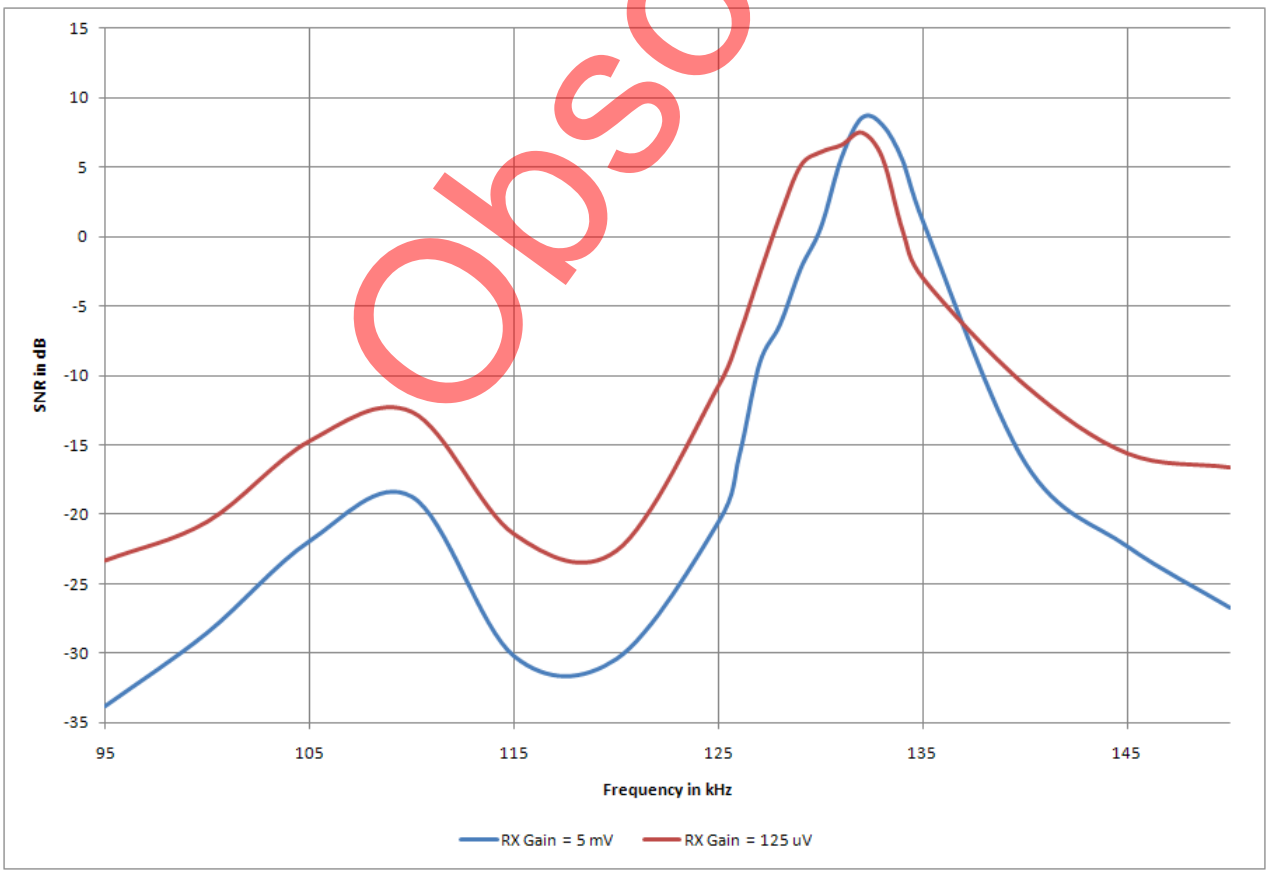
Table 1. Single Tone Burst Test Results

Baud Rates (bps)	Number of Cycles (Hz)	Burst Period (seconds)
600	100	1
600	120	1.3
2400	100	1.5
2400	120	1.8

AM Modulated

The procedure for this test is similar to that of the Single Tone Continuous test but the interfering signal used in this test is an AM Modulated sine wave with a modulation frequency of 1 kHz and depth of 80%. The following graph shows a plot of SNR against frequency at two different RX gains.

Figure 7. AM Modulated Test Results



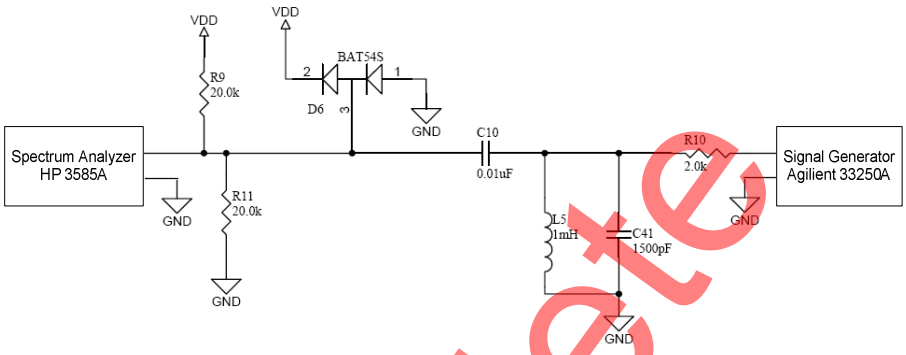
Filter Frequency Response

The coupling circuit on the CY3272 Reference Board consists of two filters: an active TX filter and amplifier and a passive RX filter. The object of this test is to show the frequency response of both these filters. More information on the design of the filter circuits including the selection of critical components for meeting performance and compliance requirements is available in the application note AN55427 – *Cypress Powerline Communication Board Design Analysis*.

RX Filter Frequency Response

The receive filter comprises of components L5 and C41, in combination with R10. It rejects some of out-of-band interference, such as AM broadcast signals that may be coupled from the line and may otherwise swamp the PLC device's internal receiver circuitry. Resistors R9 and R11 set the VCC/2 bias voltage required on the receive pin of the PLC device.

Figure 8. RX Filter Frequency Response Test Setup



A Signal Generator is used to sweep a 50 mV_{p-p} sine wave into the filter circuit on a CY3272 Reference Board. The response is measured at the input and output using a Spectrum Analyzer as shown in Figure 8.

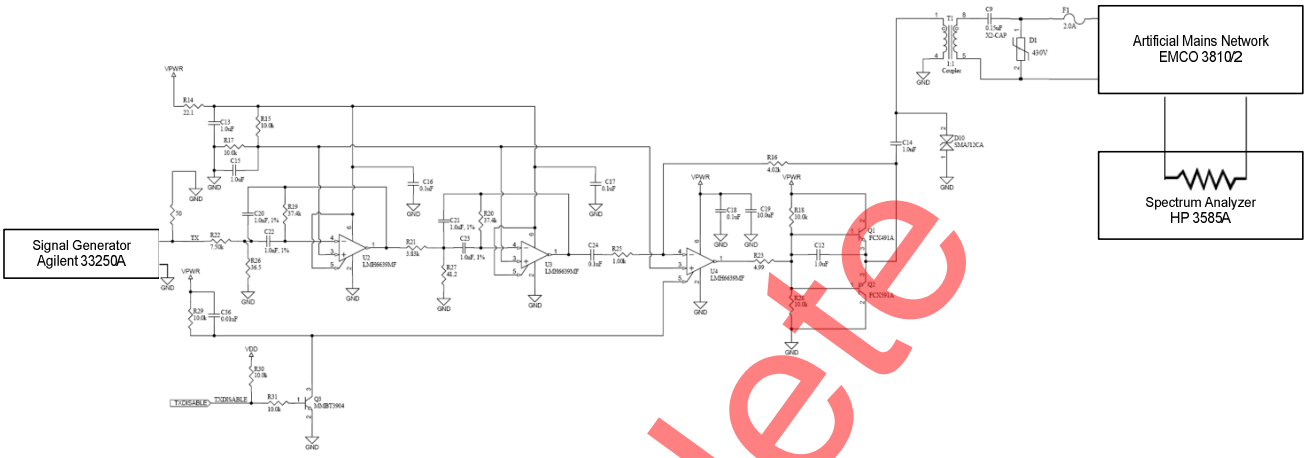
Figure 9. RX Filter Response

In the curve in Figure 9, observe that the RX filter attenuates the signal by about 3.5 dB at 132 kHz

TX Filter and Amplifier Frequency Response

The FSK transmit signal TX is generated on the FSK_OUT pin of the Cypress PLC device. This signal is applied to the input of an external transmit filter block consisting of op-amps U2 and U3, and their related passive components. The filtered transmit data signal passes through the power amplifier, which consists of op-amp U4, transistors Q1 and Q2, and associated passive components.

Figure 10. TX Filter and Amplifier Frequency Response Test Setup



The circuit is loaded with a CISPR compliant network as shown in Figure 10. A Signal Generator is connected to resistor R22 across a 50Ω load and used to sweep a 50 mV_{p-p} sine wave into the filter circuit on a CY3272 Reference Board. The response is measured by a Spectrum Analyzer and is shown in the following figure

Figure 11. TX Filter and Amplifier Response

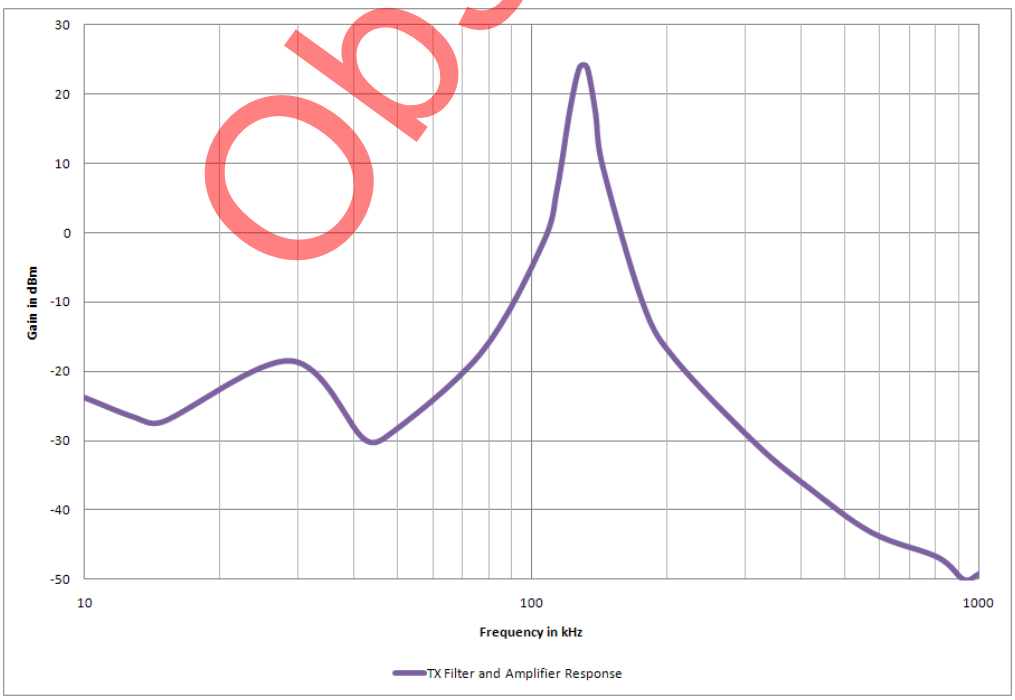


Figure 11 shows the measured response of the TX circuit. When loaded with the CISPR network, there is a gain of around 24 dB around the transmission carrier frequency

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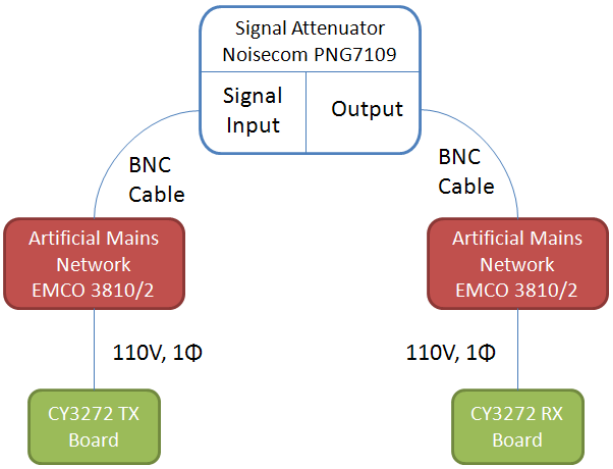
Transmit Attenuation

The object of this test is to show how the CY3272 Board Reference Design is capable of overcoming high attenuation and cross phases reliably.

Setup and Procedure

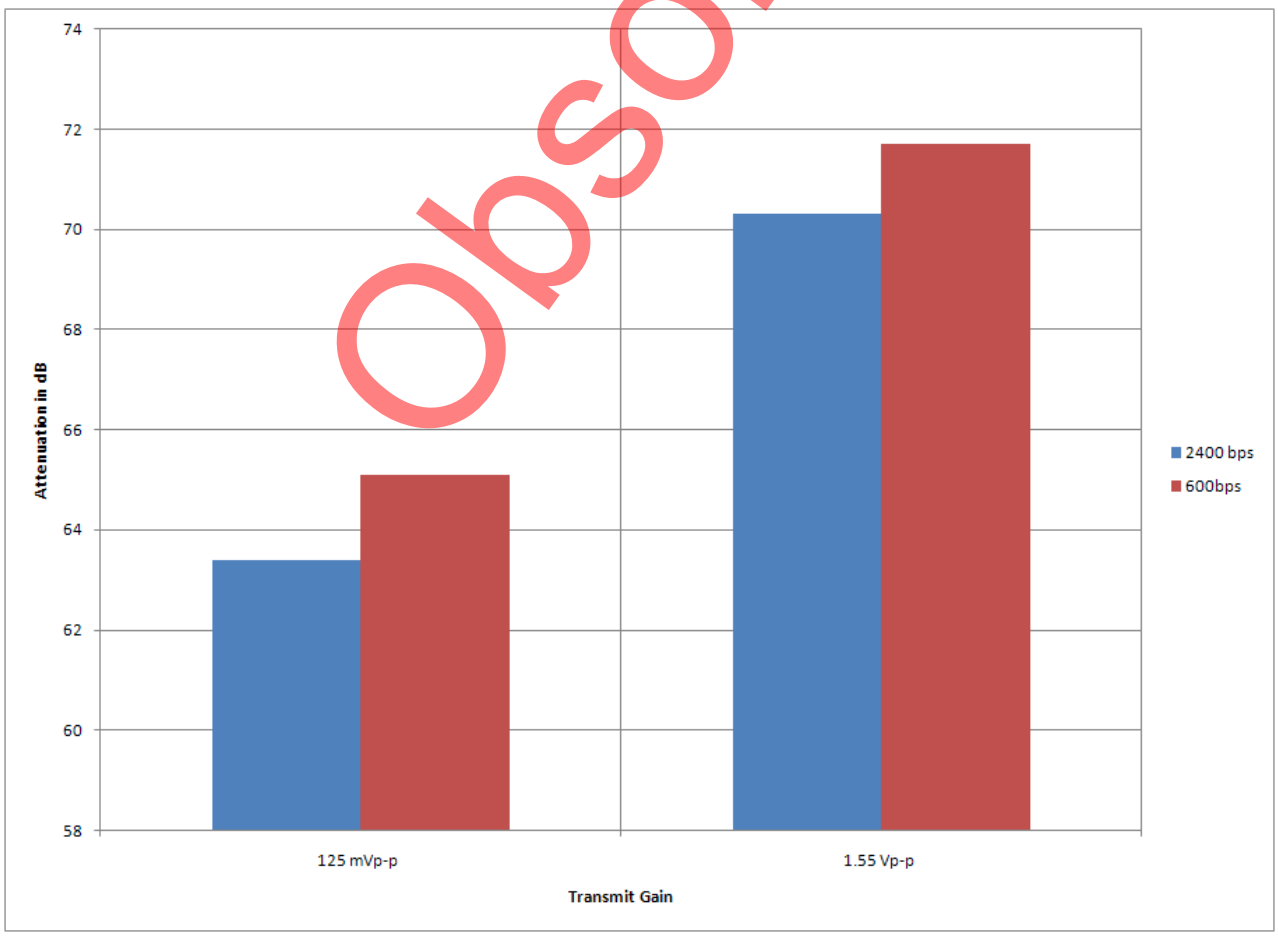
Figure 12. Transmit Attenuation Test Setup



The signal attenuator used is a Noisecom 7109 which has a low distortion signal path. The attenuation can be changed in steps of 1 dB up to a maximum of 127 dB.

Packets are sent from the TX board to the RX board using the default modem settings. This test is done with two values of TX gain, 125 mV_{p-p} and 1.55 V_{p-p} and two values of baud rate, 600 bps and 2400 bps. The two gain values correspond to an amplitude of 118.5 dBµV for 125 mV_{p-p} and 126.5 dBµV for the 1.55 V_{p-p} on the line. Packets are continuously sent in unacknowledged mode and verified using an instance of the Control Panel GUI attached to the receiver. The attenuation factor is increased from 0 dB until a level where a PER of 1% is measured. A Spectrum Analyzer is then attached to the 50Ω monitor on the RX Board Mains Network and the peak level of the received signal is measured. The analyzer is then attached to the 50Ω monitor on the TX Board Mains Network and the peak level of the transmitted signal is measured. The difference between the two measurements is the transmit attenuation and is shown in Figure 13. This graph shows that at a TX gain of 125 mV_{p-p} the signal attenuates by ~63 dB and is still received by another node. At a gain of 1.55 V_{p-p} it can get attenuated by ~70 dB. If the baud rate is decreased from 2400 bps to 600 bps, the signal can get attenuated by a further 1.5 dB before the packet success rate begins to get affected.

Figure 13. Transmit Attenuation Test Results



Power Consumption

This section deals with the power consumed by the CY3272 High Voltage and CY3273 Low Voltage Evaluation Boards coupling circuit during normal operation. The power supply for the coupling circuit is derived from the VPWR supply. For the CY3272 board, VPWR is 10V and for the CY3273 it is 5V.

Setup and Procedure

Figure 14. Power Measurement Setup for CY3272 Board

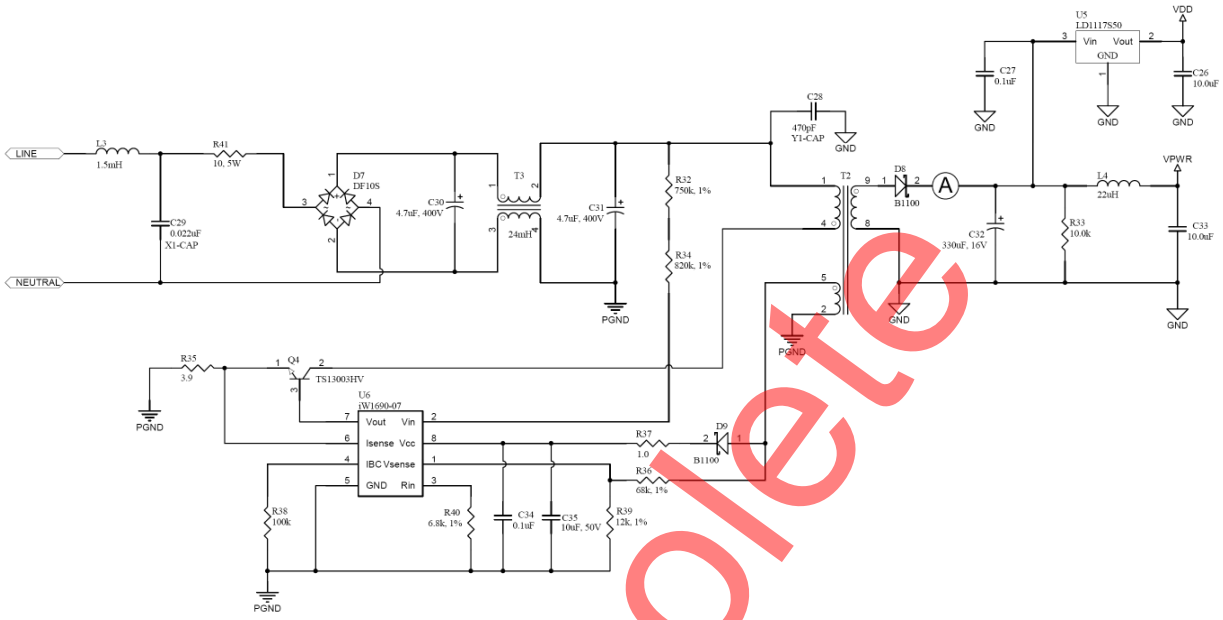
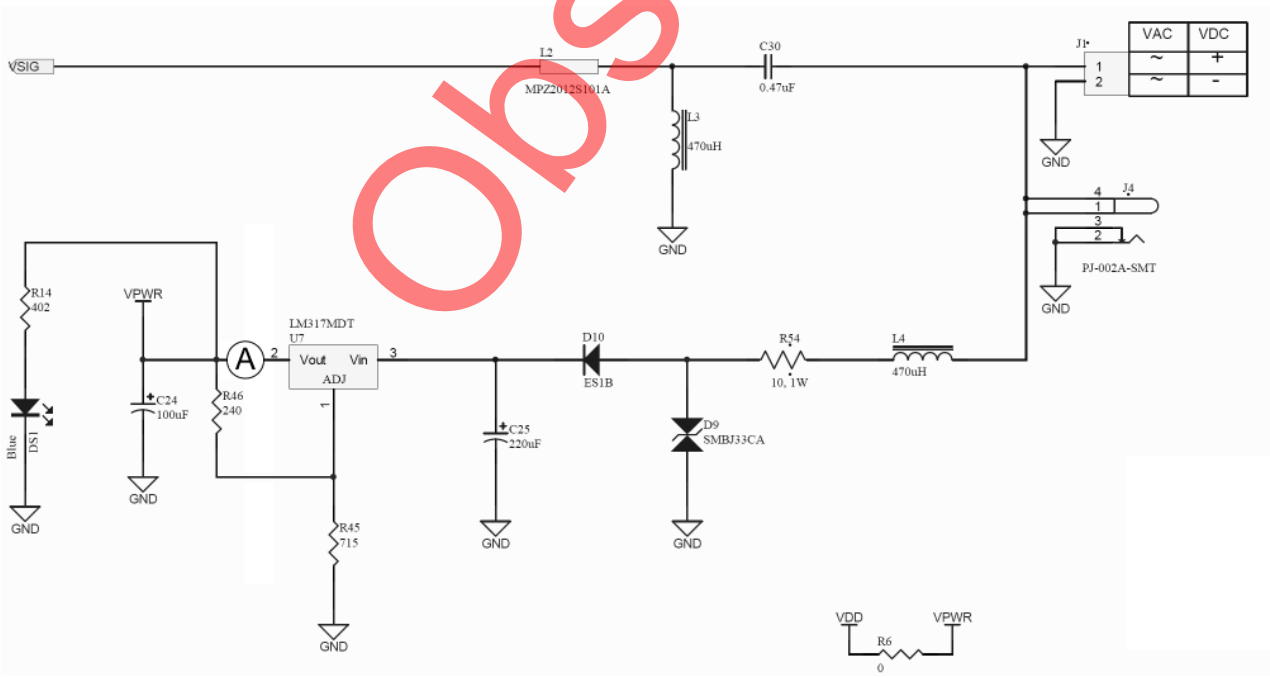


Figure 15. Power Measurement Setup for CY3273 Board



As shown in the circuit diagrams for the CY3272 and CY3273 boards, an ammeter is placed at the output of the power source for the VPWR supply. For the CY3272, the iWatt iW1690 power controller performs the AC to DC conversion and provides a stable 10V DC output. On the CY3273, the LM317MDT regulator provides the power. This test is done with two values of TX gain, 125 mV_{p-p} and 1.55 V_{p-p}.

Results

Table 2. Results for the CY3272 Board

Clocking Mode		External 32.768 kHz Crystal		External 24 MHz Oscillator	
Power Parameters	Voltage (V)	Current (mA)	Power (W)	Current (mA)	Power (W)
Idle Mode[1]	10V	31	0.31	35	0.35
RX Mode	10V	70	0.7	63	0.63
TX Mode at a Gain of 1.55 Vp-p	10V	89	0.89	82	0.82
TX Mode at a Gain of 125 mVp-p	10V	70	0.7	63	0.63

Table 3. Results for the CY3273 Board

Clocking Mode		External 32.768 kHz Crystal		External 24 MHz Oscillator	
Power Parameters	Voltage (V)	Current (mA)	Power (W)	Current (mA)	Power (W)
Idle Mode[1]	5V	25	0.125	28	0.14
RX Mode	5V	66	0.33	58	0.29
TX Mode at a Gain of 1.55 Vp-p	5V	191	0.955	184	0.92
TX Mode at a Gain of 125 mVp-p	5V	69	0.345	62	0.31

Note

1. This is preliminary data. Idle Mode requires circuit and firmware modifications. An application note on how to implement this mode will be made available in May 2010.

These results show that using an external oscillator source reduces current consumption in receive mode and transmit mode each by ~7-8 mA. Using a higher TX gain requires more current to be drawn from the supply to power the transmit amplifier section of the coupling circuit.

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**	2880534	RARP	02/26/10	New application note
*A	3928973	ADIY	03/15/2013	No content update.
*B	4717929	SREH	04/09/2015	Obsoleting application note as the data is based off an obsolete kit CY3272

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