AN55663

Migrating from CY14E256L/STK14C88 to CY14E256LA

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Associated Project: No
Associated Part Family: CY14E256L/STK14C88
CY14E256LA
Software Version: None
Related Application Notes: None

AN55663 provides details for migrating from the CY14E256L/STK14C88 nvSRAM parts to CY14E256LA part in applications. This application note also lists the parameter differences between the parts and the design considerations for migration when converting applications to CY14E256LA.

Introduction

Cypress CY14E256LA is a 5 V, 256 Kbit (32 K x 8) nvSRAM in 0.13 micron technology. This part with a few performance enhancements is functionally equivalent to CY14E256L/STK14C88 in 0.8 micron technology but with a few differences in parameters. This application note highlights the differences between the CY14E256L/STK14C88 and the CY14E256LA and the parameters that must be considered while migrating.

Note STK14C88 is the Simtek part number for CY14E256L.

Overview

The following tables compare the features and parameters of the two parts. As shown in Table 1, the 256 Kbit nvSRAM is available in x8 configuration.

Table 1. Part Number Description

Description	Original Part Number	Replacement Part Number
32 K x 8	CY14E256L/STK14C88	CY14E256LA

Feature Set

Both the parts share the same overall feature set and are available in the operation speed bins given in Table 2.

Table 2. Feature Set Comparison

Feature Set	CY14E256L/ STK14C88	CY14E256LA
AutoStore	Available	Available
Software STORE	Available	Available
Hardware STORE	Available	Available
Software RECALL	Available	Available
AutoStore Inhibit	Available	Not Available
AutoStore Enable/Disable	Not Available	Available
Preventing STORE on the fly	Available	Not Available
Speed	25 ns 35 ns 45 ns	25 ns - 45 ns
STORE Cycles	1,000,000	1,000,000
Data Retention	100 years at 55 °C	20 years at 85 °C

Operating Temperature Range

While CY14E256L/STK14C88 is available in both commercial and industrial temperature ranges, CY14E256LA is offered only in the industrial temperature range.

Table 3. Operating Temperature Range Comparison

Operating Temperature Range	CY14E256L/ STK14C88	CY14E256LA
Commercial (0 to 70 °C)	Available	Not Available
Industrial (–40 to 85 °C)	Available	Available

Packages

CY14E256LA is pin compatible with CY14E256L/STK14C88 and is available in the same packages and pin configurations, and in additional packages.

Table 4. Packages Comparison

Package	CY14E256L/ STK14C88	CY14E256LA
32-pin SOIC	Available	Available
32-pin CDIP	Available	Not Available
44-pin TSOPII	Not Available	Available

Parameters

The CY14E256LA is a pin compatible replacement for CY14E256L/STK14C88 and will require minimum changes in the application board in most applications. However, the differences in parameters should be considered before replacing one part with the other. Table 5 lists the differences in parameters between CY14E256L/STK14C88 and CY14E256LA.

Table 5. Parameter Comparison

Parameter	Description	Speed	CY14E256L/ STK14C88		CY14E256LA		Unit
			Min	Max	Min	Max	
DC Parameters							
I_{CC1}	Average V_{CC} Current	25 ns	-	100	-	70	mA
		35 ns	-	85	-	-	
		45 ns	-	70	-	52	
I_{CC2}	Average V_{CC} Current during STORE	-	-	3	-	10	mA
I_{CC3}	Average V_{CC} Current at t_{RC} = 200 ns, 5 V, 25 °C	-	10 (typ)		35 (typ)		
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle	-	-	2	-	8	mA
I_{SB1}	Average V_{CC} Standby Current (Standby, Cycling Input)	25 ns	-	31	Not specified		mA
		35 ns	-	26			
		45 ns	-	23			
I_{SB}	V_{CC} Standby Current	-	-	1.5	-	8	mA
I_{IX}	Input Leakage Current	-	–5	+5	–1	+1	uA
V_{IH}	Input High Voltage	-	2.2		2	-	V
V_{OH}	Output HIGH Voltage	-	-	2.4 (I_{OUT} = –4 mA)	-	2.4 (I_{OUT} = –2 mA)	V
V_{OL}	Output LOW Voltage	-	-	0.4 (I_{OUT} = 8 mA)	-	0.4 (I_{OUT} = 4 mA)	V
V_{CAP}	Storage Capacitor	-	54 to 260		61 to 180		µF
AC Switching Parameters							
t_{DOE}	Output Enable to Data Valid	25 ns	-	10	-	12	ns
		35 ns	-	15	-	-	
		45 ns	-	20	-	20	
t_{OHA}	Output Hold After Address Change	-	5	-	3	-	ns
t_{LZCE}	Chip Enable to Output Active	-	5	-	3	-	ns
t_{LZWE}	Output Active After End of Write	-	5	-	3	-	ns
AutoStore / Power-Up RECALL Parameters							
$t_{HRECALL}$	Power-Up RECALL Duration	-	-	0.55	-	20	ms
t_{STORE}	STORE Cycle Duration	-	-	10	-	8	ms
t_{VSBL}	Low Voltage Trigger (V_{SWITCH}) to $\overline{HSB}$ low	-	-	300	-	25	ns
V_{RESET}	Low Voltage Reset Level	-	-	3.6	Not Applicable		V
V_{SWITCH}	Low Voltage Trigger Level	-	4.0	4.5	-	4.4	V
t_{DELAY}	Time Allowed to Complete SRAM Write Cycle	-	1,000	-	-	25	ns

Parameter	Description	Speed	CY14E256L/ STK14C88		CY14E256LA		Unit
			Min	Max	Min	Max	
V_{HDIS}	$\overline{HSB}$ Output Disable Voltage	-	Not specified		-	1.9	V
t_{LZHSB}	$\overline{HSB}$ To Output Active Time	-	Not specified		-	5	µs
t_{HHHD}	$\overline{HSB}$ High Active Time	-	Not specified		-	500	ns
Software Controlled STORE/RECALL cycle Parameters							
t_{HA}	Address Hold Time	-	20	-	0	-	ns
t_{RECALL}	RECALL Duration	-	-	20	-	200	µs
Hardware STORE cycle Parameters							
t_{HLBL}	$\overline{HSB}$ LOW to STORE Busy	-	-	300	-	25 (t_{DELAY})	ns
t_{DHSB}	$\overline{HSB}$ To Output Active Time when write latch not set	-	Not specified		-	25	ns

Critical Considerations

The impact of the differences in CY14E256LA with respect to the CY14E256/STK14C88 in existing applications are discussed in this section. System designers are recommended to review the detailed datasheets when migrating to the new part.

DC Parameters

I_{CC1} (Average current at full speed) is lower in CY14E256LA and hence power supply design in applications with CY14E256L/STK14C88 would require no changes when replacing the nvSRAM with the CY14E256LA in spite of the higher values in the lower speed / higher standby current. The critical parameter to consider is the V_{CAP}.

V_{CAP}

While most of the differences do not impact the application, the difference in V_{CAP} is a critical consideration while converting from the older rev parts. V_{CAP} is the capacitor that provides the required charge for AutoStore to complete NV store of the SRAM data during power down. The required capacitor range is different for the two parts.

Table 6. V_{CAP} Comparison

Description	CY14E256L/ STK14C88	CY14E256LA
V_{CAP}	54 µF to 260 µF	61 µF to 180 µF

Therefore, any existing application which uses a capacitor value outside the overlapping range (61 µF to 180 µF) the impact of capacitor dimensions needs to be considered while changing to the new capacitor.

Note The capacitor range is the absolute value of the capacitor, net of tolerence.

AC Switching Parameters

There are a few minor differences in switching parameters between the CY14E256LA and the CY14E256L/STK14C88 as listed in the Table 5 on page 2. However, these differences do not impact most applications. For replacing 35 ns speed parts, choose the 25 ns speed parts as replacement (since 35 ns speed grade is not available in the CY14E256LA).

AutoStore / Power-Up RECALL Parameters

$t_{HRECALL}$

The power-up RECALL is much different in the CY14E256LA compared to the CY14E256L/STK14C88 because of architecture differences.

Table 7. $t_{HRECALL}$ Comparison

Description	CY14E256L/ STK14C88	CY14E256LA
$t_{HRECALL}$	550 µs	20 ms

This difference is not likely to affect applications since the initialization of the controller on the board happens at the same time. However, this should be taken into consideration when replacing the CY14E256L/STK14C88 with CY14E256LA.

Software Controlled STORE/RECALL Cycle Parameters

The Software cycle parameter t_{RECALL} is different in CY14E256LA as described below. The software address sequences are identical to that in the CY14E256L/ STK14C88 parts.

t_{RECALL}

Software RECALL time (t_{RECALL}) is higher in CY14E256LA.

Table 8. t_{RECALL} Comparison

Description	CY14E256L/ STK14C88	CY14E256LA
t_{RECALL}	20 µs	200 µs

This difference could require firmware change in the existing application to increase the controller wait state when software RECALL is initiated.

Software Sequence

The CY14E256LA has been designed to be compatible with the CY14E256L/STK14C88 in the software sequence modes. Hence, the same Software STORE and RECALL address sequences in CY14E256L/STK14C88 works in CY14E256LA, requiring no firmware change. However, there is a difference in the required state of $\overline{OE}$ / $\overline{G}$ during the software sequence reads as explained further.

In the CY14E256L/STK14C88 while software sequence must be clocked with $\overline{CE}$ / $\overline{E}$ controlled reads it is not necessary that $\overline{OE}$ / $\overline{G}$ be low for the sequence to be valid. That is, it is not necessary that the read is a real read with $\overline{OE}$ / $\overline{G}$ held LOW. But, in the CY14E256LA the software sequence may be clocked with $\overline{CE}$ controlled reads or $\overline{OE}$ controlled reads. This means that while in the CY14E256L/STK14C88 parts $\overline{OE}$ / $\overline{G}$ state was immaterial, in the CY14E256LA parts, $\overline{OE}$ needs to be LOW for a valid software sequence read. It does not matter if $\overline{CE}$ goes LOW first or $\overline{OE}$ goes LOW first but the read is valid for software sequence only when both $\overline{CE}$ and $\overline{OE}$ have gone LOW. In both the CY14E256L/STK14C88 and the CY14E256LA parts $\overline{WE}$ must be kept HIGH for all the six read sequences.

In effect, this difference will affect applications where software sequence reads are done with $\overline{OE}$ / $\overline{G}$ held HIGH. Firmware change will be required to take $\overline{OE}$ LOW when using the new part CY14E256LA. Applications where software sequence reads are performed with $\overline{OE}$ / $\overline{G}$ LOW do not require any change.

Hardware STORE cycle Parameters

The Hardware STORE parameters are improved in the CY14E256LA. The improvements are listed under the Details of Improvement section. No changes will be required in applications.

AutoStore Inhibit

The CY14E256L/STK14C88 has the AutoStore Inhibit feature and the CY14E256LA has AutoStore Disable mode. These two provide the same result of AutoStore disable but are done by different means – hardware in CY14E256L/ STK14C88 and software in CY14E256LA.

To disable AutoStore in CY14E256L/STK14C88, the power is to be connected to the V_{CAP} pin and the V_{CC} pin is grounded (or left open). This cannot be done in CY14E256LA. For proper operation of the device, in CY14E256LA, power is to be connected to the V_{CC} pin only. However, AutoStore disable is more easily done through the software sequence. Therefore, if the CY14E256L/ STK14C88 is to be replaced in an application where AutoStore has been disabled, then the layout has to be modified to connect the power to the V_{CC} pin and a software sequence has to be used to disable AutoStore function followed by a Software STORE, the first time the board is powered up.

Preventing STORE

In the CY14E256L/STK14C88, STORE function can be disabled on the fly by holding $\overline{HSB}$ pin HIGH at the onset of STORE with a driver capable of sourcing 30 mA at a V_{OH} of at least 2.2 V. This feature is not available in the 0.13 µ parts. In the CY14E256LA, a STORE initiated by any means, cannot be disabled on the fly.

Data Retention

The Data Retention in CY14E256LA part is improved from the older technology part. The CY14E256LA has data retention of 20 years at 85 °C against the CY14E256L/ STK14C88 data retention of 100 years at 55 °C. This would translate to over four times improvement in data retention at the same temperatures.

Details of Improvement

Hardware STORE Related Improvements

$\overline{HSB}$ pin (Hardware STORE Busy Indication/Hardware STORE Initiation)

The $\overline{HSB}$ pin of the nvSRAM is an open drain I/O pin (internal 100 KΩ weak pull-up resistor) used to indicate or initiate a STORE operation. When a STORE operation is in progress, nvSRAM pulls the $\overline{HSB}$ pin low to indicate that the device is busy and cannot be accessed for read/write operation. During normal operation, the $\overline{HSB}$ pin can be pulled low to initiate a Hardware STORE operation.

As shown in Table 5 on page 2, several timing parameters related to the $\overline{HSB}$ pin input and output have changed from CY14E256L/STK14C88 to CY14E256LA. All of these changes are improvements from the original part specification and should be considered as added benefits in your system while migrating to the new part number.

T_{DELAY}

If a write latch is set and the $\overline{HSB}$ pin is pulled low, CY14E256L/STK14C88 enables 1 µs time for write operations to complete before STORE operation begins and reads and writes are inhibited. This potentially enables inadvertent data to be written to the nvSRAM during the t_{DELAY} duration.

Note Write Latch: When a write operation is done, a 'write latch' is set internally. When $\overline{HSB}$ is pulled low, nvSRAM checks this write latch before initiating a STORE. This is done to prevent any unnecessary loss of endurance cycles.

In CY14E256LA, the t_{DELAY} parameter enables only one write cycle time for any ongoing write to complete after $\overline{HSB}$ pin is pulled low. This improvement provides better security from inadvertent write operations.

Also, if $\overline{HSB}$ pin is pulled low externally for a minimum of t_{PHSB} time on CY14E256LA, the output driver of $\overline{HSB}$ pin pulls the pin low only indicating a STORE operation within 25 ns (t_{DELAY}). This parameter for $\overline{HSB}$ low to STORE busy is not specified in the CY14E256L/STK14C88. (See Figure 1 and Figure 2)

$\overline{HSB}$ LOW when write latch not set:

If no writes are performed since the last STORE/RECALL operation, STORE operation does not start when $\overline{HSB}$ is pulled low. However, the $\overline{HSB}$ pin is still internally pulled low for 1 µs (t_{DELAY}) time in the CY14E256L/ STK14C88 device.

CY14E256LA device does not pull the $\overline{HSB}$ pin low internally if write latch is not set. This improvement prevents the possibility of being in an infinite loop when $\overline{HSB}$ pins of two nvSRAM devices are ganged.

Figure 1. CY14E256L/STK14C88: AC Parameters Related to $\overline{HSB}$

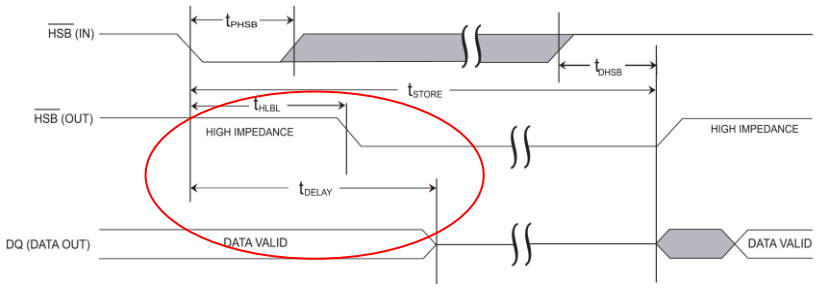
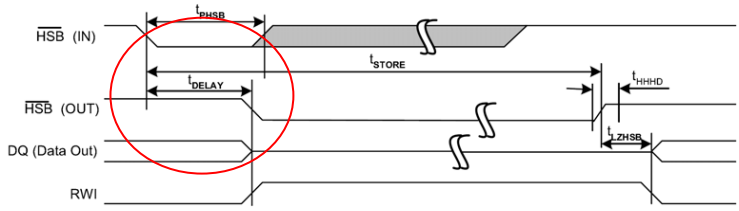
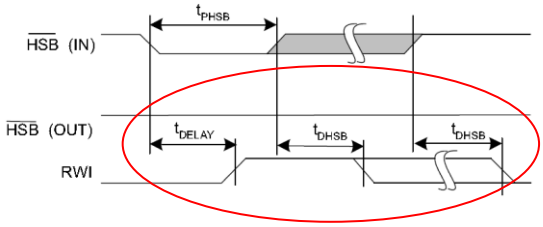


Figure 2. CY14E256LA: AC Parameters Related to $\overline{HSB}$

Write Latch Set



Write Latch not Set



Power-up Recall Related Improvements

Additional parameters are specified in CY14E256LA such as $\overline{HSB}$ Output Disable Voltage (V_{HDIS}), $\overline{HSB}$ To Output Active Time (t_{LZHSB}), and $\overline{HSB}$ High Active Time (t_{HHHD}), which helps in system design. See Figure 3 and Figure 4 for the definition of the additional specs in power-up. Also, note that $\overline{HSB}$ remains low until the end of the power-up in the new part. This would guard against the system inadvertently thinking the part has completed the boot up prior to real completion.

Figure 3. CY14E256L/STK14C88: Power-Up Recall

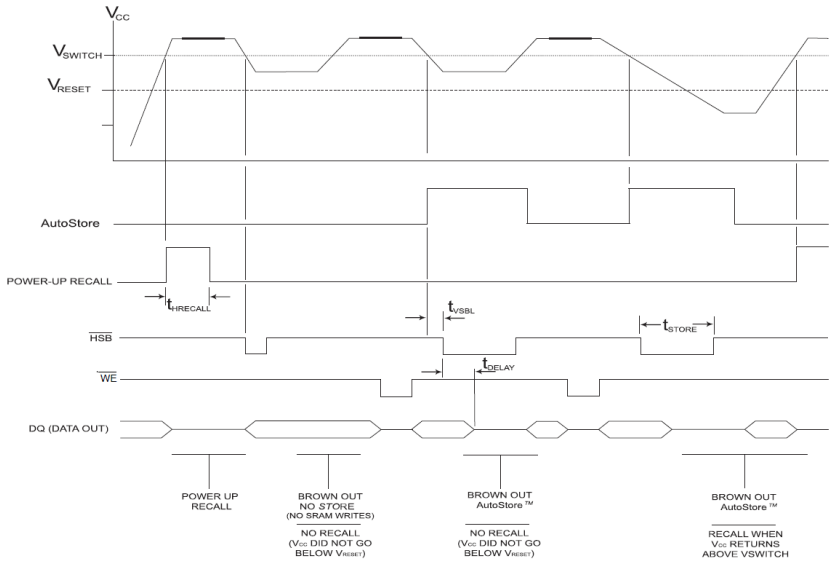
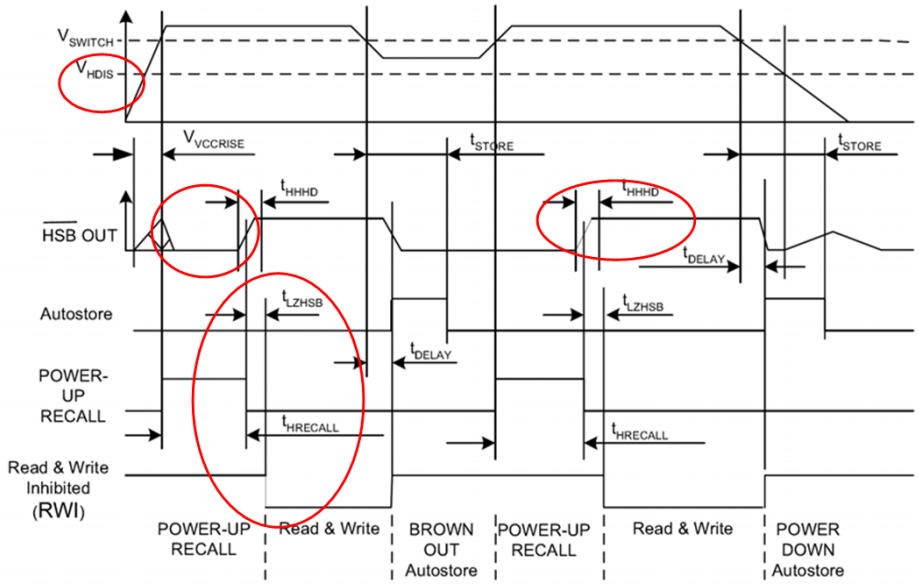


Figure 4. CY14E256LA: Power-Up Recall



Summary

The application note discusses the differences between CY14E256LA in the latest 0.13 micron technology and CY14E256L/STK14C88 in the 0.8 micron technology. Several parameters related to $\overline{HSB}$ and power-up have improved / specified in the new device enabling faster device response, greater data security, and ease of design.

CY14E256LA is pin compatible with and can replace the CY14E256L/STK14C88 device with minimum changes hardware/firmware in most applications. Applications where CY14E256L/STK14C88 is in AutoStore inhibit mode would require layout changes, and also, it is not possible to prevent STORE on the fly in the CY14E256LA. The value of V_{CAP} in the existing design needs to be considered while replacing the part.

Document History

Document Title: Migrating from CY14E256L/STK14C88 to CY14E256LA – AN55663

Document Number: 001-55663

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2773126	PSR	10/01/09	New Spec.
*A	3016464	PSR	09/27/10	Updated Introduction in page 1. Added a feature, Preventing STORE on the fly, to Table 2 in page 1 and added a paragraph under Critical Consideration in page 5 indicating this feature difference. Changed STORE cycles of CY14E256LA in Table 2 in page 1 to 1,000,000 and deleted the STORE cycles paragraph under Critical Consideration since the parts are identical in this. Changed ICC4 and ISB of CY14E256LA in Table 5 in page 2 to 8mA to align with datasheet spec. Updated Summary in page 7.
*B	3223418	PSR	04/12/11	Added $\overline{OE}$ requirement differences in Software Sequence section in page 3, 4
*C	3618997	PSR	06/05/12	Updated document to match with current Cypress template. Changed title from “Converting” to “Migrating”. Reworded the Abstract for better understanding. Text updates for more clarity. No change in technical content.
*D	3918276	PSR	03/01/2013	Updated Table 5 under Parameters (Changed unit of t_{DOE} parameter from mA to ns).
*E	4168635	GVCH	10/21/2013	Obsolete document.
*F	4221998	GVCH	12/19/2013	Document reactivated. Updated in new template.

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