AN55661

Migrating from CY14B256L/STK14D88 to CY14B256LA

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Associated Part Family: CY14B256L/STK14D88, CY14B256LA
Related Application Notes: None

AN55661 provides details for migrating from the CY14B256L/STK14D88 nvSRAM parts to CY14B256LA part in applications. This application note also lists the parameter differences between the parts and the design considerations for migration when converting applications to CY14B256LA.

Introduction

Cypress CY14B256LA is a 3 V, 256 Kbit (32 K x 8), nvSRAM in 0.13 micron technology. This part with a few performance enhancements is functionally equivalent to CY14B256L/STK14D88 in 0.25 micron technology but with a few differences in parameters. This application note highlights the differences between the CY14B256L/STK14D88 and the CY14B256LA and the parameters that must be considered while migrating.

Note: STK14D88 is the Simtek part number for CY14B256L.

Overview

The following tables compare the features and parameters of the two parts. As shown in Table 1, the 256 Kbit nvSRAM is available in x8 configuration.

Table 1. Part Number Description

Description	Original Part Number	Replacement Part Number
32 K x 8	CY14B256L/STK14D88	CY14B256LA

Feature Set

Both the parts share the same overall feature set and are available in the operation speed bins as given in Table **2**.

Table 2. Feature Set Comparison

Feature Set	CY14B256L/ STK14D88	CY14B256LA
AutoStore	Available	Available
Software STORE	Available	Available
Hardware STORE	Available	Available
AutoStore Enable/ Disable	Available	Available
Software RECALL	Available	Available
Speed	25 ns 35 ns 45 ns	25 ns - 45 ns
STORE Cycles	200,000	1,000,000
Data Retention	20 years at 55 °C	20 years at 85 °C

Operating Temperature Range

While CY14B256L/STK14D88 is available in both commercial and industrial temperature ranges, CY14B256LA is offered only in the industrial temperature range.

Table 3. Operating Temperature Range Comparison

Operating Temperature Range	CY14B256L/ STK14D88	CY14B256LA
Commercial (0 to 70 °C)	Available	Not Available
Industrial (–40 to 85 °C)	Available	Available

Packages

CY14B256LA is pin compatible with CY14B256L/ STK14D88 and is available in the same packages and pin configurations, and in additional packages.

Table 4. Packages Comparison

Package	CY14B256L/ STK14D88	CY14B256LA
32-pin SOIC	Available	Available
48-pin SSOP	Available	Available
44-pin TSOPII	Not Available	Available

Parameters

The CY14B256LA is a pin compatible replacement for CY14B256L/STK14D88 and requires minimum changes in the application board in most applications. However, the differences in parameters should be considered before replacing one part with the other. Table 5 lists the differences in parameters between CY14B256L/STK14D88 and CY14B256LA.

Table 5. Parameter Comparison

Parameter	Description	Speed	CY14B256L/ STK14D88		CY14B256LA		Unit
			Min	Max	Min	Max	
DC Parameters							
I_{CC1}	Average V_{CC} Current	25 ns	-	70	-	70	mA
		35 ns	-	60	-	-	
		45 ns	-	55	-	52	
I_{CC2}	Average V_{CC} Current during STORE	-	-	3	-	10	mA
I_{CC3}	Average V_{CC} Current at t_{RC} = 200 ns, 3 V, 25 °C	-	10 (typ)		35 (typ)		
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle	-	-	3	-	5	mA
I_{SB}	V_{CC} Standby Current	-	-	3	-	5	mA
V_{CAP}	Storage Capacitor	-	17 to 120		61 to 180		µF
AC Switching Parameters							
Read and Write cycle parameters are identical							
AutoStore / Power-Up RECALL Parameters							
t_{STORE}	STORE Cycle Duration	-	-	12.5	-	8	ms
t_{DELAY}	Time Allowed to Complete SRAM Write Cycle	-	1,000	70,000	-	25	ns
V_{HDIS}	$\overline{HSB}$ Output Disable Voltage	-	Not specified		-	1.9	V
t_{LZHSB}	$\overline{HSB}$ To Output Active Time	-	Not specified		-	5	µs
t_{HHHD}	$\overline{HSB}$ High Active Time	-	Not specified		-	500	ns
Software Controlled STORE/RECALL Cycle Parameters							
t_{HA}	Address Hold Time	-	1	-	0	-	ns
t_{RECALL}	RECALL Duration	-	-	120	-	200	µs
t_{SS}	Soft Sequence Processing Time	-	-	70	-	100	µs
Hardware STORE Cycle Parameters							
	$\overline{HSB}$ LOW to STORE Busy	-	Not specified		-	25 (t_{DELAY})	ns
t_{DHSB}	$\overline{HSB}$ To Output Active Time when write latch not set	-	Not specified		-	25	ns

Critical Considerations

The impact of the differences in CY14B256LA with respect to the CY14B256L/STK14D88 in existing applications are discussed in this section. System designers are recommended to review the detailed datasheets when migrating to the new part.

DC Parameters

I_{CC1} (Average current at full speed) is the same in CY14B256LA and hence power supply design in applications with CY14B256L/STK14D88 would require no changes when replacing the nvSRAM with the CY14B256LA in spite of the higher values in the lower speed / higher standby current. The critical parameter to consider is the V_{CAP}.

V_{CAP}

V_{CAP} is the capacitor that provides the required charge for AutoStore to complete NV store of the SRAM data during power down. The required capacitor range is different for the two parts.

Table 6. V_{CAP} Comparison

Description	CY14B256L/ STK14D88	CY14B256LA
V_{CAP}	17 µF to 120 µF	61 µF to 180 µF
Voltage Rating	6 V	4 V

Therefore, in any existing application which uses a capacitor value outside the overlapping range (61 µF to 120 µF) the impact of capacitor dimensions needs to be considered while changing to the new capacitor. The capacitor voltage rating requirement is lower in CY14B256LA as the V_{CAP} voltage is not boosted above the V_{CC} voltage as done in the CY14B256L/STK14D88.

Note The capacitor range is the absolute value of the capacitor, net of tolerence.

AC Switching Parameters

The AC parameters are identical between the CY14B256LA and the CY14B256L/STK14D88 for identical speed grades. For replacing 35 ns speed parts, choose the 25 ns speed parts as replacement (since 35 ns speed grade is not available in the CY14B256LA).

AutoStore / Power-Up RECALL Parameters

The AutoStore/Power-Up RECALL parameters are better in the CY14B256LA compared to the CY14B256L/STK14D88 and hence applications would not require any changes during migration. The improvements are listed under the Details of Improvement section.

Software Controlled STORE/RECALL Cycle Parameters

The Software RECALL time (t_{RECALL}) and Soft sequence processing time (t_{SS}) are higher in CY14B256LA as described in Table 7.

Table 7. Software Controlled STORE/RECALL Cycle Parameters Comparison

Description	CY14B256L/ STK14D88	CY14B256LA
t_{RECALL}	120 µs	200 µs
t_{SS}	70 µs	100 µs

This difference could require firmware change in the existing application to increase the controller wait state when software RECALL or AutoStore Enable/Disable cycles are initiated.

Note: In the CY14B256L/STK14D88, reads/writes are only inhibited after t_{SS} and only for the STORE or RECALL command. In the CY14B256LA, reads/writes are inhibited after t_{DELAY} and remain disabled until the end of the soft command (t_{SS} or t_{RECALL} or t_{STORE}). This is an improvement but applications where reads/writes are performed within the t_{SS} time after initiating a software sequence would require firmware change to include the wait time.

Software Sequence

The CY14B256LA has been designed to be compatible with the CY14B256L/STK14D88 in the software sequence modes for STORE and RECALL. Hence, the same Software STORE and RECALL address sequences in CY14B256L/STK14D88 works in CY14B256LA, requiring no firmware change. Only in AutoStore Disable and Enable software sequences, the 6th address in CY14B256LA is different and needs to be changed as shown in Table 8.

Table 8. AutoStore Disable/Enable 6th Address Comparison

6th Address	Addresses $A_{15} – A_0$	
	CY14B256L/ STK14D88	CY14B256LA
AutoStore Disable	0x03F8	0x0B45
AutoStore Enable	0x07F0	0x0B46

Hardware STORE Cycle Parameters

The Hardware STORE parameters are improved in the CY14B256LA and hence applications would not require any changes during migration. The improvements are listed under the Details of Improvement section. No changes are required in applications.

STORE Cycles

The NV STORE cycles endurance in the CY14B256LA is improved five times compared to the older technology giving it one million STORE cycles against 200 K STORE cycles in the older part.

Data Retention

The Data Retention in CY14B256LA part is improved from the older technology part. The CY14B256LA has data retention of 20 years at 85 °C against the CY14B256L/ STK14D88 data retention of 20 years at 55 °C. This would translate to over 20 times improvement in data retention at the same temperatures.

Details of Improvement

Hardware STORE Related Improvements

$\overline{\text{HSB}}$ pin *(Hardware STORE Busy Indication/Hardware STORE Initiation)*

The $\overline{\text{HSB}}$ pin of the nvSRAM is an open drain I/O pin used to indicate or initiate a STORE operation. When a STORE operation is in progress, nvSRAM pulls the $\overline{\text{HSB}}$ pin low to indicate that the device is busy and cannot be accessed for read/write operation. During normal operation, the $\overline{\text{HSB}}$ pin can be pulled low to initiate a Hardware STORE operation.

As shown in Table 5, several timing parameters related to the $\overline{\text{HSB}}$ pin input and output have changed from CY14B256L/STK14D88 to CY14B256LA. All of these changes are improvements from the original part specification and should be considered as added benefits in your system while migrating to the new part number.

t_{DELAY}

If a write latch is set and the $\overline{\text{HSB}}$ pin is pulled low, CY14B256L/STK14D88 enables 1 µs to 70 µs time for write operations to complete before STORE operation begins and reads and writes are inhibited. This potentially enables inadvertent data to be written to the nvSRAM during the t_{DELAY} duration.

Note Write Latch: When a write operation is done, a 'write latch' is set internally. When $\overline{\text{HSB}}$ is pulled low, nvSRAM checks this write latch before initiating a STORE. This is done to prevent any unnecessary loss of endurance cycles.

In CY14B256LA, the t_{DELAY} parameter enables only one write cycle time for any ongoing write to complete after $\overline{\text{HSB}}$ pin is pulled low. This improvement provides better security from inadvertent write operations.

Also, if $\overline{\text{HSB}}$ pin is pulled low externally for a minimum of t_{PHSB} time on CY14B256LA, the output driver of $\overline{\text{HSB}}$ pin pulls the pin low only indicating a STORE operation within 25 ns (t_{DELAY}). This parameter for $\overline{\text{HSB}}$ low to STORE busy is not specified in the CY14B256L/STK14D88. (See Figure 1 and Figure 2)

$\overline{\text{HSB}}$ LOW When Write Latch Not Set

If no writes are performed since the last STORE/RECALL operation, STORE operation does not start when $\overline{\text{HSB}}$ is pulled low. However, the $\overline{\text{HSB}}$ pin is still internally pulled low for 1 µs to 70 µs (t_{DELAY}) time in the CY14B256L/ STK14D88 device.

CY14B256LA device does not pull the $\overline{\text{HSB}}$ pin low internally if write latch is not set. This improvement prevents the possibility of being in an infinite loop when $\overline{\text{HSB}}$ pins of two nvSRAM devices are ganged.

Figure 1. CY14B256L/STK14D88: AC Parameters Related to $\overline{HSB}$

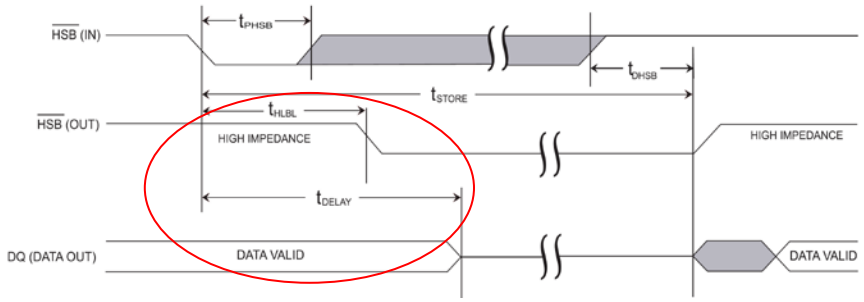
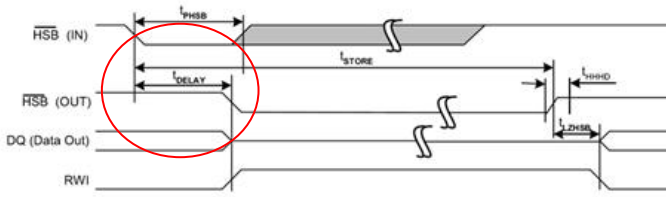
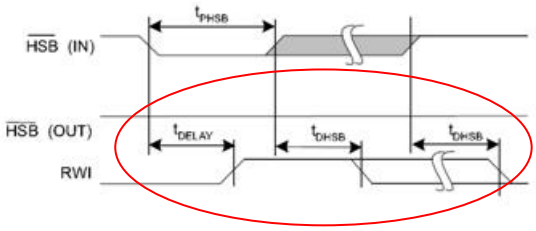


Figure 2. CY14B256LA: AC Parameters Related to $\overline{HSB}$

Write Latch Set



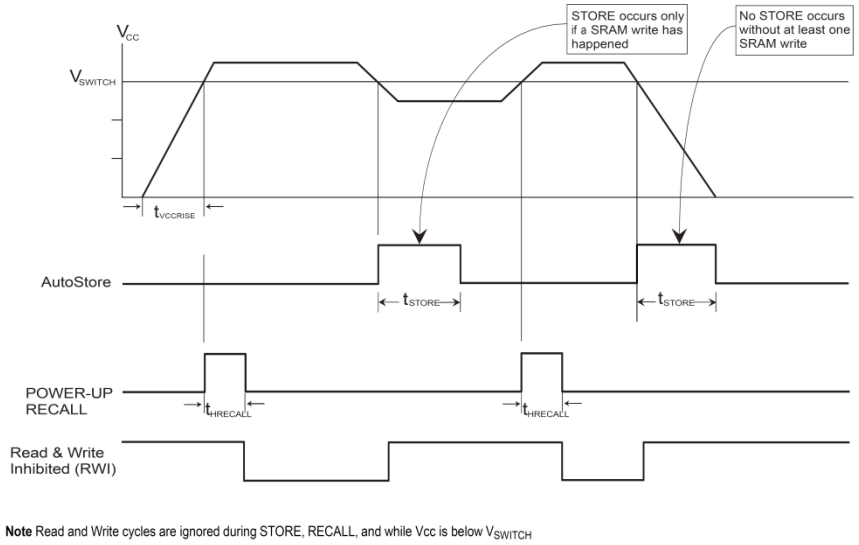
Write Latch Not Set



Power-Up Recall Related Improvements

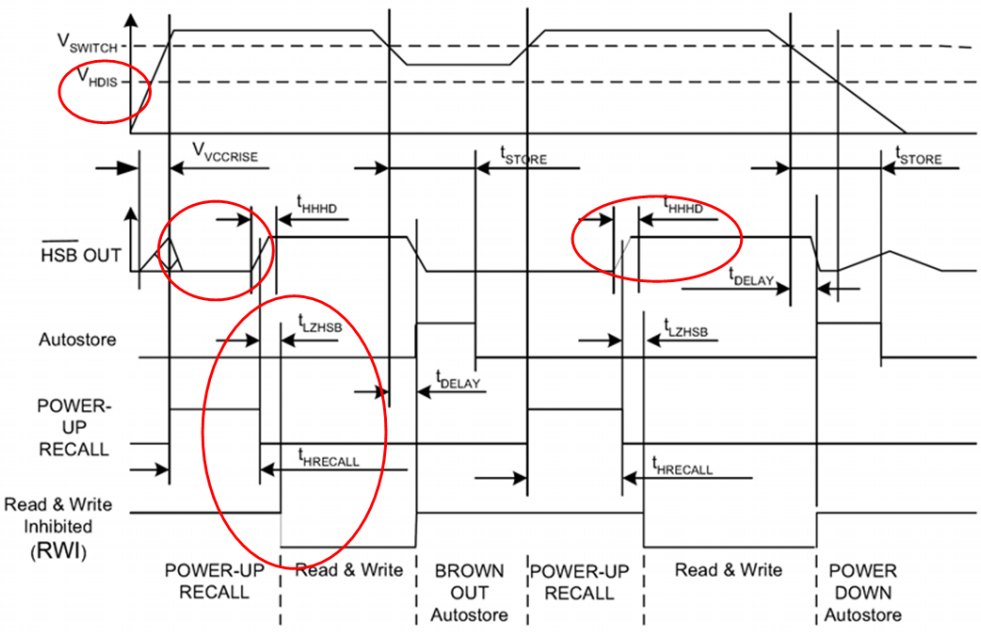
Additional parameters are specified in CY14B256LA such as $\overline{HSB}$ Output Disable Voltage (V_{HDIS}), $\overline{HSB}$ To Output Active Time (t_{LZHSB}) and $\overline{HSB}$ High Active Time (t_{HHHD}) which helps in system design. See Figure 3 and Figure 4 for the definition of the additional specs in power-up. Also, note that $\overline{HSB}$ remains low until the end of the power-up in the new part. This would guard against the system inadvertently thinking the part has completed the boot up prior to real completion.

Figure 3. CY14B256L/STK14D88: Power-Up Recall



Note Read and Write cycles are ignored during STORE, RECALL, and while Vcc is below V_{SWITCH}

Figure 4. CY14B256LA: Power-Up Recall



Summary

The application note discusses the differences between CY14B256LA in the latest 0.13 micron technology and CY14B256L/STK14D88 in the 0.25 micron technology. Several parameters related to $\overline{HSB}$ and power-up have improved / specified in the new device enabling faster device response, greater data security, and ease of design.

CY14B256LA is pin compatible with and can replace the CY14B256L/STK14D88 device with minimum changes to the hardware/firmware in most applications. Value of V_{CAP} in the existing design, the 6^{th} address for software sequence for AutoStore Enable/Disable and the controller wait state during software RECALL and AutoStore Enable/Disable cycles need to be considered while migrating.

Document History

Document Title: Migrating from CY14B256L/STK14D88 to CY14B256LA - AN55661

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2773089	PSR	10/01/2009	New Spec.
*A	3016464	PSR	09/01/2010	Changed STORE cycles of CY14B256LA in Table 2 to 1,000,000 and added a paragraph under Critical Consideration indicating the improvement.
*B	3618997	PSR	06/06/2012	Updated document to match with current Cypress template. Changed title from “Converting” to “Migrating”. Reworded the Abstract for better understanding. Text and drawing updates for more clarity. No change in technical content.
*C	4168519	GVCH	10/21/2013	Obsolete document.
*D	4221941	GVCH	12/16/2013	Document reactivated. Updated in new template.

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