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Spec No: 001-55660

Spec Title: CONVERTING FROM CY14B256K/STK17T88 TO CY14B256KA - AN55660

Sunset Owner: Ravi Prakash (PSR)

Replaced by: None

Converting from CY14B256K/STK17T88 to CY14B256KA

AN55660

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Associated Part Family: CY14B256K/STK17T88
CY14B256KA

Associated Application Notes: None

Application Note Abstract

This application note provides information on converting from CY14B256K/STK17T88 parts to the CY14B256KA part. It lists the parameter differences between the parts and the design considerations when converting existing applications from CY14B256K/STK17T88 to CY14B256KA.

Introduction

Cypress CY14B256KA is a 3 V, 32 Kb x 8, 256 Kbit nvSRAM with RTC in 0.13 u technology. This part is functionally equivalent to CY14B256K/STK17T88 (0.25 u) and is intended as a drop in replacement. (STK17T88 is the Simtek part number for CY14B256K.) This application note highlights the differences between the CY14B256K/STK17T88 and the CY14B256KA and the parameters of significance that must be considered while migrating.

Overview

The following tables compare the features and parameters of the two parts. As shown in Table 1, the 256 Kbit nvSRAM is available in x8 configuration.

Table 1. Part Number Description

Description	Original Part Number	Replacement Part Number
32 Kb x 8	CY14B256K/STK17T88	CY14B256KA

Feature Set

Both parts share the same overall feature set and are available in the following operation speed bins.

Table 2. Feature Set Comparison

Feature Set	CY14B256K/ STK17T88	CY14B256KA
AutoStore	Available	Available
Software STORE	Available	Available
Hardware STORE	Available	Available
AutoStore Enable/Disable	Not Available	Available
Software RECALL	Available	Available
RTC	Available	Available
Calibration	Available	Available
Watchdog Timer	Available	Available
Alarm	Available	Available
Capacitor or Battery backup for RTC	Available	Available
RTC Backup time with 1 F	30 days	30 days
Speed	25 ns 35 ns 45 ns	25 ns - 45 ns
STORE Cycles	200,000	1,000,000
Data Retention	20 years at 55 °C	20 years at 85 °C

Operating Temperature Range

While CY14B256K/STK17T88 is available in both commercial and industrial temperature ranges, CY14B256KA is offered only in the industrial temperature range.

Table 3. Operating Temperature Range Comparison

Operating Temperature Range	CY14B256K/ STK17T88	CY14B256KA
Commercial (0 to 70 °C)	Available	Not Available
Industrial (–40 to 85 °C)	Available	Available

Packages

CY14B256KA is pin compatible with CY14B256K/STK17T88 and is available in the same package and pin configuration.

Table 4. Package Comparison

Package	CY14B256K/ STK17T88	CY14B256KA
48-pin SSOP	Available	Available

Parameters

The CY14B256KA is a drop in replacement for CY14B256K/STK17T88 and requires minimum changes in the application board. However, the differences in parameters should be considered before replacing one part with the other. Table 5 lists the differences in parameters between CY14B256K/STK17T88 and CY14B256KA.

Table 5. Parameter Comparison

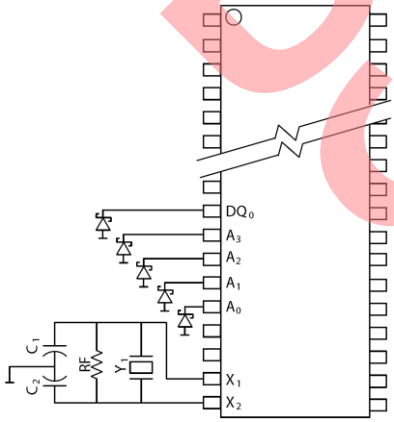
Parameter	Description	Speed	CY14B256K/ STK17T88		CY14B256KA		Unit
			Min	Max	Min	Max	
DC Parameters							
I_{CC1}	Average V_{CC} Current	25 ns	-	70	-	70	mA
		35 ns	-	60	-	-	
		45 ns	-	55	-	52	
I_{CC2}	Average V_{CC} Current during STORE	-	-	3	-	10	mA
I_{CC3}	Average V_{CC} Current at t_{RC} = 200 ns, 3 V, 25 °C	-	10 (typ)		35 (typ)		
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle	-	-	3	-	5	mA
I_{SB}	V_{CC} Standby Current	-	-	3	-	5	mA
V_{CAP}	Storage Capacitor	-	17 to 120 (CY14B256K) 17 to 57 (STK17T88)		61 to 180		uF
AC Switching Parameters							
Read and Write cycle parameters are identical							
AutoStore/Power-Up RECALL Parameters							
$t_{HRECALL}$	Power-Up RECALL Duration	-	-	40	-	20	ms
t_{STORE}	STORE Cycle Duration	-	-	15	-	8	ms
t_{DELAY}	Time Allowed to Complete SRAM Write Cycle	-	1,000	70,000	-	25	ns
V_{HDIS}	$\overline{HSB}$ Output Disable Voltage	-	Not specified		-	1.9	V
t_{LZHSB}	$\overline{HSB}$ To Output Active Time	-	Not specified		-	5	us
t_{HHHD}	$\overline{HSB}$ High Active Time	-	Not specified		-	500	ns
Software Controlled STORE/RECALL Cycle Parameters							
t_{HA}	Address Hold Time	-	1	-	0	-	ns
t_{RECALL}	RECALL Duration	-	-	170	-	200	us
t_{SS}	Soft Sequence Processing Time	-	-	70	-	100	us
Hardware STORE Cycle Parameters							
	$\overline{HSB}$ LOW to STORE Busy	-	Not specified		-	25 (t_{DELAY})	ns
t_{DHSB}	$\overline{HSB}$ To Output Active Time when write latch not set	-	Not specified		-	25	ns

Parameter	Description	T_A	CY14B256K/ STK17T88		CY14B256KA		Unit
			Min	Max	Min	Max	
RTC							
I_{BAK}	RTC Backup Current	–40°C	-	350	-	350	nA
		+85°C			-	500	
V_{RTCcap}	RTC Capacitor Pin Voltage	–40°C	1.2	2.7	1.6	3.6	V
		+85°C			1.4	3.6	
t_{OCS}	RTC Oscillator Time to Start	-	-	10	-	2 (Note)	sec
R_{BKCHG}	RTC Backup Capacitor Charge Current-Limiting Resistor	-	Not specified		350	850	Ω

Note: If V_{RTCcap} > 0.5 V or if no capacitor is connected to V_{RTCcap} pin, the oscillator starts in t_{OCS} time. If a backup capacitor is connected and V_{RTCcap} < 0.5 V, the capacitor must be allowed to charge to 0.5 V for oscillator to start.

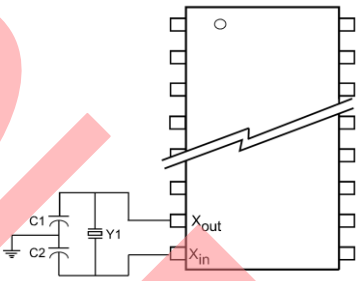
Figure 1. RTC Recommended Component Configuration

CY14B256K/STK17T88



Recommended Values
Y1 = 32.768 kHz
RF = 10M Ohm
C1 = 0 (install cap footprint, but leave unloaded)
C2 = 56 pF + 10% (do not vary from this value)

CY14B256KA



Recommended Values
Y1 = 32.768 kHz (12.5 pF)
C1 = 10 pF
C2 = 67 pF
Note: The recommended values for C1 and C2 include board trace capacitance

Table 6. RTC Register Factory Setting Comparison

Register	CY14B256K/ STK17T88								CY14B256KA								Function/Range
	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	
0x7FF6	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	Interrupts
	0x00								0x08								

Critical Considerations

The impact of the differences in CY14B256KA with respect to the CY14B256K/STK17T88 in existing applications are discussed in the following sections. Board designers are recommended to review the detailed data sheets when converting to the new part.

DC Parameters

I_{CC1} (average current at full speed) is the same in CY14B256KA and hence power supply design in applications with CY14B256K/STK17T88 requires no changes when replacing the nvSRAM with the CY14B256KA in spite of the higher values in lower speed/higher standby current. The critical parameter to consider is the V_{CAP}.

V_{CAP}

V_{CAP} is the capacitor which provides the required charge for AutoStore to complete NV store of the SRAM data during power down. The required capacitor range is different in the two parts.

Table 7. VCAP Comparison

Description	CY14B256K/ STK17T88	CY14B256KA	Unit
V_{CAP}	CY14B256K: 17 to 120 STK17T88: 17 to 57	61 to 180	uF
Voltage Rating	6	4	V

Therefore, any existing application must consider the impact of capacitor values/dimensions while changing to the new capacitor. The capacitor voltage rating requirement is lower in the newer part because the V_{CAP} voltage is not boosted above the V_{CC} voltage as done in the older part.

Note The capacitor range is the absolute value of the capacitor, net of tolerance.

AC Switching Parameters

The AC parameters are identical between the CY14B256KA and the CY14B256K/STK17T88 for identical speed grades. For replacing 35 ns speed parts, choose the 25 ns speed parts as replacement (because the 35 ns speed grade is not available in CY14B256KA).

AutoStore/Power-Up RECALL Parameters

The AutoStore/Power-Up RECALL parameters are better in the CY14B256KA compared to the CY14B256K/STK17T88 and hence can directly replace the older part. The improvements are listed in the section Details of Improvement on page 6.

Software Controlled STORE/RECALL Cycle Parameters

The Software RECALL time (t_{RECALL}) and Soft sequence processing time (t_{SS}) are higher in CY14B256KA, as described in **Error! Reference source not found.**.

Table 8. Software Controlled STORE/RECALL Cycle Parameters Comparison

Description	CY14B256K/ STK17T88	CY14B256KA
t_{RECALL}	170 us	200 us
t_{SS}	70 us	100 us

This difference may require firmware change in the application to increase the wait state when software RECALL or AutoStore Enable/Disable cycles are initiated.

Software Sequence

The CY14B256KA has been designed to be compatible with the CY14B256K/STK17T88 in the software sequence modes. Hence the same Software STORE and RECALL address sequences in the CY14B256K/STK17T88 works in CY14B256KA, requiring no firmware change.

Note The AutoStore Disable feature is not available in the CY14B256K/STK17T88. When replacing CY14B256K/ STK17T88 with CY14B256KA, leave the AutoStore in Enabled state, which is the factory default. If AutoStore is Disabled, RTC time keeping can be lost during power cycle. Refer to the data sheet for details.

Hardware STORE Cycle Parameters

The Hardware STORE parameters are much improved in the CY14B256KA. The improvements are listed in the section Details of Improvement on page 6. No changes are required in applications.

RTC

RTC oscillator has been improved in CY14B256KA to ensure that the oscillator stability is immune to the ground currents in the substrate caused by signal undershoots. Hence, as shown in Figure 1 on page 4, the Schottky diodes recommended in CY14B256K/STK17T88 are not required in CY14B256KA applications (refer to the application note AN49947, Undershoot Effect in RTC Circuit of 0.25µ nvSRAM). The values of C1, C2 are different and RF is not required in CY14B256KA. The RTC oscillator provides excellent stability with the standard best practices usually required for RTC oscillators.

Register Factory Setting

The RTC register factory setting for the Interrupt register at address location 0x7FF6 is different in CY14B256KA as described in Table 6 on page 3. The factory default in CY14B256K/STK17T88 is 0x00 while in CY14B256KA it is 0x08. This means, in the case of CY14B256K/STK17T88, at power-up, the INT pin is open drain, active LOW while in CY14B256KA the INT pin is 0, active High. This is only an initial setting and user can change this to open drain (active LOW) by writing 0x00 into the RTC address 0x7FF6 and performing a software STORE to save the setting through

power cycles. Please note that writing into the RTC registers require the W bit to be set to 1 first.

STORE Cycles

The NV STORE cycles endurance in the 0.13 u is improved five times compared to the older technology giving it one Million STORE cycles against 200 K STORE cycles in the older part.

Data Data Retention

The data retention in 0.13 u part is vastly improved from the older technology part. The CY14B256KA has a data retention of 20 years at 85 °C against the CY14B256K/STK17T88 data retention of 20 years at 55 °C. This translates to over 20 times improvement in data retention at the same temperatures.

Details of ImprovementHardware STORE Related Improvements

$\overline{HSB}$* pin *(Hardware STORE Busy Indication/Hardware STORE Initiation)

The $\overline{HSB}$ pin of the nvSRAM is an open drain I/O pin used to indicate or initiate a STORE operation. When a STORE operation is in progress, nvSRAM pulls the $\overline{HSB}$ pin low to indicate that the device is busy and cannot be accessed for read/write operation. During normal operation, the $\overline{HSB}$ pin can be pulled low to initiate a Hardware STORE operation.

As shown in Table 5 on page 3, several timing parameters related to the $\overline{HSB}$ pin input and output have changed from CY14B256K/STK17T88 to CY14B256KA. All of these changes are improvements from the original part specification and must be considered as added benefits in your system while converting to the new part number.

Write Latch: When a write operation is done, a 'write latch' is set internally. When $\overline{HSB}$ is pulled low, nvSRAM checks this write latch before initiating a STORE. This is done to prevent any unnecessary loss of endurance cycles.

t_{DELAY}

If a write latch is set and the $\overline{HSB}$ pin is pulled low, CY14B256K/STK17T88 enables 1 us to 70 us time for write operations to complete before STORE operation begins and reads and writes are inhibited. This potentially enables inadvertent data to be written to the nvSRAM during the t_{DELAY} duration.

In CY14B256KA, the t_{DELAY} parameter enables only one write cycle time for any ongoing write to complete after $\overline{HSB}$ pin is pulled low. This improvement provides better security from inadvertent write operations.

Also, if $\overline{HSB}$ pin is pulled low externally for a minimum of t_{PHSB} time on CY14B256KA, the output driver of $\overline{HSB}$ pin pulls the pin low only indicating a STORE operation within 25 ns (t_{DELAY}). This parameter for $\overline{HSB}$ low to STORE busy is not specified in the CY14B256K/STK17T88. (See Figure 2 and Figure 3)

$\overline{HSB}$ LOW when write latch not set

If no writes are performed since the last STORE/RECALL operation, STORE operation does not start when $\overline{HSB}$ is pulled low. However, the $\overline{HSB}$ pin is still internally pulled low for 1 us to 70 us (t_{DELAY}) time in the CY14B256K/STK17T88 device.

CY14B256KA device does not pull the $\overline{HSB}$ pin low internally if write latch is not set. This improvement prevents the possibility of being in an infinite loop when $\overline{HSB}$ pins of two nvSRAM devices are ganged.

Figure 2. CY14B256K/STK17T88: AC Parameters Related to $\overline{HSB}$

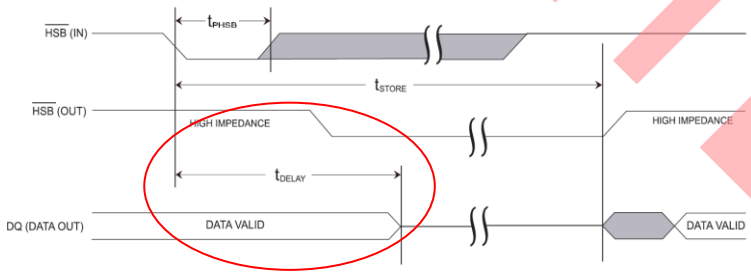
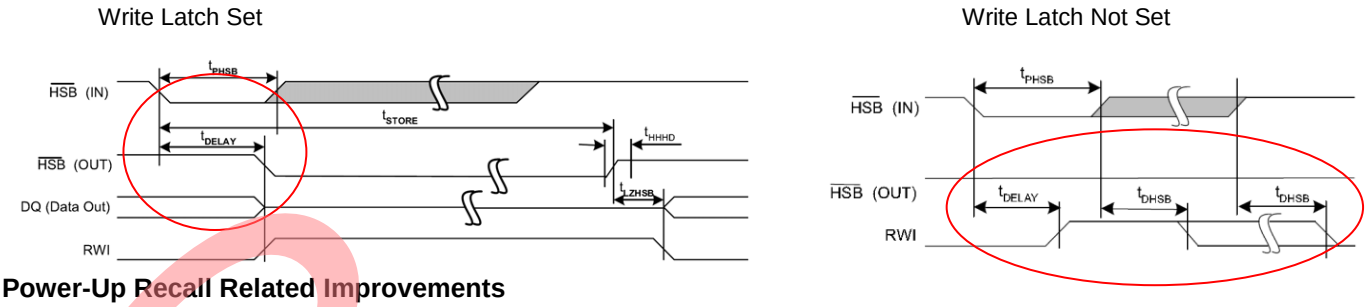


Figure 3. CY14B256KA: AC Parameters Related to $\overline{HSB}$



Power-Up Recall Related Improvements

Additional parameters are specified in CY14B256KA such as $\overline{HSB}$ Output Disable Voltage (V_{HDIS}), $\overline{HSB}$ To Output Active Time (t_{LZHSB}), and $\overline{HSB}$ High Active Time (t_{HHHD}) which helps in system design. Refer to Figure 4 and Figure 5 for the definition of additional specs in power-up. Also, note that $\overline{HSB}$ remains low until the end of the power-up in the new part. This guards against the system inadvertently thinking the part has completed the boot up prior to real completion.

Figure 4. CY14B256K/STK17T88: Power-Up Recall

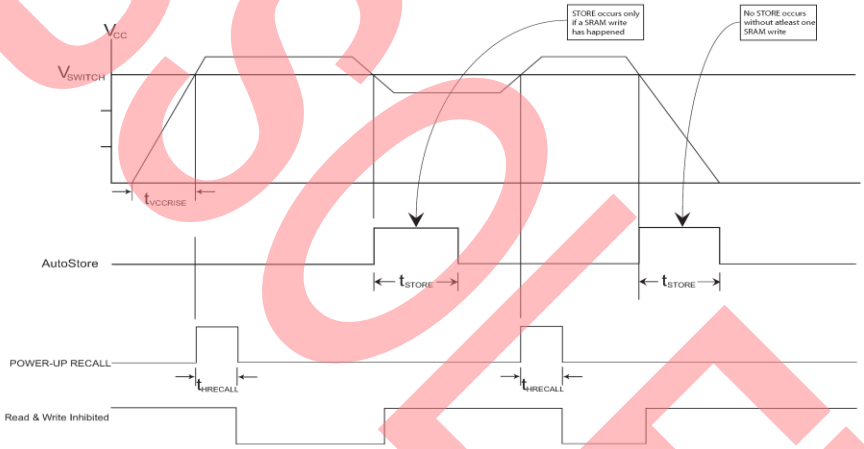
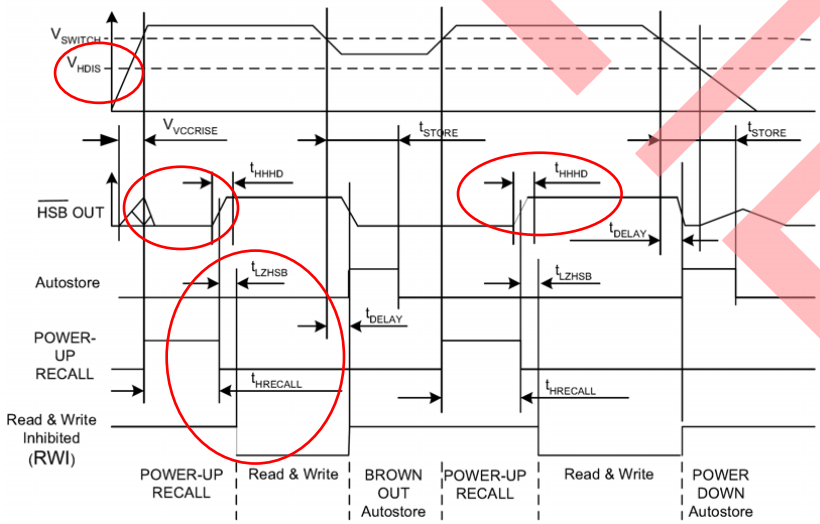


Figure 5. CY14B256KA: Power-Up Recall



RTC Improvements

The RTC oscillator circuit has been greatly improved in CY14B256KA to make the oscillator immune to signal undershoots. This is a major improvement from the CY14B256K/STK17T88 which required external Schottky diodes to keep the input signals free of undershoots which are greater than 0.5 V. The C1, C2 values are different in the CY14B256KA. The I_{BAK} current is higher in the CY14B256KA but the RTC circuit provides the same backup times with external V_{RTCcap} as in CY14B256K/STK17T88, namely, 72 hours with V_{RTCcap} = 0.1 F, 14 days with 0.47 F, and 30 days with 1 F.

The RTC Oscillator Time to start, t_{OCS} has also been improved from 10 sec in CY14B256K/STK17T88 to 2 sec in CY14B256KA. However, note that in V_{RTCcap} applications, the V_{RTCcap} pin needs to be charged to a minimum of 0.5 V for the oscillator to start up. This is considered only for the first time the circuit is powered up and hence does not affect normal applications. In applications, the V_{RTCcap} needs to be allowed to charge to 2.7 V to get the desired backup time.

Summary

The application note discusses the differences between CY14B256KA in the latest 0.13 u technology and CY14B256K/STK17T88 in the 0.25 u technology. Several parameters related to $\overline{HSB}$ and power-up have improved and been specified in the new device enabling faster device response, greater data security, and ease of design.

CY14B256KA is pin compatible and can replace the CY14B256K/STK17T88 device with minimal or no changes to the firmware. Value of V_{CAP} in the existing design must be considered while replacing the part and the values of C1, C2, and RF in the RTC circuit must be changed. Also, the factory default setting for INT pin is LOW in CY14B256KA while it is open drain in the older part. This needs to be considered and, if required, changed through writing into a RTC register.

Document History

Document Title: Converting from CY14B256K/STK17T88 to CY14B256KA – AN55660

Document Number: 001-55660

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2773089	PSR	10/01/09	New Spec.
*A	2792849	PSR	10/26/09	Corrected typo in Table 7 in t_{RECALL}
*B	3016473	PSR	08/30/10	Changed STORE cycles of CY14B256KA in Table 2 in page 1 to 1,000,000 and added a paragraph under Critical Consideration indicating the improvement. Added Table 6 for difference in RTC register factory setting Added a paragraph, RTC Register Factory Setting, under Critical Considerations
*C	3441285	GVCH	11/17/2011	Obsolete Spec

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