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Spec No: 001-54390

Spec Title: AN54390 - POWERPSOC(R) IN A 5 V INPUT SUPPLY SYSTEM

Sunset Owner: Madhan Kumar Kuppaswamy (MKKU)

Replaced by: 001-52699

PowerPSoC® in a 5 V Input Supply System

Author: Jaideep Allam and Kaushik Subramanian
Associated Project: Yes
Associated Part Family: CY8CLED0xx0x
Software Version: None
Related Application Notes: AN52699, AN52581

AN54390 describes the use of PowerPSoC® in systems using a 5 V supply. The concept is illustrated with the help of two design examples – one for color control using RGB LEDs and the other for driving a string of white LEDs. Starting with a brief theory of the boost and buck topologies used in this design, this document further discusses the implementation and circuit specifications. The various waveforms captured during testing are also attached.

Introduction

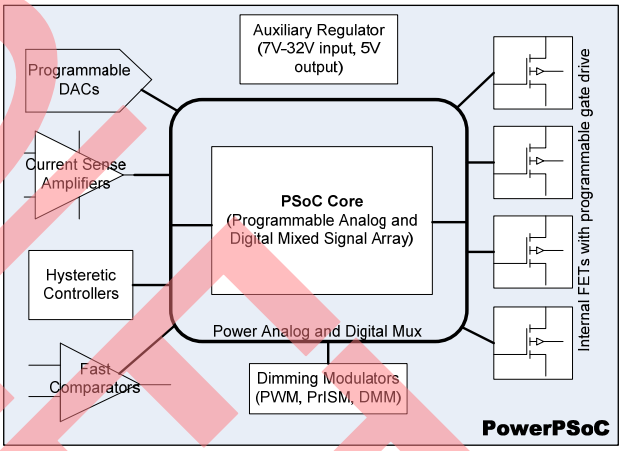
Compact devices that can deliver the same performance using a lower supply voltage are very popular now. Therefore, design engineers often face the challenge of designing these systems to work from a low voltage to meet space and power constraints. The most common method is to use switch mode power supplies which can power high voltage systems using the low voltage that is available on board. This document describes one such design using Cypress's PowerPSoC device.

The PowerPSoC family of devices has the flexibility of the classic PSoC® M8C core and the power of four built-in FETs. Each channel has its own current sense amplifier, hysteretic controller, a power FET, and a modulator. This sets up a perfect platform for designing precisely controlled high power applications up to 32 V, 1 A per channel, optimized for lighting. The programmability of the PSoC blocks makes it possible to use them in a variety of applications. The power peripherals, for example, can be configured as boost or floating load buck, or a combination of both. They meet a range of design requirements from lighting control, motor, and relay drives to power supply design and power factor correction systems.

The integrated DACs and hardware comparators provide protection to the system against overvoltage, current, or temperature. The auxiliary regulator of the PowerPSoC generates a 5 V supply to power the microcontroller core and the other onboard peripherals from the input supply to the chip. This eliminates the need for an external voltage regulator.

The following figure shows a simplified block diagram of the PowerPSoC architecture.

Figure 1. Simplified Block Diagram of PowerPSoC



System Overview

While the built-in switching regulator and current sense amplifiers in PowerPSoC are rated for operation from 7 V to 32 V, all of the other power peripherals and the PSoC Core operate from a 5 V power rail. Thus, when PowerPSoC is used to implement a constant current mode DC-DC converter in 5 V-powered systems, a two stage approach is used.

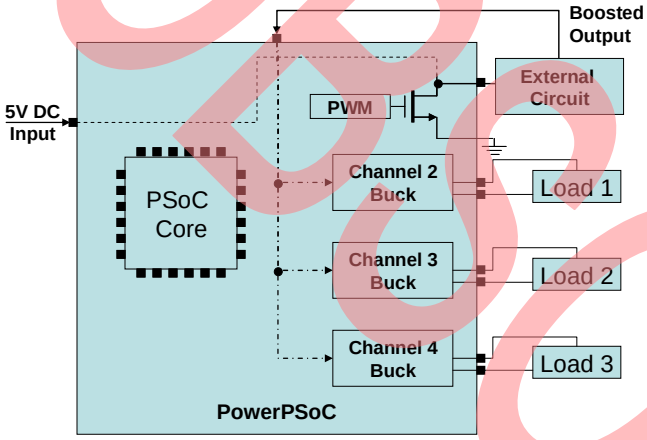
The first is a boost converter stage using PowerPSoC's modulator blocks and the internal power FET. If the input current requirement is higher than 1 A, external power MOSFETs can be used. The boosted output voltage is fed into the second stage that is configured as a floating load buck converter. This stage is used to drive the load at the desired constant current.

Based on this architecture, this application note illustrates two design examples. The first example describes a

typical RGB LED lamp that can generate any desired color within its range. The second example considers a white light driver built using strings of white LEDs. In both of these systems, PowerPSoC is used in the design of the constant current driver. It can also be used to add intelligence such as color-mixing abilities and feedback systems such as temperature and optical feedback.

The boost output voltage and the buck output current are both regulated using PowerPSoC's built-in power peripherals. The details are discussed in the section Design Implementation.

Figure 2. System Architecture for the Examples



All the power converters (boost and buck) use the PowerPSoC's internal FETs for switching. The buck and boost channels use the switching regulator within the hysteretic controllers to regulate the output current and voltage, respectively. In addition to this, the modulator blocks of PowerPSoC can be used to adjust the brightness of LEDs. This feature helps in designing a color mixing system by adjusting the intensity of RGB LEDs.

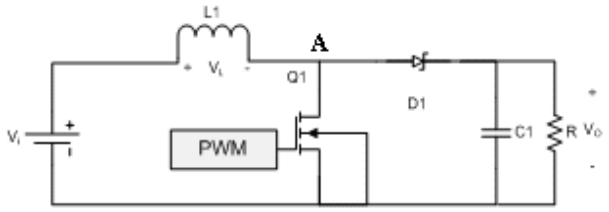
Safety features to protect against overvoltage or undervoltage, short circuit, and current surges are incorporated in the design. These are discussed in the section Design Implementation.

The following sections describe the working principles of boost and buck regulators, followed by detailed implementation of the two examples.

Boost Converter

The boost converter is a DC-DC converter, where the output voltage is higher than the input voltage. The following figure shows the basic circuit of a boost converter.

Figure 3. Basic Boost Converter



The boost circuit influences the property of the inductor to resist instant changes in current. It absorbs energy during the charging cycle and releases the stored energy in the discharge cycle.

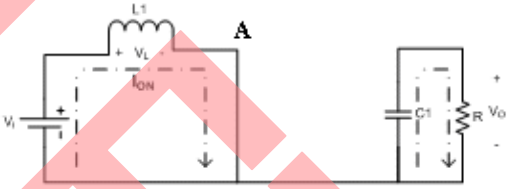
$$V_L = L\left(\frac{di}{dt}\right) \qquad \text{Equation 1}$$

As Equation 1 indicates, the voltage produced during the discharge phase is related to the rate of change of current, enabling different input and output voltages.

The functioning of the boost converter is explained in two stages:

- FET Q1 is ON

  Figure 4. Current Flow when Q1 is ON



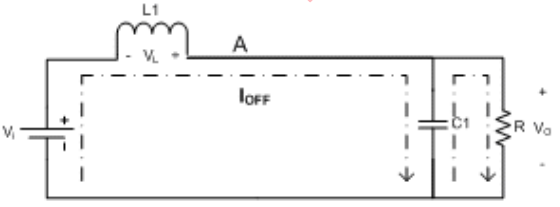
  When the transistor Q1 is ON, the inductor is charged (see Figure 4), resulting in a linear increase in the inductor current. The diode D1 prevents the capacitor from discharging into the transistor Q1.

$$V_i = L\frac{di}{t_{ON}} = L\frac{di}{DT} \qquad \text{Equation 2}$$

  where D is the duty cycle of the PWM switching pulse and T is the time period of the switching pulse.

- FET Q1 is OFF

  Figure 5. Current Flow when Q1 is OFF



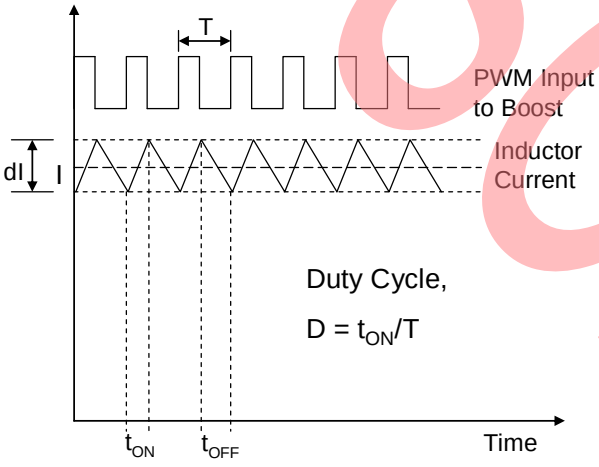
While the transistor Q1 is OFF, the inductor tries to maintain the current through it. This causes the voltage at node A to rise higher than the capacitor voltage. This triggers the diode to start conducting and enables the charge stored in the inductor to be transferred to the capacitor C1 (see Figure 5).

Neglecting the drop across the diode, write the following:

$$-(V_i - V_o) = -L\left(\frac{di}{t_{OFF}}\right)$$
$$= -L\left(\frac{di}{(1-D)T}\right) \quad \text{Equation 3}$$

The variation of current in the two stages is shown in Figure 6. This is the continuous current mode (CCM) of operation where the output current is not enabled to fall to zero.

Figure 6. Inductor Current Waveform and PWM to the FET



Assuming a steady state operation, Equations 2 and 3 result in:

$$\frac{V_o}{V_i} = \frac{1}{(1-D)} \quad \text{Equation 4}$$

where D is the duty cycle and D < 1

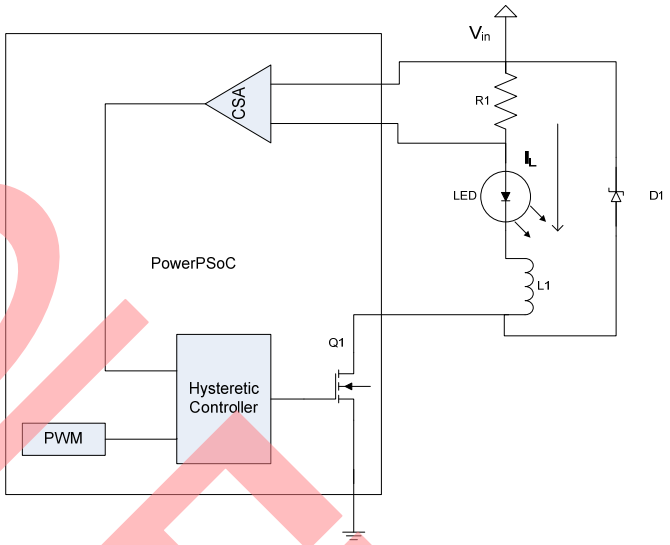
This shows that the output voltage in a boost converter is higher than the input voltage, and can be varied by changing the duty cycle, D, of the transistor switching signal.

Floating Load Buck Topology

The buck converter is also a DC-DC converter, using the same property of the inductor as the boost. This type of power converter 'bucks' or steps down the input voltage. While doing this, the buck also steps up the current. In this case too, the output voltage is changed by varying the duty cycle of the switching elements. If current feedback is provided, the circuit acts as a current mode regulator. This type of circuit is, therefore, employed in LED brightness control, where a constant current is maintained and the brightness is varied by changing the ON/OFF time of the LEDs (Pulse Width Modulation).

The floating load buck topology designed using PowerPSoC's internal hysteretic controller and current sense amplifier (CSA) is shown in the following figure.

Figure 7. Floating Load Buck Topology using PowerPSoC's Built-in Control Elements



The functioning of the floating load buck topology is explained in two stages, as in the boost:

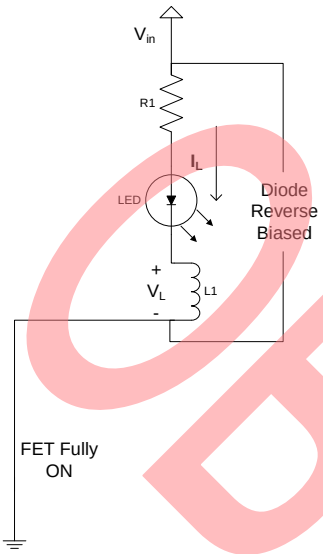
- FET Q1 is ON.

  During the ON cycle, the FET is turned on and the current through the inductor increases linearly as shown in Equation 5)

$$(V_i - V_{LED}) = L\left(\frac{di}{t_{ON}}\right) \quad \text{Equation 5}$$

The diode D1 is reverse biased in this cycle, so the only path for the current to flow is shown in the following figure.

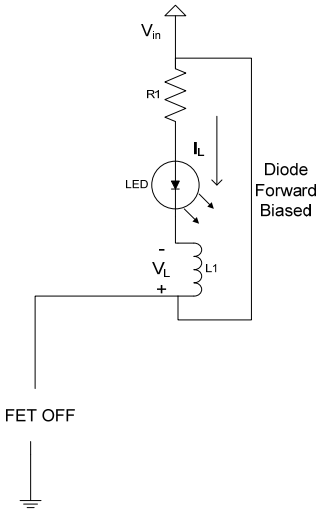
Figure 8. Current Flow when FET Q1 is ON



- FET Q1 is OFF

  When the FET is turned off, the inductor starts to discharge through the diode and the LED, as shown in Figure 9.

  Figure 9. Current Flow when FET Q1 is OFF

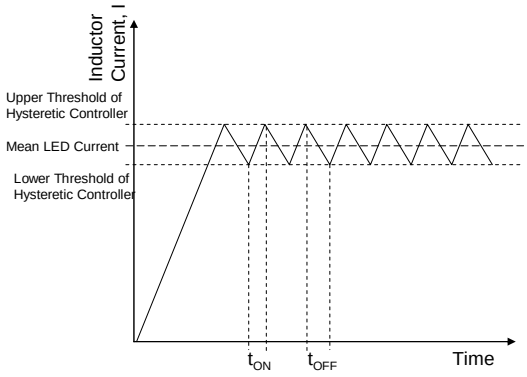


The current starts to decrease linearly as shown in the following equation:

$$-V_{LED} = -L\left(\frac{di}{t_{OFF}}\right) \qquad \text{Equation 6}$$

This results in an inductor current as shown in the following figure.

Figure 10. Inductor/Load Current Waveform



The control block determines the time for which the transistor Q1 is ON or OFF. There are a number of algorithms available for this purpose. However, PowerPSoC's integrated low side power transistor and high side current sense amplifier along with the hysteretic controller make this as easy as setting a few parameters in the firmware. This is discussed in the section Buck Output Current Regulation.

Design Implementation

This section describes the voltage and current regulation features of the boost and buck converters, followed by the safety features built into each. The circuit specifications are provided later in this section.

Boost Output Voltage Regulation

The output of the boost converter is regulated using a Voltage Mode Feedback to the hysteretic controller. The boost output is divided by a voltage divider (set to 1/10) and fed to the hysteretic controller's feedback input through the function pin FN_0_0. The feedback path consists of the comparator and the reference DACs integrated into the hysteretic controller of the PowerPSoC. This is shown in Figure 11. When the output of the boost falls below Ref Low, the hysteretic controller output goes high, enabling the PWM to switch the FET, resulting in an increase in the output voltage. When the boost output goes above Ref High, the hysteretic controller output goes low, turning off the PWM control of the FET. This causes the boost output voltage to fall. Thus, the low frequency hysteretic controller output gates the high frequency PWM switching pulse to the FET. This way, the output of the boost is regulated at the required level.

The DAC reference voltages for the two designs are as follows:

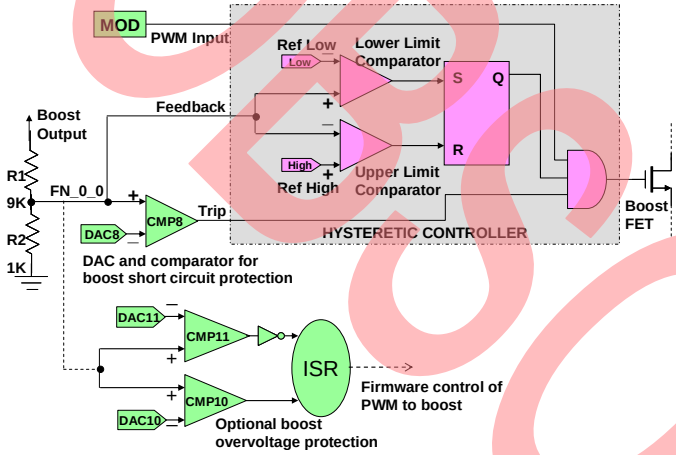
Example 1: Ref Low: 0.8 V
Ref High: 0.9 V
Example 2: Ref Low: 2.1 V
Ref High: 2.25 V

Note that the output voltages are enabled to vary from 8 V to 9 V and 21 V to 22.5 V in the two examples based on the references, resulting in an output voltage ripple of about 1 V and 1.5 V respectively.

PWM Soft Start

This feature ensures a smooth ramp up in the output voltage of the boost when the system is switched on. This is implemented by a software loop that increases the PWM duty cycle in discrete steps. This, in turn, results in a gradual increase in the output voltage of the boost.

Figure 11. Boost Voltage Regulation and Protection



Boost Short Circuit and Overvoltage Protection

The boost stage must be protected against short circuit and overvoltage. The output of the boost should never fall to less than $V_{IN} – V_F$ (the forward voltage of the diode), which is about 4.5 V in this system. If it does, there is a continuous flow of current through the inductor, which increases when the FET is turned ON. A current exceeding the rated maximum for the inductor can damage it. The short circuit protection circuit takes care of this condition.

Figure 11 shows the implementation of these two features. PowerPSoC's internal bank of hardware comparators and DACs is useful in designing this feature. DAC8 and comparator CMP8 constitute the short circuit protection mechanism. The output of the boost is fed back to the comparators through the resistive voltage divider comprising resistors R1 and R2, chosen for a 1/10 division. DAC8 is set to 0.45 V and the output of CMP8 is set to "Invert Enable." Thus, as long as the voltage at the output is higher than 4.5 V, the output of the comparator is 0 and does not trip the hysteretic controller. After the voltage goes below 4.5 V, the comparator output goes high, shutting down the hysteretic controller.

shows the implementation using hardware DAC9 and CMP9 in the PSoC Designer 5 environment. The output of the voltage divider is fed to the positive input of the comparator through FN_0_0. The reference voltage is set using the DAC. The comparator output is inverted and sent to the trip input of the hysteretic controllers. Thus, the

Note that CMP8 is the last user module to be included in the firmware so that it does not disable the boost from starting up on power on.

Overvoltage protection safeguards the circuit against the no load condition. In this design, the hysteretic controller that regulates the output voltage also protects the circuit against overvoltage by regulating the boost output voltage.

Figure 11 also shows an alternate implementation of the overvoltage protection. This can be used in designs where the hysteretic controller of the boost is used in a current mode feedback instead of voltage mode. In this method, DACs 10 and 11 are used to set reference inputs to the two comparators: CMP10 and 11 respectively. Here too, the output of the boost is fed back to the comparators through the voltage divider. This feature is interrupt driven, and is implemented by the ISR in the firmware. Comparator CMP10 triggers an interrupt when the boost output goes above DAC10 reference, and shuts off the PWM to the boost FET. Comparator CMP11 (with inverted output) triggers an interrupt when the output goes below DAC11 reference and turns on the PWM to the boost FET. The waveform in **Error! Reference source not found.** shows this mechanism in action.

Buck Output Current Regulation

As indicated in Figure 7, the buck converter uses current mode feedback to the hysteretic controller to regulate its output current. The control loop consists of the sense resistor, current sense amplifier, the hysteretic controller, and the integrated FET.

When Q1 turns ON, the current through the inductor (and the LED load) rises linearly. This current is sensed by the sense resistor R1. The voltage across the resistor is fed to the CSA, which amplifies it 20 times and feeds it to the hysteretic controller. The voltage is compared with preset upper and lower current limits set using the hysteretic controller's integrated DACs.

After this current reaches the upper current limit set in the hysteretic controller, Q1 is turned OFF. This results in a ramp down of current, until it reaches the lower current limit set in the hysteretic controller. At this point, the transistor Q1 is turned ON again. The mean current is the midpoint between the lower and upper current levels. Cypress recommends a ripple of 15 to 30 percent for most designs.

Buck Undervoltage Lockout Protection

This feature has been incorporated to prevent the buck loads from turning on until the boost output has reached the required load voltage.

loads are not switched on until the boost output reaches the value set by the reference DAC. After the output crosses this value, the comparator output goes low, turning on the hysteretic controllers of the buck converter. The reference values for the two examples are:

Example 1: DAC9 reference: 0.7 V

Example 2: DAC9 reference: 2 V

Example 1: RGB LED Control

The first example illustrates the application of PowerPSoC in an RGB LED control system. The block diagram of this design is shown in Figure 12. The boost stage boosts the 5 V to 8.4 V. This is fed into the three floating load buck channels. Each of the buck channels is connected to LED loads, which in this example, are three red, two green, and two blue LEDs. The boost output is chosen to maintain 2 V headroom over the output voltage.

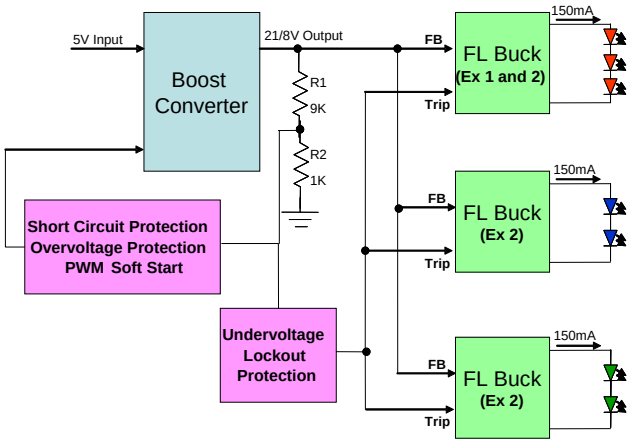
Example 2: White LED String Control

This example shows the PowerPSoC in a HB white LED lighting system. Here the boost stage steps up the voltage from 5 V to 21.3 V and feeds it to one buck channel that is connected to a string of 6 HB white LEDs, making it a 19 V load at the output.

Note that the LED voltages indicated are at the specified current of 150 mA. It should be noted that the LED load voltage changes with current and the boost voltage should be set accordingly.

The CY3267 PowerPSoC Lighting Evaluation Kit was used for conducting both these tests. Out of the four channels in this board, one of the channels' internal FET was isolated from the rest of the components and used as a part of a boost circuit which was constructed externally.

Figure 12. Block Diagram for the Two Examples



Safety Features

The safety features are discussed in the Design Implementation section. These are the safety features included in the design:

1. PWM Soft Start
2. Boost Short Circuit and Overvoltage Protection
3. Buck Undervoltage Lockout Protection

Circuit Diagrams and Specifications

The circuit diagrams with the component values for the boost and buck stages are shown in Figure 12 and Figure 13. The circuit specifications are shown in Table 1 and Table 2.

The duty cycle of the PWM is set to produce a boost voltage that is slightly higher than the upper threshold of the hysteretic controller. This is to allow the controller to regulate the output voltage between the two thresholds.

For example, the duty cycle for Example 2 is set to 78%, corresponding to an output voltage of about 23 V, which exceeds the higher threshold of the hysteretic controller (22.5 V). This ensures that the hysteretic controller functions as desired, regulating the output voltage between the two threshold levels.

Figure 13. Boost Circuit with Component Values

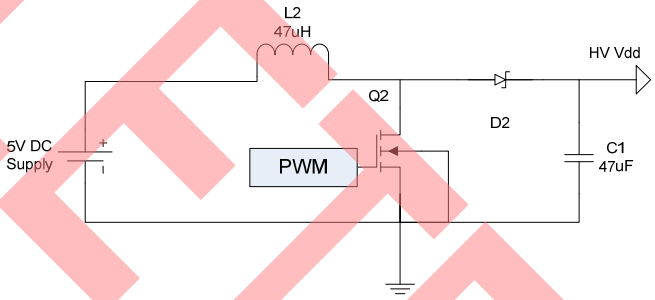


Table 1. Boost Circuit Specifications

Parameter	Ex. 1	Ex. 2
Input Voltage	5 V	5 V
Output Voltage	8.4 V	21.3 V
PWM Duty Cycle	48%	77%
Switching Frequency	200 kHz	200 kHz
Input Current	730 mA	640 mA

Figure 14. Buck Circuit with Component Values

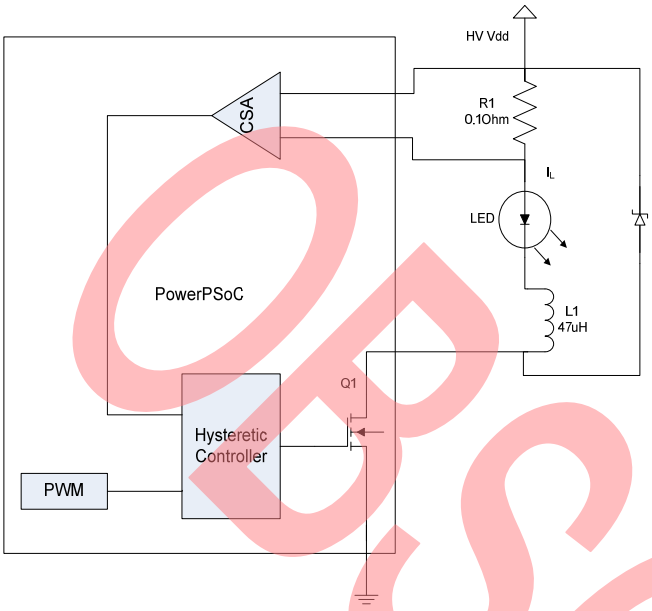


Table 2. Buck Circuit Specifications (No Dimming)

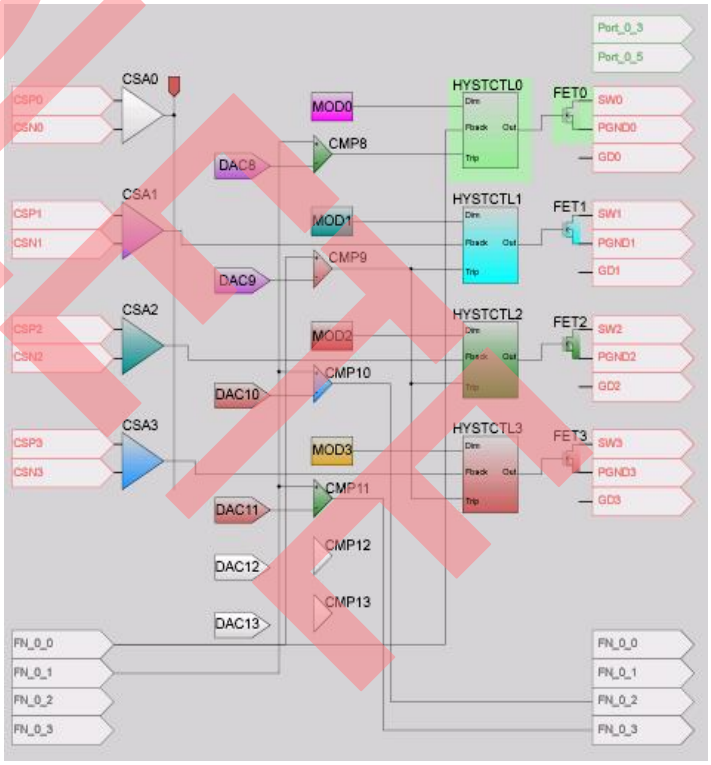
Parameters	Ex. 1			Ex. 2
Input Voltage (V)	8.4			21.3
Output Voltage (V)	6.6	6.46	6.9	19
Current Ripple	20%			20%
Output Current (mA)	155	162	145	146

Module Placement and Routing

This section describes the various blocks used in the firmware design.

- MOD0: PWM switching pulse to the boost FET.
- MOD1-3: PWM dimming input to the buck channels.
- FET0: Internal FET used for boost circuit design.
- FET1-3: Internal FETs used for buck circuits.
- HYSTCTRL0: Hysteretic controller used for boost output voltage regulation.
- HYSTCTRL1-3: Hysteretic controllers used for the buck output current regulation. These are configured to drive a constant current of 150 mA with a 20 mA ripple through the LEDs in both the examples.
- CSA0: Not Used.
- CSA1-3: current sense amplifiers used in the feedback loop of buck channels.
- DAC8 and CMP8: Digital to analog converter and comparator used for boost short circuit protection.
- DAC9 and CMP9: Digital to analog converter and comparator used for buck undervoltage lockout protection.
- CMP10-CMP11: PowerPSoC's built-in hardware comparators used for overvoltage protection. (optional)
- DAC10-DAC11: Digital to analog converters used as a reference input to the comparators 10 and 11. (optional)
- FN_0_0 and FN_0_1: Function pins connected to the voltage divider output.
- FN_0_2 and FN_0_3: Function pins connected to the output of CMP10 and 11 for interrupt detection.

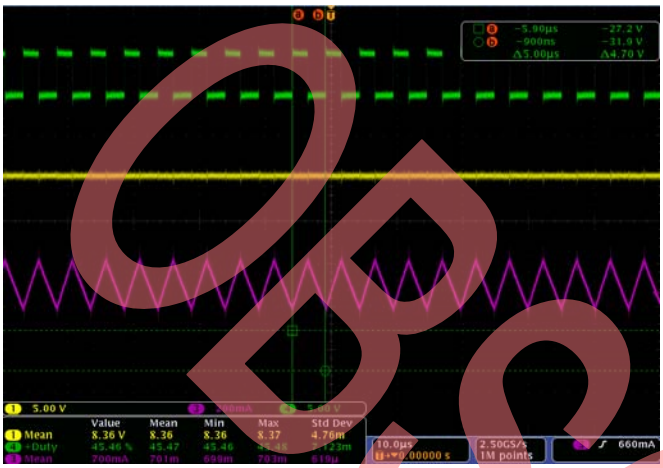
Figure 15. User Module Placement and Routing in PSoC Designer



Waveform Captures

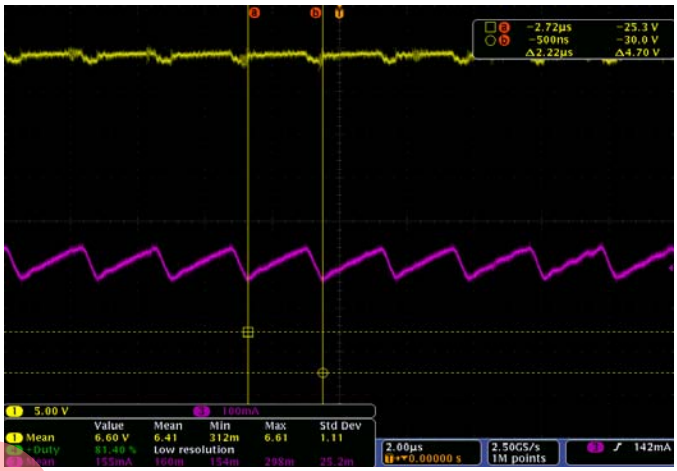
Example 1: RGB LEDs Driven from Three Buck Channels

Figure 16. Boost Characteristics



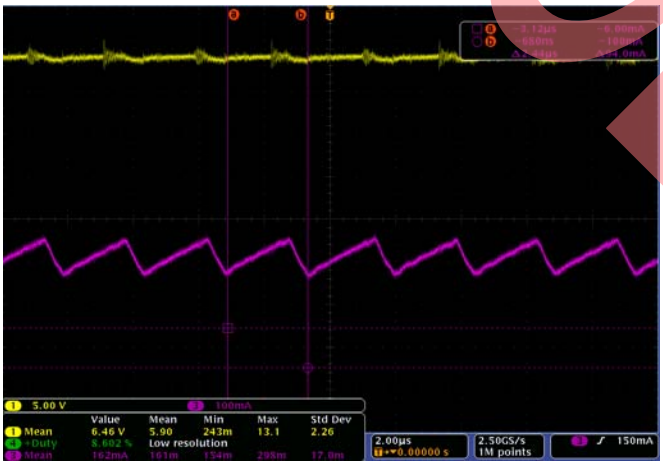
CH1: PWM to FET
CH2: Boost Output Voltage
CH3: Boost Inductor Current

Figure 17. Buck Channel 1 Characteristics



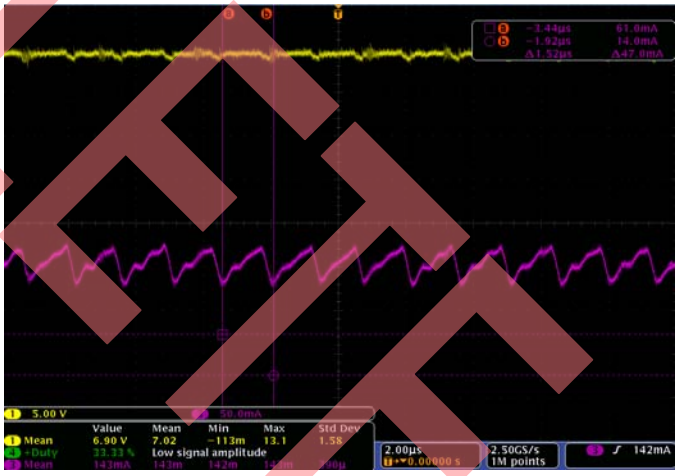
CH2: Buck 1 Output Voltage
CH3: Buck 1 Inductor/Load Current

Figure 18. Buck Channel 2 Characteristics



CH2: Buck 2 Output Voltage
CH3: Buck 2 Inductor/Load Current

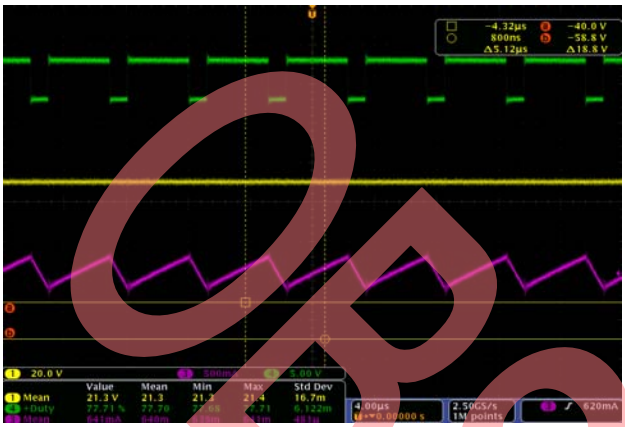
Figure 19. Buck Channel 3 Characteristics



CH2: Buck 3 Output Voltage
CH3: Buck 3 Inductor/Load Current

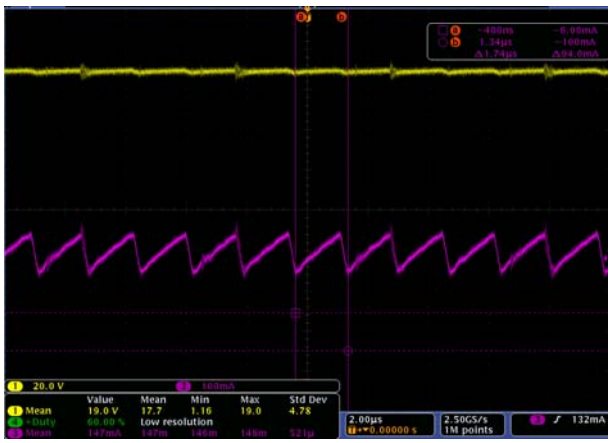
Example 2: String of Six White LEDs Driven from One Buck Channel

Figure 20. Boost Characteristics



CH1: PWM to FET
CH2: Boost Output Voltage
CH3: Boost Inductor Current

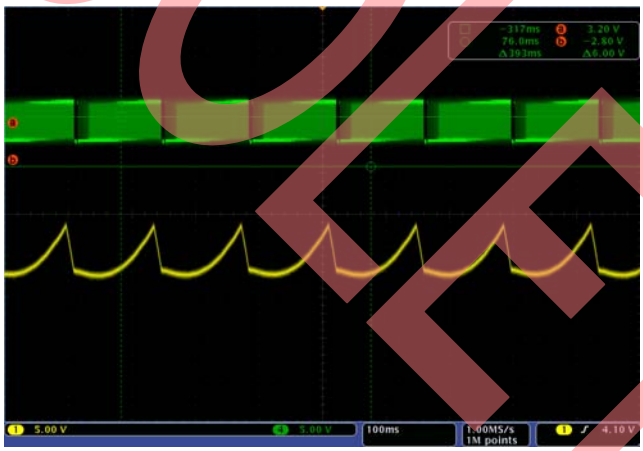
Figure 21. Buck Characteristics



CH2: Boost Output Voltage
CH3: Boost Inductor Current

Overvoltage Protection Circuit in Action

Figure 22. Boost Output Voltage when Load is not Connected



CH1: PWM to boost FET
CH2: Boost Output Voltage

Efficiency Calculations

The overall system efficiencies for the two designs are calculated using the following formulae:

Design Example 1:

V_{outx} and I_{outx} are the output voltage and current of buck x. V_{in} and I_{in} are the input voltage and current to boost (or the overall system).

$$\eta = \frac{V_{out1} \times I_{out1} + V_{out2} \times I_{out2} + V_{out3} \times I_{out3}}{V_{in} \times I_{in}}$$

Design Example 2:

V_{out} and I_{out} are the output voltage and current of the buck.

V_{in} and I_{in} are the input voltage and current of the boost (or the overall system).

$$\eta = \frac{V_{out} \times I_{out}}{V_{in} \times I_{in}}$$

Summary

With its programmability and configurable hardware features, PowerPSoC simplifies the design of precisely controlled power applications. This application note describes the use of PowerPSoC as a voltage and current regulator using built-in blocks in a 5 V input system.

Because most of the power channel control is done with the device's integrated hardware, the microcontroller core of PowerPSoC can be used to add intelligence and processing capabilities, making it versatile for high end system design.

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2732129	ALAM/QUS	07/06/2009	New application note
*A	3676111	MKKU	07/13/2012	Updated template and associated part family.
*B	3934547	MKKU	03/15/2013	Obsolete spec.

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