

Real Time Clock Calibration in Cypress nvSRAM

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Associated Part Family: nvSRAM RTC

AN53313 describes the Real Time Clock (RTC) calibration feature in Cypress nvSRAM. This feature helps to maintain precise system time by compensating for the crystal frequency error from its nominal frequency of 32.768 kHz. This application note also provides a lookup table for the calibration adjustment.

1 Introduction

The Real Time Clock (RTC) in Cypress nvSRAM is driven by a crystal oscillator, with an external crystal having a nominal frequency of 32.768 kHz. Most 32.768-kHz crystals have a frequency tolerance of ± 20 parts per million (ppm) at $+25$ °C. This frequency tolerance results in timing error over a long period of time. For example, a crystal with 20-ppm error in nominal frequency can drift the clock accuracy by 52 seconds in a month. You can compensate this drift by using the calibration feature in the nvSRAM RTC.

Another crystal parameter that affects crystal clock accuracy is the parabolic curvature constant, k , which changes the crystal frequency with temperature. The parabolic curvature constant, k , is typically -0.036 ppm/°C². If the operating temperature is known, the RTC can be calibrated to compensate for the RTC clock frequency drift due to temperature change.

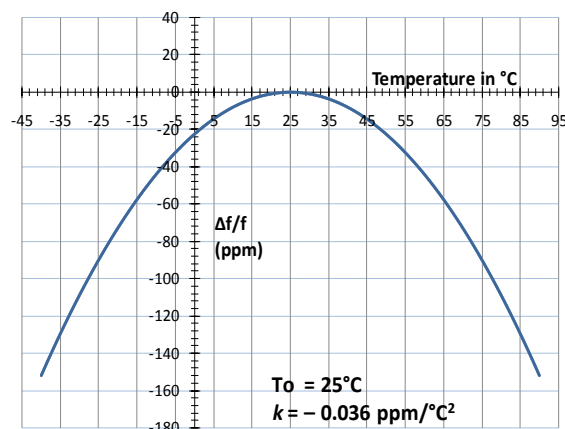
1.1 Typical Crystal Behavior

Though crystal oscillators are one of the most accurate oscillator circuits, the accuracy of the RTC mainly depends on the accuracy of the crystal. Crystals, similar to other common electrical components, such as resistors and capacitors, have certain tolerances associated with them. A crystal that is specified to have a nominal variation of 32.768 kHz at 25 °C may actually have a frequency ± 20 ppm from its nominal frequency. The crystal frequency also varies with temperature changes. Figure 1 shows the parabolic relation between the temperature and crystal frequency. The curve is specified by the crystal manufacturer in terms of turnover temperature (T_o) and curvature (k). The frequency variation as a function of T and k is shown in the following equation:

$$f - f_o = kf_o(T - T_o)^2 \quad \text{Equation 1}$$

The curvature, k , is intrinsic to the mechanical properties of the crystal and can vary from manufacturer to manufacturer. The crystal datasheet gives a typical specification for the curvature. Alternatively, this parameter can be determined empirically by testing the change in frequency output across temperatures. T_o is specified as 25 °C ± 5 °C, and k as -0.036 ppm/°C² ± 0.006 ppm/°C².

Figure 1. Parabolic Temperature Curve of a Crystal



The purpose of the calibration circuit is to adjust this curve by moving it up or down to achieve an accuracy of zero or +1 or -2 ppm at a selected temperature. This is accomplished by adding or subtracting counts from the oscillator divider chain.

1.2 Calibration Methodology

The RTC design in Cypress nvSRAM employs periodic counter corrections. The digital calibration circuit adds or subtracts counts from the oscillator divider circuit as shown in Figure 2. Similarly, Figure 3 shows an example clock diagram that illustrates how extra clock counts are added during positive calibration to speed up the clock, or subtracted during negative calibration to slow it down. The number of pulses added or subtracted is controlled by the data written into the five lower bits, D4 to D0, of the calibration register. These bits can be set to represent any value between 0 and 31 in the binary format. Bit D5 is a sign bit, where a '1' indicates positive calibration and a '0' indicates negative calibration.

Calibration occurs within a 64-minute cycle. The first 62 minutes in the cycle may, once every minute, have one second calibrated. This second may be speeded up (by adding 256 cycles) or slowed down (by subtracting 128 cycles). If a binary 1 is loaded into the register, only the first 2 minutes of the 64-minute cycle is modified; if a binary 6 is loaded, the first 12 are affected, and so on. Therefore, each calibration step has the effect of adding 512, or subtracting 256, oscillator cycles for every 125,829,120 actual oscillator cycles (64 min x 60 sec/min x 32,768 cycles/sec). Adding 512 cycles per 125,829,120 cycles corresponds to 4.068 ppm (512 cycles / 125,829,120 cycles) x 10⁶ ppm). Similarly, subtracting 256 cycles for every 125,829,120 cycles corresponds to a modification of -2.034 ppm ((256 cycles / 125,829,120 cycles) x 10⁶ ppm).

If a '0' is loaded into the sign bit (D5) of the calibration register, it indicates a negative calibration. A binary '1' loaded into bits D4 to D0 modifies the clock by -2 ppm, a binary 2 by -4 ppm, a binary 3 by -6 ppm, and so on. The maximum value of binary 31 modifies the clock by -63 ppm.

A '0' in the Bit D5 (sign bit) implies negative calibration and Number of cycles suppressed (per million cycles) = 2.034 x < value loaded into calibration bits > ppm Equation 2

Similarly a '1' in the sign bit (D5) denotes a positive calibration and,

Number of cycles added (per million cycles) = 4.068 x < value loaded into calibration bits > ppm Equation 3

Thus, a value 1 loaded into Calibration register bits (D4 to D0) modifies the clock by 4 ppm and the maximum value of 31 written into the Calibration register bits (D4 to D0) modifies it by 126 ppm.

Figure 2. Oscillator Divider Circuit

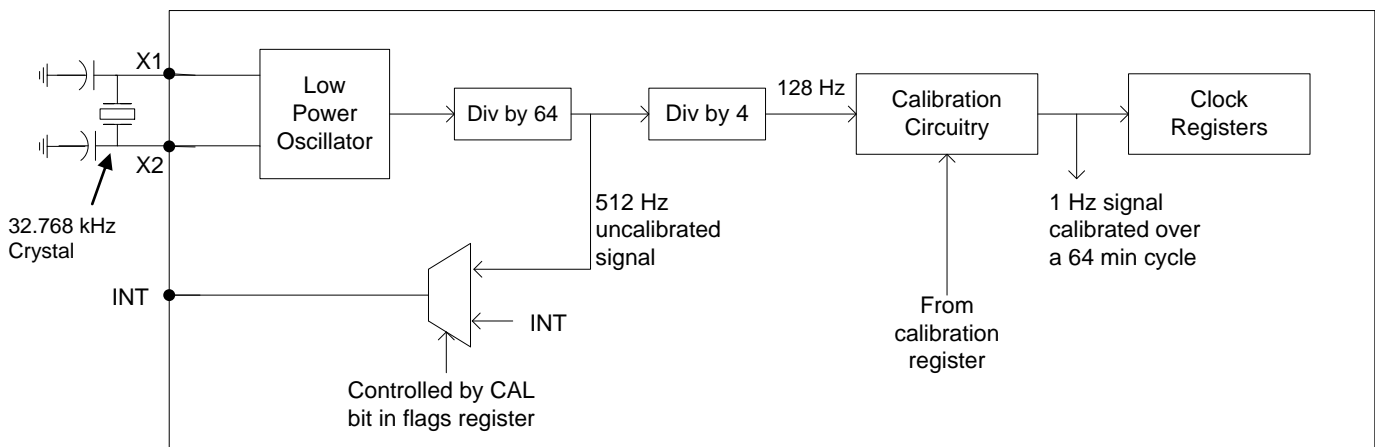
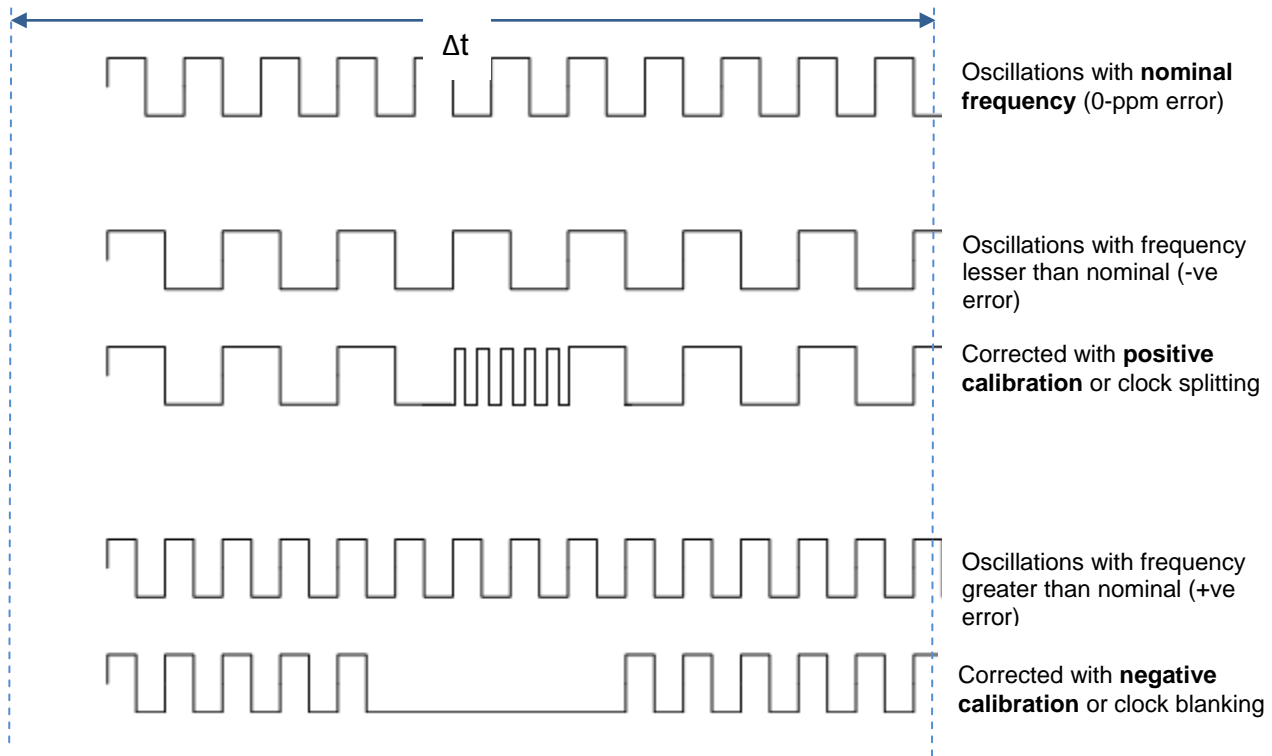


Figure 3. Clock Splitting and Clock Blanking



1.3 Setting the Calibration

1.3.1 Calibration/Control Register

To set the calibration, write an appropriate value into the Calibration/Control register located in the RTC Register Map Table (refer to the respective device datasheet for the RTC Register Map table). The Bit D7 of the Calibration/Control register is the oscillator enable bit and the oscillator runs only when this is set to 0. The Bit D6 is unused and will read 0. The Bit D5 is the Calibration sign bit. Setting the Calibration sign bit D5 to '1' denotes positive calibration, and that the calibration adjustment as specified through the Calibration bit [D4:D0] will be added. Setting the Calibration sign bit D5 to '0' denotes negative calibration and that the calibration adjustment, as specified through Calibration bit [D4:D0], will be subtracted. The binary value in bits D4 to D0, ranging from 0 to 31, determines the amount of calibration to be done (as indicated in Equation 2 and Equation 3 on page 2).

Table 1. Calibration/Control Register

D7	D6	D5	D4	D3	D2	D1	D0
OSCEN	0	Calibration sign	Calibration				

1.3.2 Determining Clock Error

Before setting a calibration value, determine the amount of calibration required. When the CAL bit (bit 2) of the Flags register is set, an uncalibrated 512-Hz clock derived from a 32.768-kHz crystal (shown in Figure 2 on page 2) comes out on the INT pin. This clock output enables an application to determine the error in the crystal's output frequency from its nominal frequency of 32.768 kHz. The deviation of the actual measured frequency from 512 Hz determines the degree and direction of the required correction. The error in ppm can be determined by using Equation 4:

$$Error\ in\ ppm = \frac{(Measured\ frequency - 512)Hz}{512\ Hz} \times 10^6\ ppm \quad \text{Equation 4}$$

For example, if setting the CAL bit in the Flags register causes the INT pin to toggle at 512.01024 Hz, it indicates a 20-ppm oscillator frequency error. Because the correction needed is -20 ppm, a -10 (001010) is loaded into the calibration register. Note that setting or changing the calibration bits does not affect the frequency on the INT pin. Table 2 on page 4 lists the amount of calibration for each value of the calibration register.

Table 2. Calibration Adjustment Values in nvSRAM RTC

Sign	Calibration	Modification in ppm	Time in sec/month ¹	Sign	Calibration	Modification in ppm	Time in sec/month ¹
0	00000	0	0	1	00000	0	0
0	00001	-2	-5	1	00001	4	11
0	00010	-4	-11	1	00010	8	21
0	00011	-6	-16	1	00011	12	32
0	00100	-8	-21	1	00100	16	42
0	00101	-10	-26	1	00101	20	53
0	00110	-12	-32	1	00110	24	63
0	00111	-14	-37	1	00111	28	74
0	01000	-16	-42	1	01000	33	87
0	01001	-18	-47	1	01001	37	97
0	01010	-20	-53	1	01010	41	108
0	01011	-22	-58	1	01011	45	118
0	01100	-24	-63	1	01100	49	129
0	01101	-26	-68	1	01101	53	139
0	01110	-28	-74	1	01110	57	150
0	01111	-31	-81	1	01111	61	160
0	10000	-33	-87	1	10000	65	171
0	10001	-35	-92	1	10001	69	181
0	10010	-37	-97	1	10010	73	192
0	10011	-39	-102	1	10011	77	202
0	10100	-41	-108	1	10100	81	213
0	10101	-43	-113	1	10101	85	223
0	10110	-45	-118	1	10110	89	234
0	10111	-47	-124	1	10111	94	247
0	11000	-49	-129	1	11000	98	258
0	11001	-51	-134	1	11001	102	268
0	11010	-53	-139	1	11010	106	279
0	11011	-55	-145	1	11011	110	289
0	11100	-57	-150	1	11100	114	300
0	11101	-59	-155	1	11101	118	310
0	11110	-61	-160	1	11110	122	321
0	11111	-63	-166	1	11111	126	331

Note 1: One month = 365/12 days.

2 Summary

The simple calibration feature provided by the Cypress nvSRAM RTC device improves timekeeping accuracy. This scheme does not provide an automatic adjustment option to compensate variations that arise due to dynamic changes in ambient temperature. However, the RTC calibration method provides an incremental improvement in accuracy and can compensate for any anticipated temperature drift.

Document History

Document Title: AN53313 – Real Time Clock Calibration in Cypress nvSRAM

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2713135	UNC	06/03/2009	New application note
*A	3709464	ZSK	08/10/2012	Updated template. Fixed typos and minor grammar errors.
*B	4020942	ZSK	06/05/2013	Modified Abstract to align with Application Note contents. Modified Introduction section to add the nvSRAM RTC calibration feature details. Modified the parameter 'k' name from "curvature" to "parabolic curvature constant", which is a more popularly used nomenclature in RTC crystal datasheets. This does not affect the equation or assumed value of 'k' in Equation 1. Other minor enhancements.
*C	4149461	ZSK	10/07/2013	Updated to improve grammar. No content update.
*D	5415054	ZSK	08/25/2016	Updated template
*E	5701654	AESATP12	04/19/2017	Updated logo and copyright.

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