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Spec No: 001-52518

Spec Title: DRIVING LED FIXTURES WITH REDUCED WIRE COUNT - AN52518

Sunset Owner: Madhan Kumar Kuppaswamy [mkku]

Replaced by: 001-52699

Driving LED Fixtures with Reduced Wire Count

Associated Project: No
Associated Part Family: PowerPSoC™ (CY8CLED0xD/G0x)
Software Version: NA
Related Application Notes: None

Abstract

Traditional floating load buck topologies for driving common anode LED Fixtures treat the LED or LED String as a two wire element and run wires for the two sides of the string. Many LED Driver ICs assume this topology; hence require 2N wires for N channels. The added wiring cost is a significant disadvantage. This application note proposes a modified topology to reduce the wires to N+1 for N channels.

Introduction

Switch mode power converters because of their higher efficiency are a better option than linear ballasts (active or passive) for driving high brightness LEDs. Two commonly used topologies are floating load buck converter and standard buck converters. Floating load buck converters offer significant advantages including reduced component count and simple control strategy. The floating load buck converter is named after the fact that the load (in this case the LED string) has both ends floating; that is, they are not referenced to power or ground, unlike a conventional buck converter which can drive a grounded load.

Wiring is a substantial cost in floating load buck systems that have remote loads with long wires running from control electronics to the load. This application note proposes a wiring topology, which substantially reduces wiring cost and simplifies installation for such systems.

Cypress's PowerPSoC™ family of intelligent LED controllers is used to demonstrate this topology. The PowerPSoC family, along with Programmable System-on-Chip™ technology, features high-performance power electronics including 1 A, 2 MHz power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators. This enables creation of intelligent power electronics solutions for LED power management.

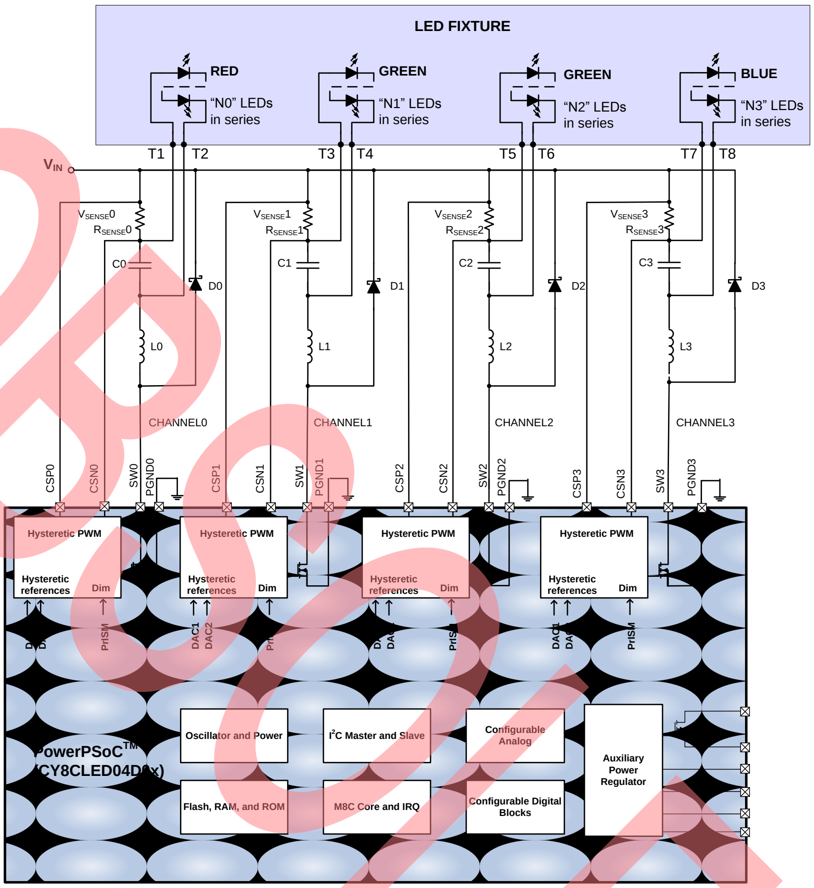
Traditional Floating Load Buck Topology

Figure 1 on page 2 shows PowerPSoC in a traditional floating load buck topology for four channels. Using CHANNEL0 as an example, the internal FET is controlled with a hysteretic control function. The current in the LED string is monitored by measuring the voltage across $R_{SENSE}0$.

The hysteretic controller maintains the current between two thresholds by turning the FET ON when the current drops below the lower threshold and OFF when the current rises above the upper threshold. Therefore, the current is constantly ramping either up or down and the average value of the current is the average of the lower and upper thresholds. By controlling the upper and lower thresholds, the average can be controlled. The diode D0 is the freewheel diode.

The wiring is routed out to the LED fixture to drive the LED strings. The disadvantage is that this circuit requires two wires for each LED string, a total of 2N wires for N LED Strings (Each string may have multiple LEDs in series). Wiring is always a cost and additional wires impose an added cost on the installation.

Figure 1. PowerPSoC in a Traditional Floating Load Buck Topology



Modified Floating Load Buck Topology

The modified-floating load buck topology, as shown in Figure 2 on page 3, positions the current sense resistor below the LED string and also uses a truly differential current sense technique, rather than a sensing technique relative to V_{IN}. Since the sensing is not dependent on V_{IN}, this modified topology has better power supply rejection (PSR).

This modification in the sense resistor's position now enables wiring reconfiguration, allowing reduction in the wire count. A common wire can now be used for all the anodes and one wire each for the cathode end of every string. Thus, all the N strings are now driven with N+1 wires.

The Cypress CY8CLED0xD/G0x controllers with integrated power control have sense amplifiers for differential sensing, enabling this modified topology with no additional components.

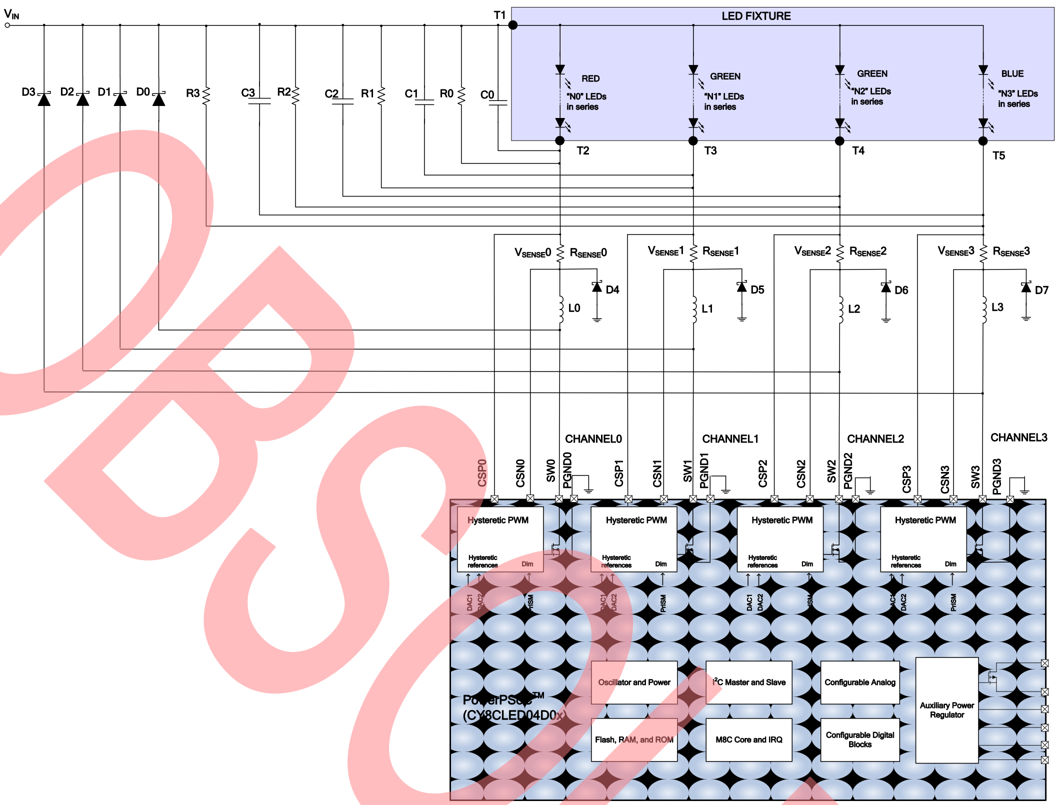
The capacitors C0 to C3 are added if the ripple current in the wiring needs to be reduced. These capacitors are typically small, sub-1 µF. There is no impact on the selection of the inductor and the sense resistor.

The Schottky diodes D4 to D7 are for open circuit protection on the load. They are important especially if the load is connected to the control board using connectors. Any intermittent connections can cause the load to temporarily open circuit. Because the LEDs are in series with an inductor, any open circuit conditions must be protected against. When the load is on the same board as the control electronics and mechanical construction can guarantee against open circuits, these diodes are not mandatory; however, they are recommended. The diodes should be able to withstand the entire load current for a short duration of time.

The resistors R0 to R3 are pull ups, which are discussed in detail in the section Passive Pull Up.

This topological modification works cleanly, and is applicable whether using the integrated or external FETs with PowerPSoC. For the four channels shown there are five connection terminals for the load fixture. T1 is the common terminal and T2 to T5 are channel specific.

Figure 2. PowerPSoC in a Modified Floating Load Buck Topology



Passive Pull Up

A side effect of the modified floating load buck topology (see Figure 2) is that during the OFF phase, when the LEDs are dimmed to zero percent, there is a small leakage current. Most of this leakage is the input bias current for the current sense amplifier. Depending on this and the characteristics of the LEDs, they may appear to be dimly illuminated. This usually does not produce much in the way of illumination. However, there may be a requirement to absolutely turn OFF the LEDs, which requires zero current through them.

This can be achieved by inserting a pull up resistor R0 in parallel with the LED string as shown for CHANNEL0 in Figure 3 on page 4. The pull-up should be placed on the control electronics board as shown in Figure 3 on page 4 across the LED fixture terminals T1 and T2. The pull-up should be sized such that it shunts any leakage current through the LED string when the LEDs are supposed to be turned OFF. Every channel requires its own pull-up as shown in Figure 2.

The following example describes how to select these pull ups. Figure 3 on page 4 shows a PowerPSoC device driving a load of six LEDs on CHANNEL0. Assume each LED has a minimum forward voltage drop of 3 V and a maximum forward voltage drop of 3.5 V. This results in a $V_{F,LOAD}$(min) of 18 V and a $V_{F,LOAD}$(max) of 21 V for the LED string. The worst case leakage I_{LEAK}(max) is 1 mA.

The pull up can be sized using the following rule of thumb

$$R_{PU} = \frac{V_{F,LOAD}(\min) \cdot k_1}{I_{LEAK}(\max)} \quad \text{Equation 1}$$

Here R_{PU} is the value of the pull up resistor and $V_{F,LOAD}$(min) is the minimum forward voltage drop for the LED string. The forward voltage is multiplied by a fractional constant k_1 as a guard-band to ensure R_{PU} always provides a lower resistance path for leakage. I_{LEAK}(max) is the maximum leakage through the LEDs during the OFF phase. I_{LEAK}(max) in our case is 1 mA. Let us select $k_1 = \frac{1}{2}$.

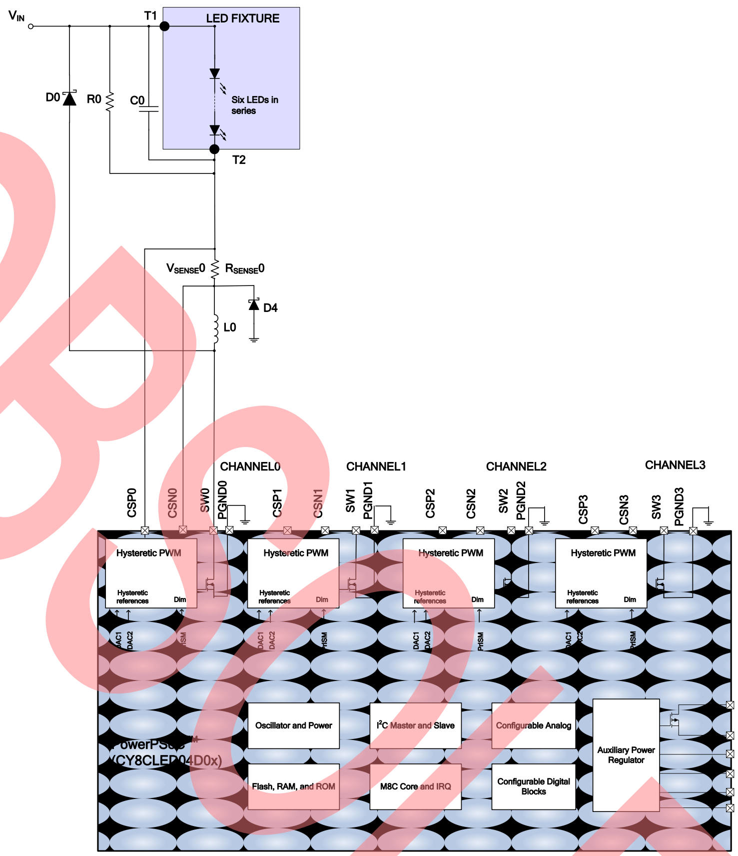
Hence R_{PU} = 9 kΩ

Let us calculate the power dissipation through this pull-up (PD_{PU}) when the LEDs are completely turned ON.

$$PD_{PU} = \frac{V_{F,LOAD}(\max)^2}{R_{PU}} \quad \text{Equation 2}$$

PD_{PU}, turns out to be 0.049W. So a ¼W resistor is sufficient. The power dissipated in the resistor is less than 0.25 percent of the total power consumed by the load. Thus the selection of k_1 governs PD_{PU}.

Figure 3. System Solution with Passive Pull Up



Choosing the Right Topology

The modified topology can save substantial wiring cost for systems having remote loads with long wires running from control electronics to load. However, if the load is on the same board as the control system this topology may be less attractive.

Although the modified topology comes with the cost advantage of reduced wiring, when compared with traditional floating load buck topology, there are a few points to consider.

- Added design complexity with addition of passive pull ups.
- The amount of voltage available to the LED string is lower as compared to the traditional floating load buck topology. The key is to examine the excess of input voltage over the LED voltage (the so called voltage headroom).
- Requirement of protection diodes when using this wiring scheme for systems having remote loads, to protect against open circuits.

Summary

The modified floating load buck topology proposed in this application note substantially reduces wiring cost and simplifies installation for systems having remote loads. This topology enables differential sensing by the current sense amplifier, which in turn improves Power Supply Rejection. Choosing a particular topology should be based on the type of load - whether the load is remote or is on the same board as the control electronics - and the voltage headroom available in the application. The PowerPSoC family of devices can be used with either topology to create a highly integrated solution.

Document History

Document Title: Driving LED Fixtures with Reduced Wire Count – AN52518

Document Number: 001-52518

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2678765	KJV/KDG	03/25/2009	New application note.
*A	2683533	VED	04/03/2009	Release to external web site
*B	3556565	MKKU	03/20/2012	Removed ‘About the Author’ section and author details in the document.
*C	3917961	MKKU	03/12/2013	Obsolete spec.

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