Latch-up prediction for SCR TVS device

Latch-up considerations in highspeed interfaces

About this document

Scope and purpose

1. This document describes the different characteristic of ESD protection devices (TVS diodes) from the standard one up to the most efficient SCR (Silicon Controlled Rectifier) structures.
2. ESD protection devices based on SCR structures can cause a “latch-up”. Based on a “load-line analysis” stable operating conditions of SCR based ESD protection devices in various applications become visible.
3. A detailed latch-up analysis is performed for HighSpeed interfaces e.g. USB3.x, HDMI,…

Intended audience

This document is intended for design / application engineers using Infineon’s high performance SCR based ESD protection devices without latch-up issues.

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1 Introduction of AN525

1.1 ESD protection – inline with miniaturization of the semiconductors

Increasing data rate in digital interface circuits and continuous miniaturization of semiconductor structures, ESD susceptibility becomes a severe problem. Dedicated ESD protection, especially for the external high speed interfaces is mandatory on the PCB in front of the IC I/Os. Moving forward in the technology nodes, the maximum tolerated ESD clamping voltage (V_{t2}) at the IC I/Os vs. GND and the maximum ESD current (I_{t2}) capability continuously decreases.

To ensure the ESD robustness of an entire system, on-board system ESD protection is implemented on the PCB close to the ESD entry point, normally close to the external interface connector. This on-board ESD protection structure is called “System Level ESD Protection”.

System level ESD robustness is tested according to IEC61000-4-2.

Transmission Line Pulse measurement technique is used to compare the high current IV characteristic of ESD protection devices as well as IC I/Os. The TLP measurement is well defined, highly reproducible and fits to the ESD System Level performance of the ESD device or the IC I/O quite well. Referring to the Infineon Application Note AN210 describing the TLP measurements principle [1].

High speed interfaces e.g. USB3.x, DisplayPort (DP), Thunderbolt, HDMI2.0 withstand only a low maximum ESD clamping voltage (V_{t2}) at the I/Os, sometimes lower than the IC´s supply voltage at the Vcc node. This low V_{t2} in combination with a low maximum ESD current (I_{t2}) increases the effort for system level ESD protection according IEC61000-4-2.

2 Principal I/V response of different TVS diode types

State-of-the-art system level ESD protection devices are based on pn-diodes or npn-structures operating in reverse condition (Figure 1). Exceeding the trigger voltage (e.g. via an ESD event), the ESD clamping voltage of the “Avalanche TVS diode” stays above the trigger voltage (Vt1). For the “Snapback TVS diode type”clamping voltage reduces below trigger voltage (Vt1) to a holding voltage (Vh).

The snapback TVS diode type achieves a lower ESD clamping voltage compared to Avalanche TVS diodes.

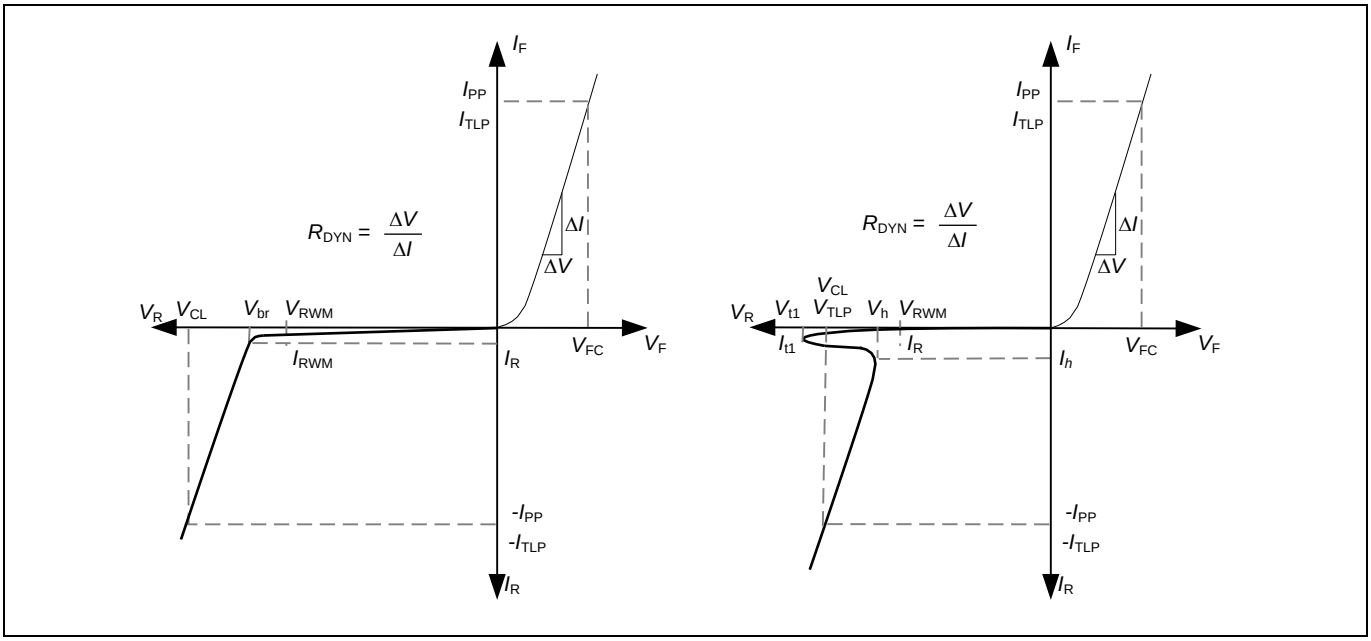


Figure 1 ESD protection device characteristic: 1a: Pure Zener 1b: snap-back device

Abbreviation

V_R … Reverse voltage
V_{RWM} … Reverse working voltage max.
V_{CL} … Clamping voltage
V_{t1} … Trigger voltage
V_{br} … Breakdown voltage
V_h … Holding voltage
V_{t2} … V_{CL} max: < V_{t2} (destruction limit)
V_F … Forward voltage

R_{DYN} … Dynamic resistance

I_R … Reverse current
I_{PP} … Peak pulse current
I_{TLP} … TLP current
I_{t1} … Trigger current
I_{br} … Breakdown current
I_h … Holding current
I_{t2} … V_{TLP} max: < I_{t2} (destruction limit)
I_F … Forward current

The ESD performance of TVS devices is improved by continuous reduction of the ESD clamping voltage.

- Increased snapback has to consider the working voltage of the application. For direct current (DC) supply it is mandatory to ensure $V_{hold} > V_{cc}$
- Lowest dynamic resistance.

SCR based TVS structures have a much lower holding voltage (V_{hold}) after triggering compared to snapback TVS diodes (Figure 2).

Exceeding the trigger voltage of a SCR device, the clamping voltage across the ESD device (V_{clamp}) reduces to a significant lower value of less than 2V and reduces the residual ESD stress for the IC I/Os significantly.

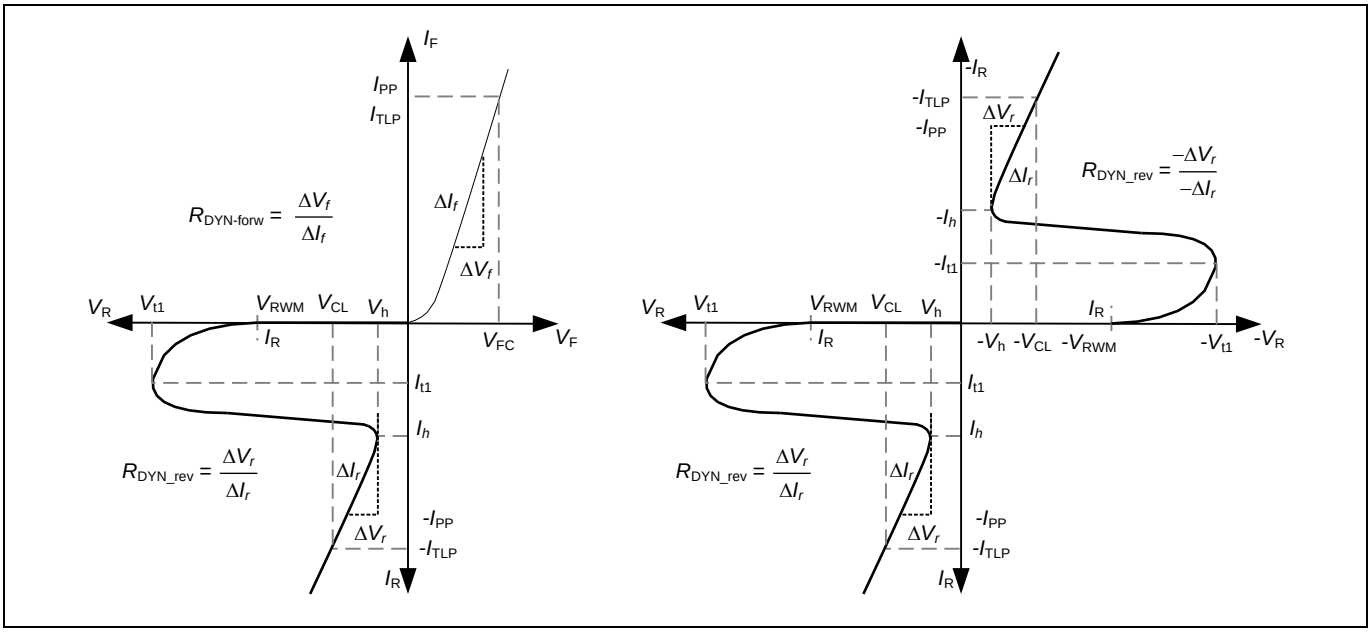


Figure 2 SCR ESD protection device. a: uni-directional SCR b: bi-directional SCR

2.1 How to deal with a potential latch-up in SCR devices

The strong snap-back to a low holding voltage (V_{hold}) cause a potential risk for “latch-up”. The SCR structure moves into latch-up mode by an ESD event / voltage glitch ($V > V_{trig}$) and is “locked” in conducting mode (ON mode). The supply bias (-voltage and –current) keeps the latched SCR device ON state even after the ESD strike decays. The SCR device drains a huge (DC) current through, resulting in a device damage caused by Electrical Over-Stress (EOS).

Requirements to drive the SCR device into latch-up mode (both topics must be fulfilled):

- applied bias voltage must be higher than V_{hold} ($V > V_{hold}$) **AND**
- applied bias source current higher than I_{hold} ($I > I_{hold}$)

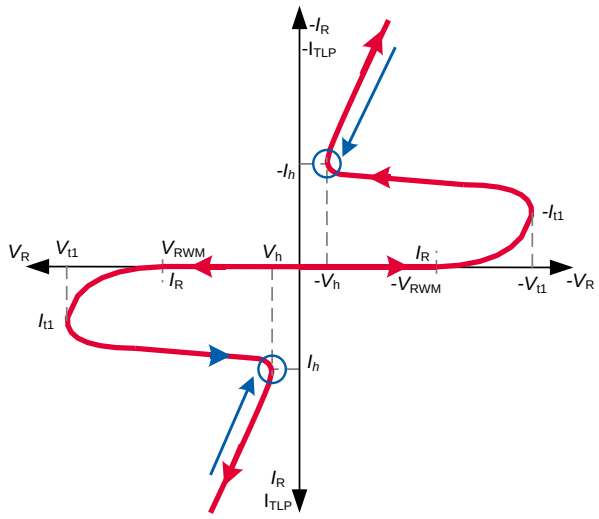
Latch-up state is terminated by : $V < V_{hold}$ **OR** $I < I_{hold}$ **OR** power down

An SCR based ESD protection approach in a dedicated application must be inherent latch-up safe!

SCR structure is inherent latch-up safe if : $V_{hold} > V_{bias-max}$ **OR** $I_{hold} > I_{bias-max}$

SCR based ESD protection devices utilize the strong snapback to achieve improved ESD performance (lower clamping voltage). Therefore, $V_{hold} > V_{bias\text{-}max}$ is NOT always fulfilled and $I_{hold} > I_{bias\text{-}max}$ is mandatory.

In Figure 3 the red trace shows the dynamic I/V behavior for different TLP/ESD events applied to the SCR based protection device. For the TLP/ESD event the I_{TLP} always passes the I_{hold} area and stays above I_{hold} as long the TLP/ESD pulse lasts. After the TLP/ESD pulse decays, I_{TLP} decreases (blue trace). In case there is a $V_{bias} > V_{hold}$ applied which can serve an $I_{bias} > I_{hold}$, the SCR device remains in the I_{hold} respectively V_{hold} region and is locked in latch-up mode.



SCR characteristic rising ESD strike

- triggered by an ESD strike (V_{t1}, I_{t1}),
- snapback to low hold voltage (V_{h1}, I_{h1})
- follow the resistive branch of large signal I/V curve

=> low clamping voltage @ high ESD current

SCR characteristic falling ESD strike

- follow down the resistive branch of I/V curve to V_{h1}
- - IF NO bias / bias + signal < V_{h1} => SCR is "OPEN"
- - IF bias/ bias + signal >= V_{h1} & I_{bias} + signal > I_{h1}

=> SCR locks in the "conducting latch-up" state

Figure 3 Latch-up path for the bi-directional SCR ESD device

2.2 Load Line analysis to predict the latch-up in the I/V plane

For a better understanding of the latch-up scenario we perform a load-line analysis [2] for actual high speed interfaces. The high speed PHY driver is described by a voltage source, a serial driver resistance and the protection device (TVS diode) (**Fehler! Verweisquelle konnte nicht gefunden werden.**).

On one hand (protection device = OPEN), the maximum possible voltage across the protection device is visible: V_{dd} @ I_{ss} = 0 (ref. point #1) ref. to (Figure 4).

On the other hand (protection device = SHORT), the maximum current through the protection device is given by: $I_{ss\_max} = V_{dd}/R_s$ (ref. point #2), (Figure 4).

In the current−voltage plane (I/V-plane), a line (the load−line) links these two points (Figure 6.). Any point located above this load−line is a stable operating point of the application circuit.

In a load line analysis the linear I/V characteristic of the load line and the nonlinear characteristic of a TVS diode are superimposed (Figure 6).

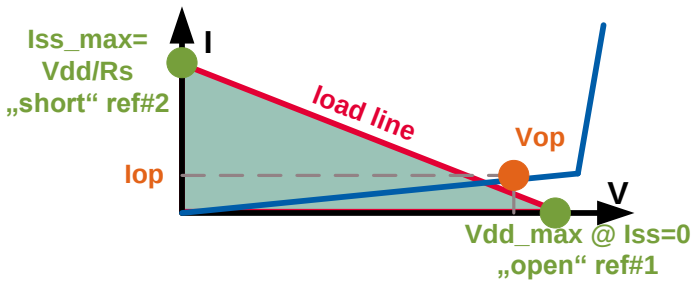


Figure 4 Load line example

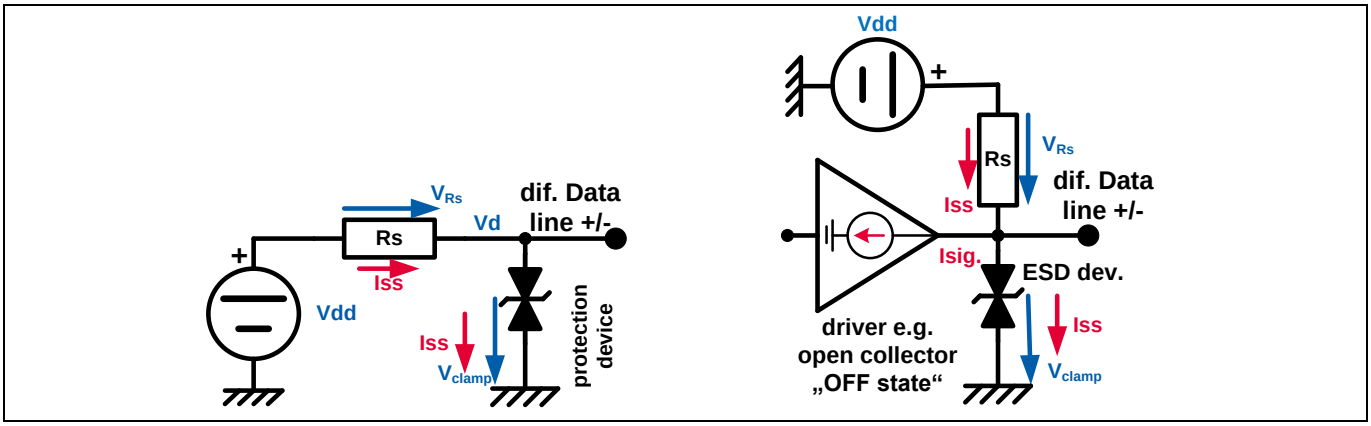


Figure 5 Schematic of the TVS environment for Load-Line Analysis

For a pn-diode like TVS device characteristic, there is only one unique intersection point (operating point – OP). This stable OP is located before $V_{trigger}$ and the correlating I_{op} is very low (leakage current). A pn-diode based ESD protection device is latch-up free, because of one unique OP (Figure 6).

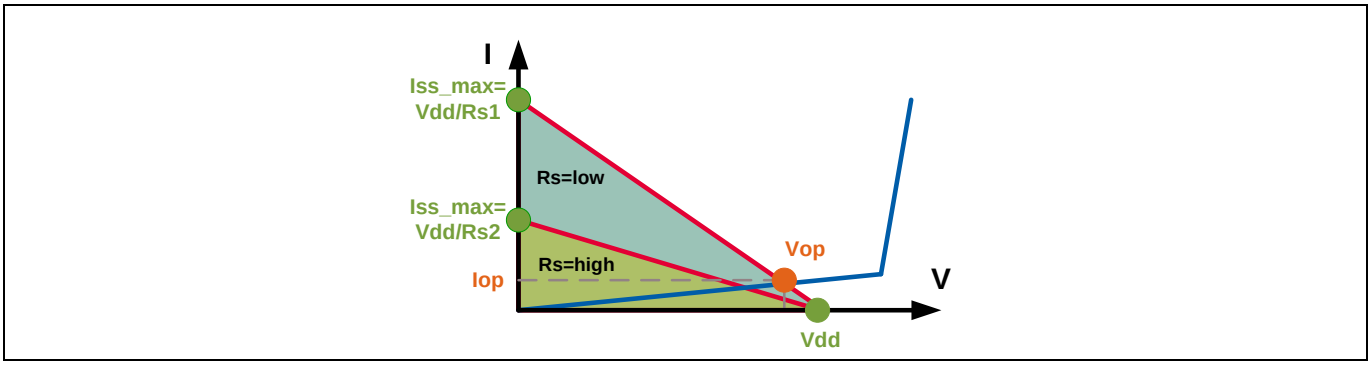


Figure 6 Load line analysis for a pn-diode like TVS diode –latch-up save

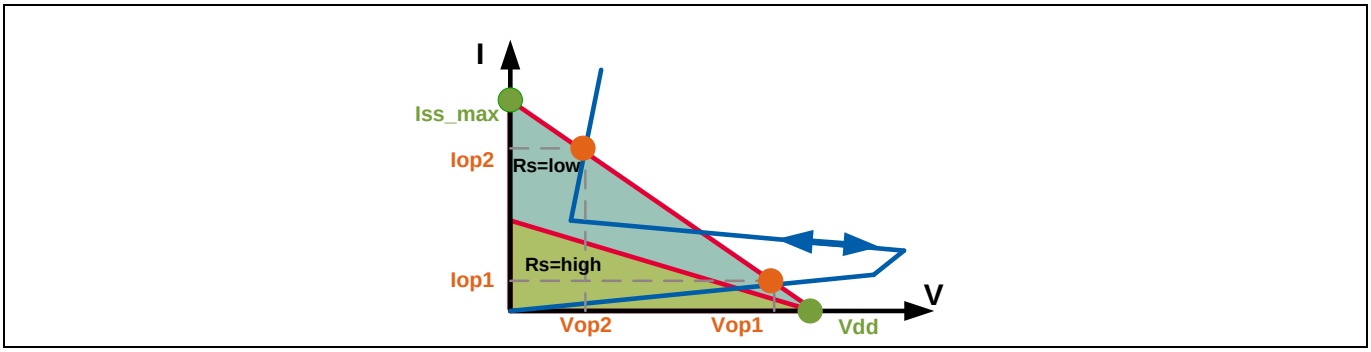


Figure 7 Load line analysis for a SCR based TVS diode – latch-up critical

A SCR based ESD protection device offers more than one intersection point, meaning several stable operation points. The lower one (V_{op1}, I_{op1}) is the normal one in the leakage current domain. The other one (V_{op2}, I_{op2}) is much more critical, because latch-up conditions are fulfilled (Figure 7).

The system becomes latch-up free after OP2 disappears (Figure 8, Figure 9).

To become inherent latch-up free following requirements have to be fulfilled:

- Increase of Rs value (Figure 8)
  Rs is defined by the application and can not be changed easily.
- Increase of the holding current (I_{hold}) of the SCR based ESD protection device (Figure 9).

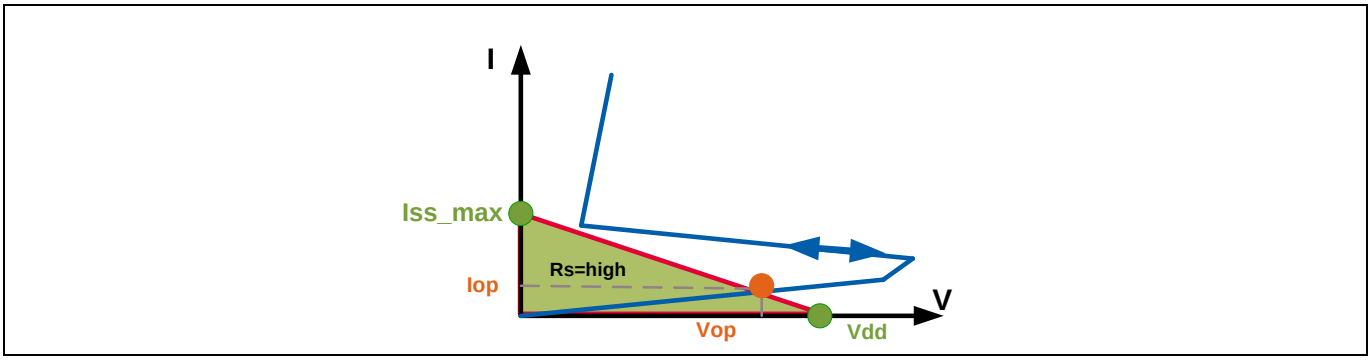


Figure 8 Inherent latch-up save by high Rs

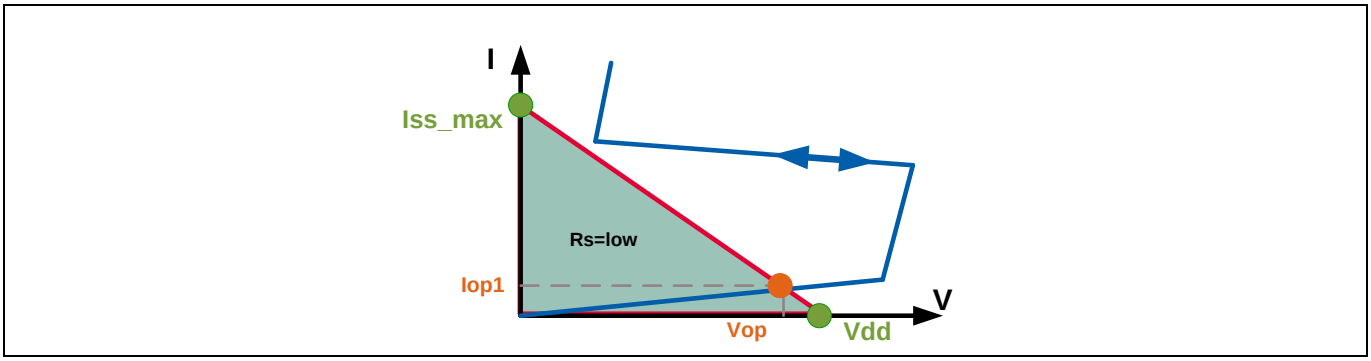


Figure 9 Inherent latch-up save by high Rs

A higher R_s in an application reduces the required minimum I_{hold} of the SCR based ESD protection device to reducethe latch-up risk. Applications with a low R_s, require a high I_{hold} for SCR based ESD protection devices.

Latch-up situation for DC supply line:

DC supply lines show a low R_s. Furthermore they are often buffered with a huge capacitor. In case $V_{cc} > V_{hold}$ of the SCR based ESD protection device, as high latch-up risk is present.

- Inherent latch-up free for DC applications : $V_{hold} > V_{cc}$

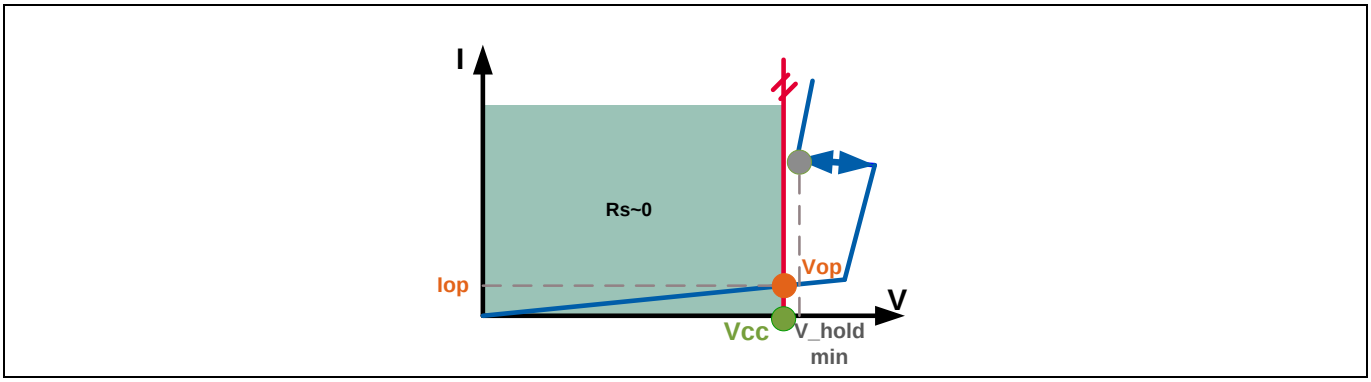


Figure 10 DC supply lines are latch-up free in case of $V_{cc} > V_{hold}$ for a SCR based ESD protection device

Latch-up situation for AC lines with and without bias:

The latch-up situation on AC lines is more relaxed.

Signals on DC bias free AC/RF lines are continuously alternating and stay below the trigger voltage of the ESD protection device. In case of an ESD event (trigger voltage is exceeded), the SCR based ESD protection device latches until the next AC signal period and terminate the latch-up state. This latch-up self turn-off capability makes the DC bias free AC/RF line latch-up save.

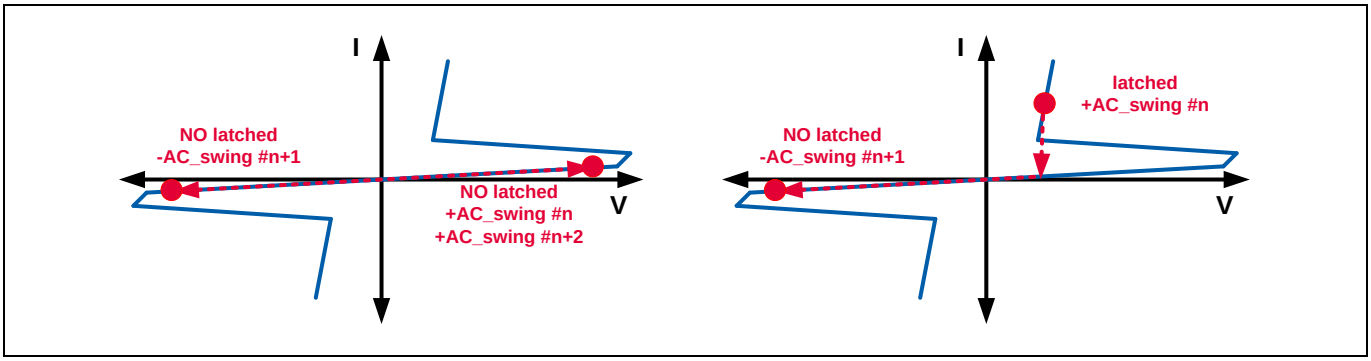


Figure 11 Latch-up "self turn off" of DC bias free AC line

The trigger voltage and -current of the SCR based ESD protection device must be high enough to avoid clipping/ distortion of the RF signal swing (Figure 11). RF signals induce displacement currents in the SCR structure which trigger the ESD protection device and lead to clipping/distortion of the RF signal.

The system is NOT inherent latch-up save, but terminates the latch-up after every RF periode.

DC biased large signal RF/AC lines can benefit from the "latch-up self turn off" behavior in case of a large RF/AV signal whichfalls below V_{hold} every swing/period (Figure 12).

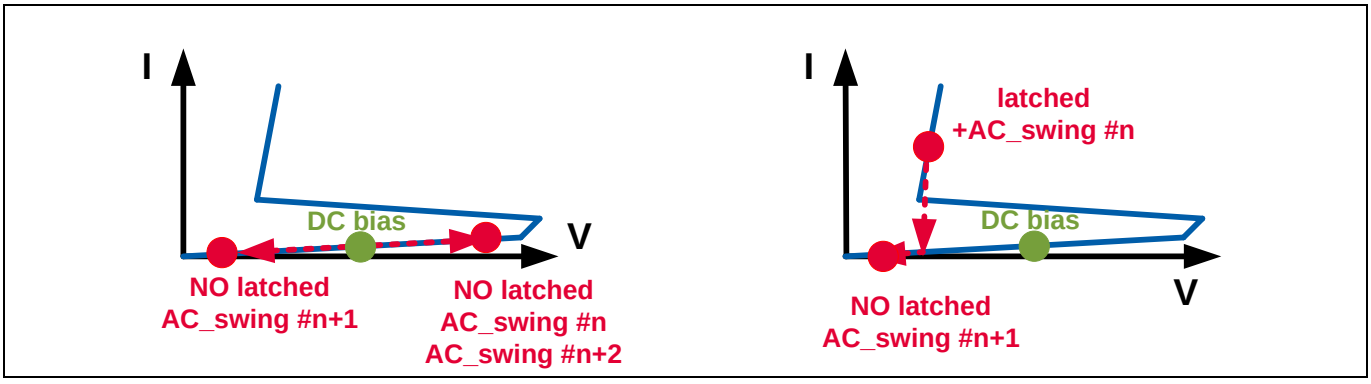


Figure 12 Latch-up situation for a DC biased large signal RF/AC line

For a biased small signal RF/AC lines, NO "latch-up self turn off" effect is supported and the latch-up risk is identical to a normal signal line (Figure 7):

SCR structure is inherent latch-up safe if : $V_{hold} > V_{bias-max}$ **OR** $I_{hold} > I_{bias-max}$

3 Latch-up situation for highspeed data interfaces

3.1 Latch-up analysis for the USB2.0 data bus

USB2.0 transceivers (Tx/RX) can be limited to USB1.1 functionality, providing LowSpeed (LS) and FullSpeed (FS) modes only. Other USB2.0 transceivers (TX/RX) support LS, FS and HS mode (Figure 13). This has an impact on the final R_s value important for the required SCR holding current ($I_{hold\text{-}SCR}$). For USB2.0 specification we refer to [3].

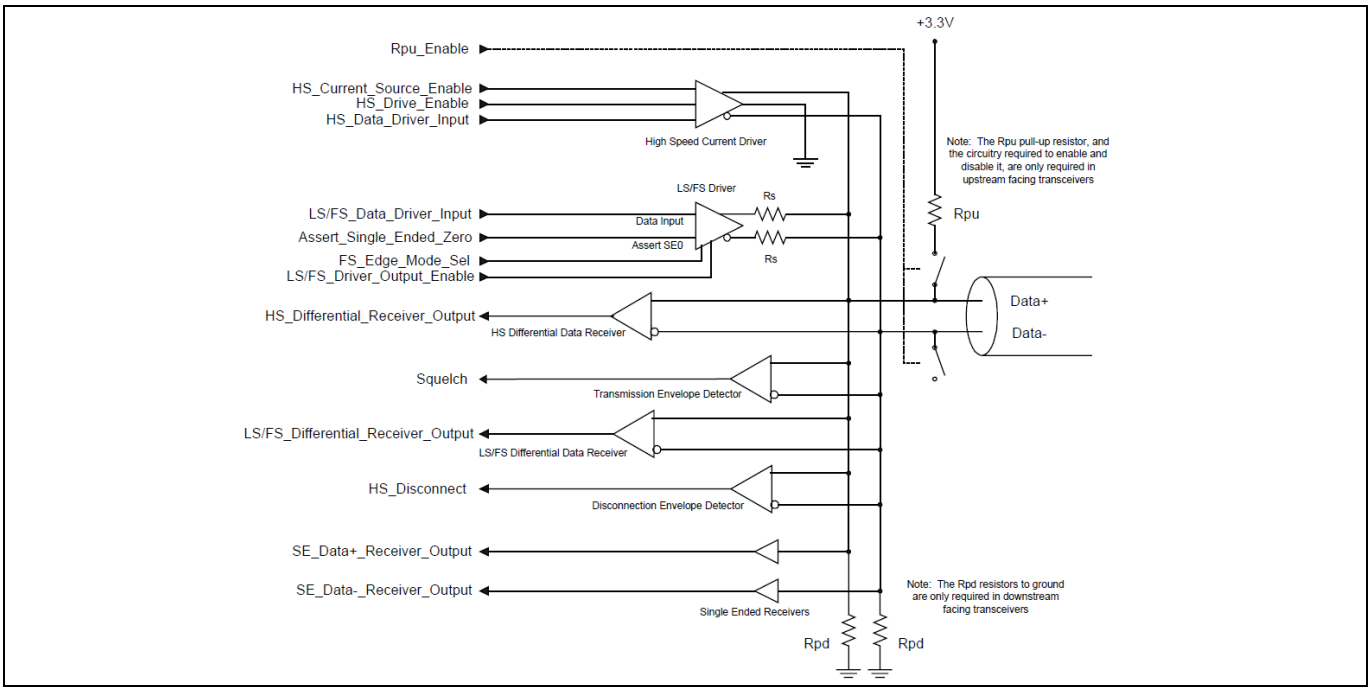


Figure 13 USB2.0 LS/FS/HS Transceiver [3].

Basic requirement for latch-up in the 2.0 LS / FS system:

- V_{dd} @ driver output in “high” state (**in front of Rs**) NON latch-up: 3.6V max
- V_d @ driver output in “high” state (**after Rs**) NON latch-up: ~3.6V max (RL>1k)
- V_d > SCR´s holding voltage ($V_{hold\text{-}SCR}$)
- I_{ss} = latch-up current I_{ss} >= SCR holding current ($I_{hold\text{-}SCR}$)

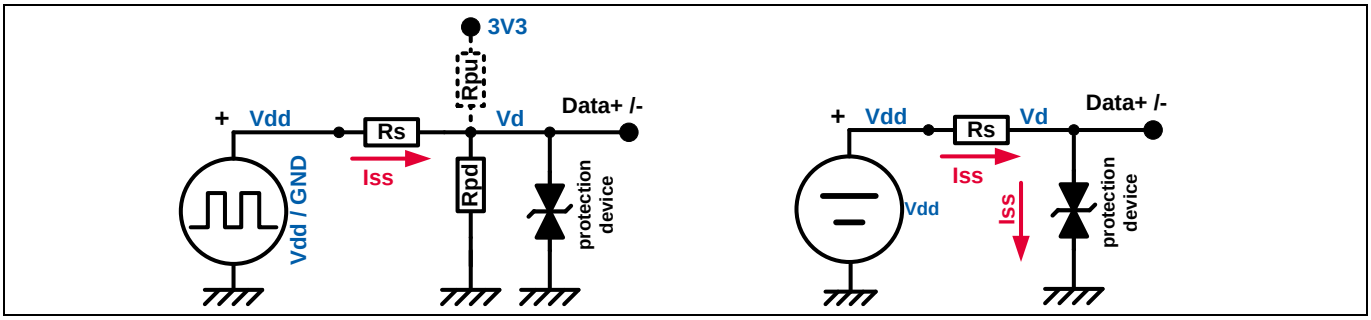


Figure 14 Equivalent and simplified circuit of LS and FS driver for USB2.0 Latch-up analysis

Boundary conditions for USB2.0 TX/RX WITHOUT HS capability (refer to USB1.1 mode) [3], Figure 14:

- R_s (LS/FS mode only TX/RX sys.) [Ohm]: 28 min 44 max 28 wc

Boundary conditions for USB2.0 TX/RX WITH HS capability (typical USB2.0 transceiver) [3], Figure 14:

- R_s (LS/FS mode in HS TX/RX sys.) [Ohm]: 40 min 50 max 40 wc
- Driver V_{dd} [V]: 2.8 min 3.6 max 3.6 wc

V_{dd_wc} is lower in loading case e.g. in latch-up case. The pull-up (R_{pu}) and pull-down (R_{pd}) resistors are ~1k5 Ohm respectively ~15 kOhm. Because of their high value respectively to Rs they are not taken into account here.

To stay inherent latchup save @ V_{dd} = 3.6V:

$V_{hold\ SCR} > 3.6V$ **OR** $I_{hold\ SCR} >= (V_{dd\ wc} - V_{hold\ SCR})/R_{s\ wc}$ **is required**

Example for USB2.0 TX/RX with HS capability (typical USB2.0 transceiver):

- $V_{hold\text{-}SCR}$ = 2V $I_{hold\text{-}SCR}$ >= (3.6V-2V)/40 Ohm =40mA
- $V_{hold\text{-}SCR}$ = 1V $I_{hold\text{-}SCR}$ >= (3.6V-1V)/40 Ohm = 65mA

Important remark:

The latch-up possibility in the **USB2.0 LS/FS system** is very low, because the fundamental requirement is a permanent “high” triggered LS/FS signal source, fixed to V_{dd}. This happens only in present of a close (shielded) link with connection to the responding RX side (Figure 14). High glitches on D+/D- exceeding the trigger voltage of the SCR, or residual ESD impact through cable-jacks or via airgaps or directly into the equipment are remaining issues for latch-up in USB2.0.

For USB2.0 (HS) we face following situation.

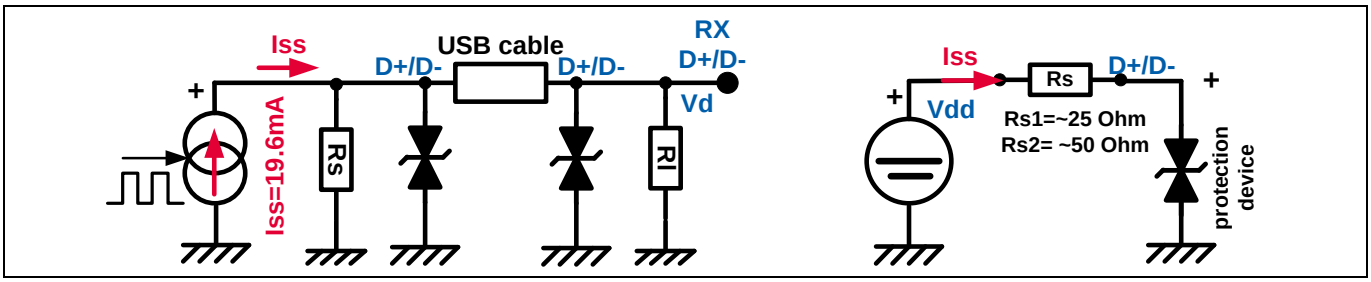


Figure 15 Equivalent circuit of USB2.0 HS driver environment to check latch-up

- R_s (HS mode) [Ohm]: 40.5 min 49.5 max
- Driver I_{ss} [mA]: 16.2 min 19.6 max 19.6 wc

Scenario1 – complete USB link w. TX and RX section. Iss is high state (I_{ss} via R_s//R_l):
Driver V_{dd} [V] = I_{ss}*R_{s1} => 19.6mA* 25 Ohm = ~0.5V

Scenario2 (should NOT be possible) – broken USB link. TX and RX are separated. Iss is high state via R_s.
Driver V_{dd} [V] = I_{ss}*R_{s2} => 19.6mA* 50 Ohm = ~1V

Summary: USB2.0 LS/FS and for HS PHY types

For USB2.0 LS/FS there is a certain minor Latch-up risk for $V_{hold\text{-}SCR}$ < 3.6V, BUT a latch-up situation can only occur under very special circumstances.

The USB2.0 HS link is inherent latch-up save for $V_{hold\text{-}SCR}$ > ~0.5V (1.0V).

3.2 USB3.0 / 3.1 Latch-up analysis

Universal Serial Bus Revision 3.1 Specification [4]

The USB 3.0/3.1 interface uses two differential pairs for SuperSpeed (SS) Gen1 (5Gb/s) or for Gen2 (10Gb/s). The SSTX pair is dedicated for TX (transmit), the SSRX for RX (receive). The third differential lines are used for the USB2.0 HighSpeed capable link. The latch-up situation for the USB2.0 HS link was discussed in the previous section. Power supply e.g. for the “device”, is supported by a 5V Vcc line and the correlating GND line.

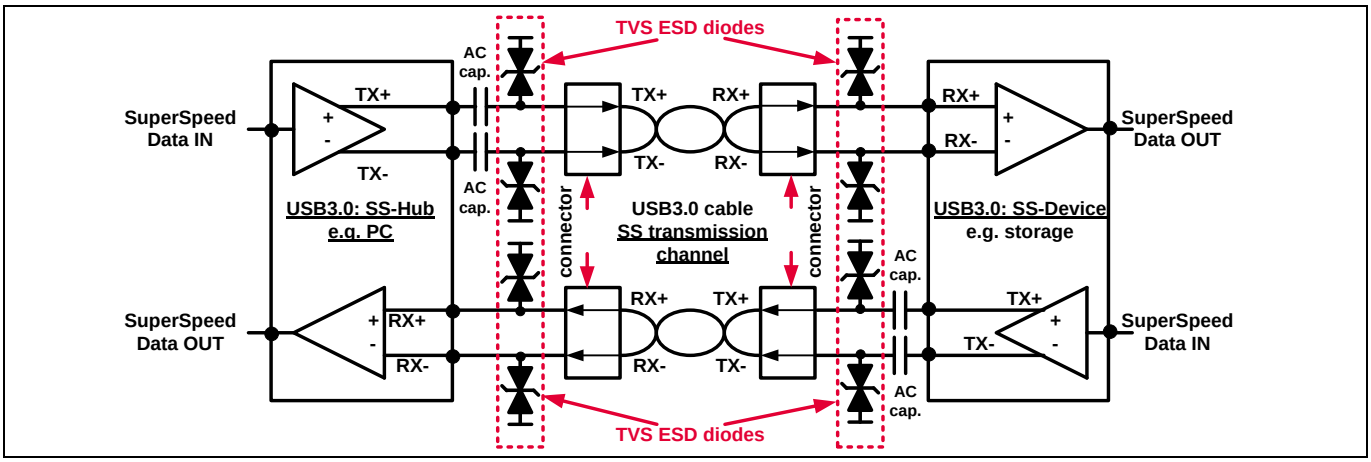


Figure 16 SuperSpeed connection between two USB3.x devices acc. case 2,3

The data lines are AC coupled at the TX side, resulting in a different common mode at the IC side and the connector side of the AC coupling capacitor. The value of the coupling capacitor is huge, because the “low frequency communication signal” must pass. Furthermore the low side cut off frequency of the SuperSpeed Gen2 (10Gb/s) data signal (coding 128b/132bit) is low.

According USB3.0/3.1 specification [4] http://www.usb.org/developers/docs/usb20_docs/we are facing following waveform for V_{DIFF} and V_{CM} (Figure 17).

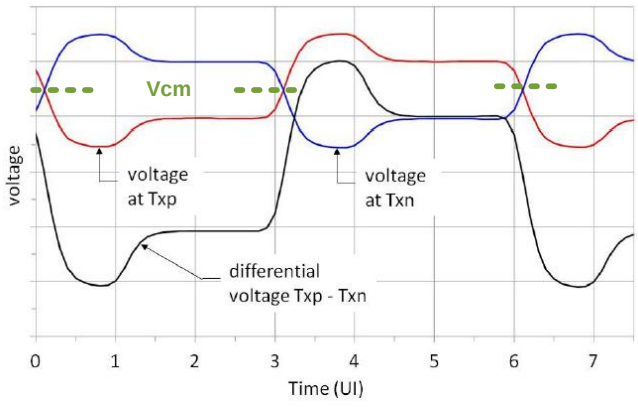


Figure 17 Single-ended and Differential Voltage Levels on USB [4]

There are 3 cases for potential latch-up scenarious on the USB3.0/3.1 SuperSpeed lines.

- **CASE 1 – closed / open link:** The ESD prot. device is placed betw. the TX PHY output and the AC coupl. cap. **This case is NOT save for AC caps**. ESD transients can destroy AC caps + latch-up risk @ TX.!!!.

Nevertheless, latch-up scenario for case 1 is rated as following:
The transmitter output at each line (TX_p and TX_n) is affected by $V_{DIFF} + V_{CM}$.

In the USB3.0 spec. [4] only V_{DIFFpp} is specified for the "Transmitter Normative Electrical Parameters".
In "Transmitter Informative Electrical Parameters at Silicon Pads" V_{CM} is stated.

  - V_{DIFFpp} = 1.2V max => V_{DIFp} = 0.5* V_{DIFFpp} V_{DIFp} = 0.6V max (Figure 17, Figure 18)
  - $V_{CM\_(Vdd)} = V_{CM\_(Vd)}$ = 2.2V max, because NO I_{CM} via Rs in NON latch-up mode.
    "The Instantaneous allowed DC CM voltage at the con. side of the AC coupl. cap"
    => so we assume V_{CM} = 2.2V max @ transmitter side of AC coupling capacitors as well

Combining V_{CM} with V_{DIFp} we get V_d max @ TX_p and TX_n vs. GND: 2.2V +0.6V = 2.8V

Boundery conditions for USB3.0/3.1 Gen1/2 TX/RX [4]

- Rs [Ohm]: 36 min 60 max 36 wc

To stay inherent latchup save @ $V_{d\text{-}max}$ = 2.8V:

$V_{hold\ SCR} > 2.8V$ **OR** $I_{hold\ SCR} >= (V_{dd-max} - V_{hold\ SCR})/R_{s\ wc}$ **is required**

Example for $I_{hold\text{-}SCR}$ as a fuction of $V_{hold\text{-}SCR}$.

- $V_{hold\text{-}SCR}$ = 2V $I_{hold\text{-}SCR}$ >= (2.8V-2V)/36 Ohm =~22mA (ONLY TX-SCR latch)
- $V_{hold\text{-}SCR}$ = 1V $I_{hold\text{-}SCR}$ >= (2.8V-1V)/36 Ohm = 50mA (ONLY TX-SCR latch)

CASE 1 is NOT inherent latchup save under all conditions !!!!
CASE 1 is NOT the regular use case because of risk for AC coupling caps and the latch-up situation!

- **CASE 2-closed link:** The ESD prot. device is placed betw. the AC coupl. cap. and the USB3 con. (Figure 16). **CASE 2 Correct placed ESD protection.** TX section and RX section connected via USB3 cable => closed link.

Major difference to case 1 is **the SCR is NOT facing a permanent DC source any more**. The AC blocking capacitor separates the DC-TX domain ($V_{CM\text{-}TX}$) from the DC-RX TX domain ($V_{CM\text{-}RX}$). On RX side there side NO DC source which can force a latch-up. According [4] for $V_{CM\text{-}RX}$ it is mentioned:
"Instantaneous allowed DC CM ($V_{CM\text{-}RX}$) voltage at the connector side of the AC coupling capacitor is: 2.0V" which is $V_{displacement}$, generated by the TX section. The AC coupling capacitor is discharged quite fast via the DC path of the RX section.

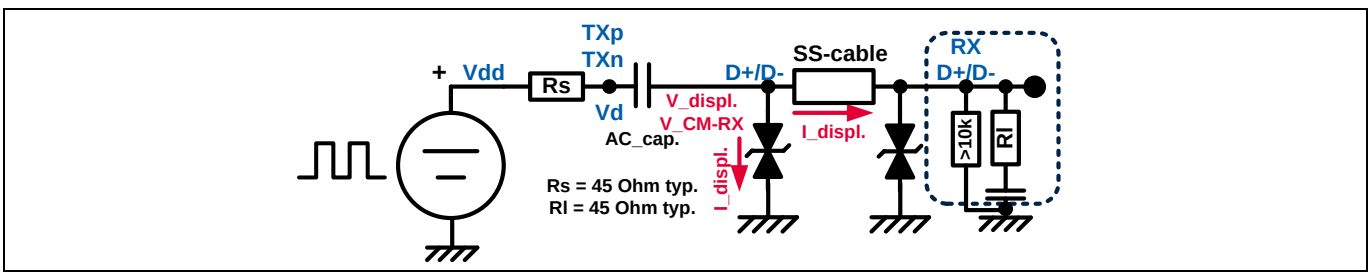


Figure 18 Typical ESD protection structure regarding latch-up in USB3.x SS-lines (case2)

CASE 2 is inherent latchup save under all conditions

- **CASE 3-open link :** The ESD device is placed acc. case 2, BUT the link is open. NO TX / RX connection.

Here we focus on the TX section (incl. ESD protection) BUT without connected RX section. The only difference respective case 2 is there is NO RX DC path. $V_{displacement}$ is NOT dischared quite fast because of lacking RX DC path. We are facing up to 2V for $V_{CM\text{-}RX}$ (V_d) in this case. If the SCR provides a $V_{hold\text{-}SCR}$ = < 2V, a latch-up is possible, until $V_{displacement}$ < $V_{hold\text{-}SCR}$ by discharging ($I_{displacement}$). In the described scenario, no latch-up situation is possible.

CASE 3 is inherent latchup save.

Summary:

The USB3.0/3.1 SuperSpeed link is inherent latch-up save placing the SCR according case 2 and case3. In general, it is not recommended to use the ESD protection device according to case 1 anyway to avoid an ESD EOS for the AC coupling capacitors.

3.3 Thunderbolt Version 1,2,3

Thunderbolt interface was defined by INTEL to run highest data rate.
Thunderbolt Version 1 and 2 provides 10Gb/s per lane, Version 3 is speeded up to 20Gb/s per lane.
Each Thunderbolt connection shows 2 TX lanes and 2 RX lanes driving two TB channels.
For Version 2 and Version 3 data on two lanes (two channels) can be logicaly aggregated ending up totally at 20Gb/s respectively 40Gb/s.

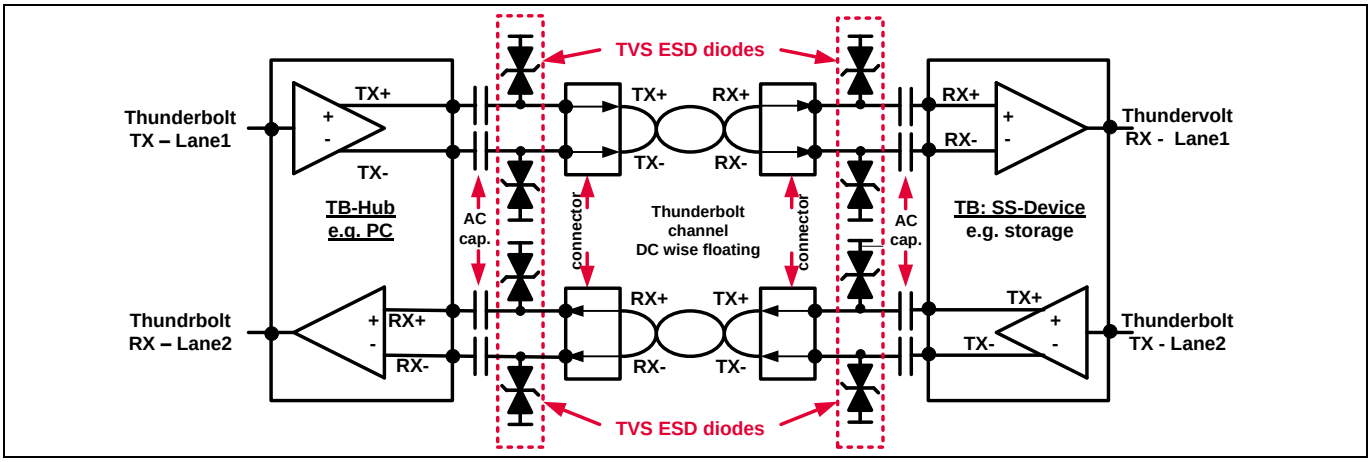


Figure 19 Thunderbolt signaling lanes for TX and RX (2 times per main link)

Following the recommendation for USB 3.x to place the ESD protection devices according to “case 2” , NO latch-up is possible because DC blocking capacitors are at both sides (source and sink) of the link. NO DC path between source and TVS or RX_bias to TVS is available. The only latch-up current is provided by the displacement / discharge current of the AC coupling capacitors.

Summary:

SCR based ESD protection devices are latch-up free for the Thunderbolt interface. TB is inherent latch-up save because the DC current is de-coupled from the TX PHY and the RX PHY (via AC coupling capacitors).

3.4 HDMI Version 1.3, 1.4 and 2.0 and DVI

HDMI and the DVI signal principle bases on TMDS (Transition-Minimized Differential Signaling) which is an application tailored version of LVDS (Low Voltage Differential Signaling). Latch-up scenario is checked for HDMI 1.3b [6]. In higher HDMI versions the principle is expected to be the same because of similar environment. For DVI, the signaling environment is the same. DVI and HDMI are treated in the same way regarding latch-up considerations.

HDMI (High-Definition Multimedia Interface) provides 3.4Gb/s per lane for Version 1.3b and 1.4. For Version 2.0 speed was upgraded to 6Gb/s per lane. DVI (Digital Visual Interface) is similar to HDMI 1.3b showing a data rate of 1.65Gb/s per lane respectively 3.4Gb/s per lane. Three lanes are used for data allways, the fourth is for the clock.

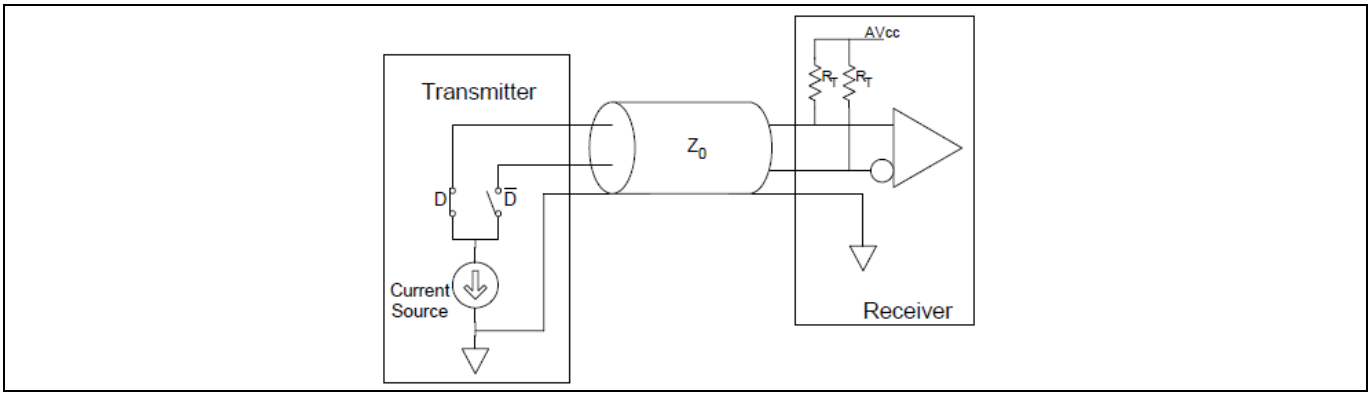


Figure 20 Principle structure of one TMDS line (w.o. Rsource)

Important for HDMI is the Vcc sourcing point, located at the sink (RX). In case of an unconnected HDMI link (NO HDMI cable between HDMI source (TX) and HDMI sink (RX)), latch-up can only occur at the sink side under the condition V_{dd} is in high state.

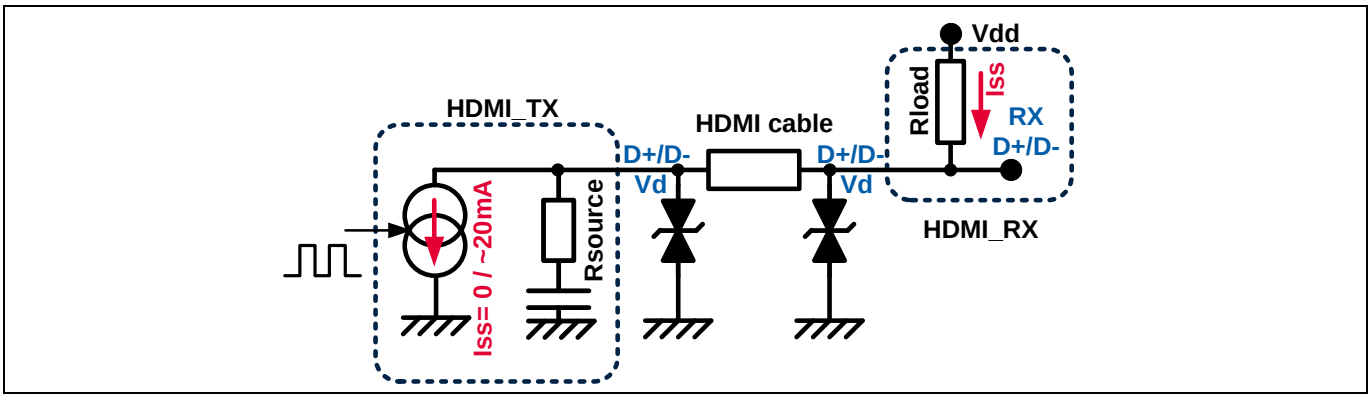


Figure 21 HDMI signaling on one line

According HDMI specification the environment is as follow:

- R_{source} [Ohm]: 45 min 55 max 45 wc (R_s is highly recom. for >1.65Gb/s)
- R_{load} [Ohm]: 45 min 55 max 45 wc
- V_{dd} [V]: 3.13 min 3.47 max ~3.5V wc
- I_{ss} [mA] 0 min 20mA 0 wc ($V_d = V_{dd}$)

To stay inherent latch-up save @ $V_{dd\text{-}max}$ = 3.5V:

$V_{hold\ SCR} > \sim 3.5V$ **OR** $I_{hold\ SCR} >= (V_{dd-max} - V_{hold\ SCR})/R_{s\ wc}$ **is required**

Example for $I_{hold\text{-}SCR}$ as a function of $V_{hold\text{-}SCR}$.

- $V_{hold\text{-}SCR}$ = 2V $I_{hold\text{-}SCR}$ >= (3.5V-2V)/36 Ohm =~42mA
- $V_{hold\text{-}SCR}$ = 1V $I_{hold\text{-}SCR}$ >= (3.5V-1V)/36 Ohm = ~70mA

Summary:

The HDMI and DVI link can be latch-up critical at sink side in combination with an SCR based ESD protection device. To avoid this problem a huge $I_{hold\text{-}SCR}$ or $V_{hold\text{-}SCR}$ is required. Therefore HDMI and DVI requires special SCR devices to overcome the potential latch-up problem, or $V_{hold\text{-}SCR}$ tailored "snap-back" TVS diodes .

3.5 DisplayPort (DP) interface

The DisplayPort (DP) is a very popular digital highspeed interface to connect the computer with the TFT monitor. DP is an alternative to HDMI, which is most popular for TV sets. [7]

Latch-up scenario is checked for DP1.1b. In higher DP versions the principle is expected to be the similar.

For the latch-up scenario evaluation following restrictions are imposed. The SCR based ESD protection device is placed as described in USB3.x "case 2" The TX ESD protection is places between capacitor "C_ML" and the DP source connector.

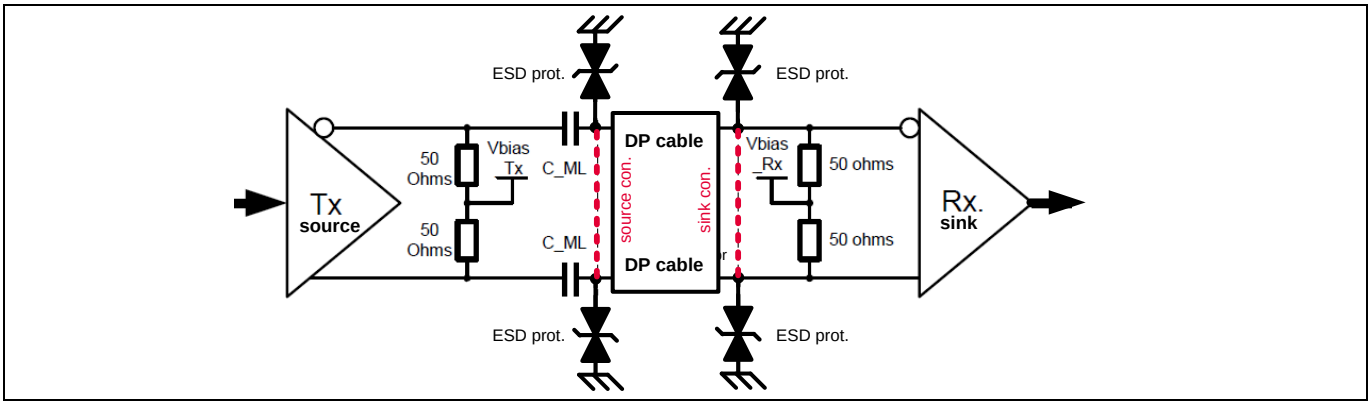


Figure 22 DiplayPort differential pair w. ESD protection (4 times per main link)

For the open DP link (no connection between source and sink via DP cable), there is NO latch-up possibility on AC coupled TX side. Only on RX side latch-up can happen if Vbias_Rx is on.). For closed DP link there is a latch-up potential for the RX side only, but TX ESD protection and RX ESD protection would be affected in this case too.

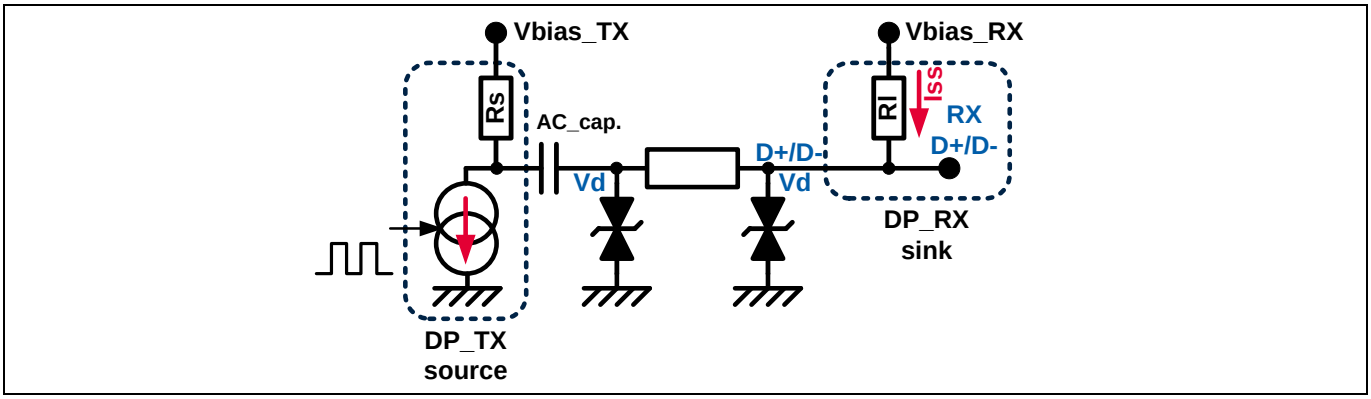


Figure 23 DisplayPort signaling on one line

According DP1.1a table 3-10 / 3-11 (DP main link RX parameters):

$V_{bias\_RX} = V_{bias\_TX}$: 0V…2V R_s = 50 Ohm

To stay inherent latchup save @ $V_{dd\text{-}max}$ = 3.5V:

$V_{hold\ SCR} > 2V$ **OR** $I_{hold\ SCR} >= (V_{bias\ RX} - V_{hold\ SCR})/R_s$ **is required**

Example for $I_{hold\text{-}SCR}$ as a fuction of $V_{hold\text{-}SCR}$.

- $V_{hold\text{-}SCR}$ = 1V $I_{hold\text{-}SCR}$ >= (2V-1V)/50 Ohm = 20mA

Summary:

The DiplayPort is inherent latch-up save or $V_{hold\text{-}SCR}$ = 2V OR an $I_{hold\text{-}SCR}$ >=20mA .

3.6 Conclusion

For ESD protection performance improvement (V_{clamp} reduction) latest ESD protection arebased on the SCR (Silicon Controlled Rectifier) structure. Typical SCR devices have a holding voltage ($V_{hold\text{-}SCR}$) lower than supply voltage or signal voltage. Therefore principle potential risk for latch-up is present. Various latch-up scenarios are checked for different applications. A procedure (load line analysis) is used to determine the potential of latch-up and to calculate required characteristics for the SCR based ESD protection devices to stay inherent latch-up free.

In general, the risk for a potential latch-up is **ONLY** present for HDMI. All other mentioned interfaces can collaborate with SCR based ESD protection devices providing an $V_{hold\text{-}SCR}$ of about 2V or more. For these applications the Infineon ESD131 / ESD132 is a perfect choise.

4 Authors

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5 Reference

[1] Infineon Application Note AN210

[2] Load Line Analysis

[3] Universal Serial Bus Revision 2.0 specification

[4] Universal Serial Bus Revision 3.1 Specification Chapter 6 Physical Layer (PHY)

[5] Chapter 6 Physical Layer (PHY)

[6] HDMI 1.3a (High-Definition Multimedia Interface) released by "HDMI.ORG" – Nov. 2006.

[7] DisplayPort Standard 1.1a, released by VESA (Video Electronic Standard Association) Jan. 2008

[8] Thunderbolt is the brand name of a hardware interface developed by Intel.

Revision History

Major changes since the last revision

Page or Reference	Description of change

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