Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

THIS SPEC IS OBSOLETE

Spec No: 001-52209

Spec Title: AN52209 - CY8CLED0XX0X POWERPSOC(R) - HARDWARE DESIGN GUIDELINES

Replaced by: NONE

AN52209

CY8CLED0xx0x PowerPSoC® – Hardware Design Guidelines

Doc. No. 001-52209 Rev. *G

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone (USA): 800.858.1810
Phone (Intnl): 408.943.2600
http://www.cypress.com

Copyrights

Contents

1. Introduction

The Cypress PSoC® family of devices is well established in the field of programmable mixed-signal microcontroller-based devices. The traditional method of implementing power management systems (for example, high-brightness LED lighting systems) involves using a similar system-on-chip to interface with high-power discrete devices, such as constant current drivers and MOSFET switches.

In PowerPSoC®, the classic PSoC core is combined with high-performance power electronics. This results in an integrated intelligent power electronics solution in a single QFN package. The intent of PowerPSoC is to significantly reduce the BOM cost, part count, and board space for implementing power management systems while retaining performance. CY8CLED04D01 family of devices combines up to four independent channels of constant current drivers.

The level of integration and versatility offered by PowerPSoC can lead to considerable simplification of design, thus allowing the designers who are less familiar with power electronics domain to venture into these designs. In order to avoid oversimplification and/or overlooking of certain fundamental system-level considerations, Cypress offers this document to address the following four key issues in any power conversion system design: thermal, layout, transient handling, and ESD. By gaining familiarity with the issues and employing suggested techniques and guidelines in these chapters, the designers will certainly improve the integrity of their designs and likelihood of first pass success.

1.1 Overview of Chapters

1.1.1 Basic Thermal Guidelines for using PowerPSoC®

Power conversion systems' inefficiencies or losses result in generation of heat within the system. The control and dissipation of this heat is an important system design criterion, commonly known as thermal management. As the power density of systems increase, the system designers need to pay more attention in managing heat dissipation from key portions of the system to maintain devices within their optimum operating temperatures. This chapter provides a thermal model for PowerPSoC and lists key considerations for achieving a robust thermal design.

By reading this chapter, you will be able to create a first pass thermal model of the intended system and ensure that the device junction temperature stays within desired limits through design of appropriate thermal paths on the printed circuit board (PCB).

1.1.2 PowerPSoC® PCB Design Guidelines for LED Driver Circuits

Realization of PCB designs using PowerPSoC requires adherence to certain guidelines for optimal performance and first pass success. In this chapter, systematic guidelines with design examples are provided for PCB design of LED driver circuits using PowerPSoC.

The guidelines cover three major areas: component placement choices, circuit board choices, and power/grounding layout choices. Illustrated examples are given for layout considerations for floating buck, floating buck-boost, and grounded boost LED drivers. In addition, important information regarding via usage, trace selection, and other PCB routing details are provided. For a beginner, it may be overwhelming to assimilate and follow all the guidelines at once. In such cases, it is essential that the grounding and trace selection guidelines are followed more closely.

1.1.3 Minimizing Power and Ground Transients in LED Driver Circuits

A high-brightness LED driver circuit has significant switching transients and current flow levels that can complicate the design. PowerPSoC simplifies many of these design aspects with its high integration of power components. This chapter provides guidelines for reducing transients in the power and ground domains, and the use of filtering components to optimize power supply design using PowerPSoC. Further, it describes how to select power supply decoupling capacitors and provides examples of minimum capacitance calculations based on system parameters. A section on the use of ferrite beads is also included.

This chapter contains detailed treatment of ground and power domains – definitions, recommendations, and examples. It alerts the designer that all **grounds** are not equal and careful identification of switching transients and their effects prior to layout prevents unwanted signal couplings. In addition, a set of examples are provided to illustrate the calculations of decoupling capacitors for various sections of the PowerPSoC application circuit. As illustrated, prevailing system requirements play a key role in the final determination of the decoupling capacitors.

1.1.4 System Level ESD Considerations for a PowerPSoC® Based LED Driver

This chapter highlights the ESD challenges in LED lighting systems with secondary side controllers and describes the design of PowerPSoC based products with robust system-level ESD performance. Protection is provided by including a few low-cost circuit components and by incorporating minor changes to the lighting fixture design.

While the focus of this compact chapter is on averting ESD events coming from the LED fixtures from impacting the PowerPSoC pins, the techniques described here are universally applicable. The key messages from this chapter are:

- Provide sufficient bypass paths for any external ESD or other transients so that they do not get to the vulnerable part of the system, i.e., PowerPSoC.
- Build sufficient protection at the CSP and CSN pins of the PowerPSoC in terms of bypass capacitors and TVS diodes as further precaution.

1.2 Guidelines on Prioritization (Trade-offs)

The chapters in this primer cover different aspects of board realization. It is natural and likely that during any specific circuit implementation, conflicts will arise between the guidelines from different chapters (or sometimes from within a chapter). As any engineering exercise involves making trade-offs, this should not be too surprising. Each application will have its own priorities and key requirements, so it is difficult to provide generalized guidelines. However, following points may help when you are trying to resolve the conflicts between guidelines (or prioritizing amongst them).

- Give primacy to thermal considerations – without stable thermal operation, system design is meaningless.
- If system requirements involve exposure to external (human or material) electrostatic impulses, then build in the protection described in the ESD chapter.
- When designing decoupling capacitance, err on the side of choosing higher value in a smaller package.
- For layout exercises, give primacy to using Star grounds and short traces for power nets.

2. Basic Thermal Guidelines for using PowerPSoC®

It is easier to model a thermal system by drawing analogy to an electrical system. In an electrical system, current flows through a path comprised of electrical resistance if there is a potential difference between two points. Similarly, in a thermal system, heat flows through a path comprised of thermal resistance if there is a temperature difference between two points.

From a semiconductor perspective, the goal of every thermal design is to keep the junction temperature well below the maximum datasheet specification. This can be achieved by optimizing the thermal path from the semiconductor junction to a thermal ground.

This document uses Cypress's PowerPSoC family of intelligent LED controllers to demonstrate the concepts with help of some examples. The PowerPSoC family, along with PSoC technology, features high-performance power electronics including 1 A, 2 MHz power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators. These features enable creation of intelligent power electronics solutions for LED power management with efficiencies greater than 90 percent.

This document covers the basic guidelines for a good thermal design. Although beyond the scope of this document, it is useful to note that intelligent thermal protection can be designed using the programmability available within PowerPSoC.

2.1 Thermal Theory

The design of a thermal system is usually governed by four factors – power dissipated by the devices, thermal resistance of the devices, thermal resistance of the heat sinking mechanism, and ambient temperature. Except for thermal resistance of the device, the designer has control over the other factors. Although different applications have a different balance of these factors, the goal is always the same – to minimize the junction temperature of critical devices. Critical devices are devices operating close to their rated power dissipation.

2.1.1 Thermal Resistance

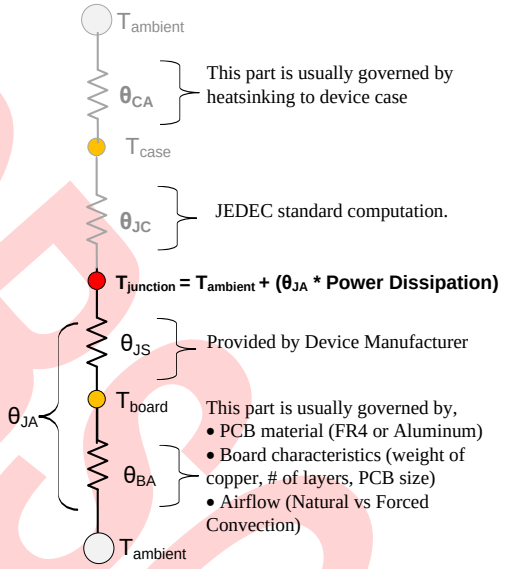
Similar to electrical systems where resistances impede current flow, a thermal system consists of thermal resistances that impede heat flow. Thermal resistance is usually specified in °C/W. The most common parameters found in power semiconductor manufacturer datasheets are -

- thermal resistance from device junction to ambient (θ_{JA}) and
- thermal resistance from device junction to device case (θ_{JC}).

Less common, but increasingly specified is the thermal resistance from device junction to solder (θ_{JS}) ('s' refers to the solder that connects the device thermal pad to the board), which is important for devices with a solderable thermal attachment and is becoming more prevalent in high-density designs.

Thermal resistances are shown in Figure 2-1. θ_{BA} and $\theta_{CA,}$ which are thermal resistances from board-to-ambient and device case-to-ambient, are also shown. In PowerPSoC, almost 96 percent of the total heat is transferred through the bottom thermal pad. Therefore, θ_{JA} is dictated by θ_{JS} and θ_{BA} and its θ_{JC} and θ_{CA} components are not considered.

Figure 2-1. Thermal Resistance Network



2.1.2 Heat Transfer

Unlike electrical flow, which is always conductive, heat transfer can take place in any of the following three modes.

2.1.2.1 Conduction

This mode of heat transfer occurs due to direct contact between two solid surfaces. Conductive heat transfer usually depends on geometry, type, thickness, and area of heat flow. Air has the lowest thermal conductivity. Hence, a copper or aluminum surface is usually required to accelerate heat removal from the device junction.

2.1.2.2 Convection

This mode of heat transfer occurs due to the movement of fluids (liquid or gas) past a solid surface, which is at a temperature different from the fluid. Convective heat transfer usually depends on type, area, and amount of fluid flow. It is also possible to create forced convection (using fans) that increases the rate of fluid flow. However, due to cost and other complexities, natural convection is the preferred method in many high-density systems.

2.1.2.3 Radiation

This mode of heat transfer occurs by electromagnetic waves through empty space. Radiated heat transfer usually depends on surface temperature, surface emissivity, and surrounding temperature.

2.1.3 Power Dissipation

The source of heat in a power device is the **power dissipation** of the device. Power dissipation is the sum of all the losses in the device. As seen in Equation 1, junction temperature is a function of power dissipation.

$$T_{junction} = T_{ambient} + PD * (\theta_{JA})$$ Equation 1

Where:

$T_{junction}$ denotes junction temperature of the device in °C.

$T_{ambient}$ denotes ambient temperature of the system in °C.

PD denotes power dissipation of the device in W.

θ_{JA} denotes thermal resistance from the device junction to ambient in ºC/W.

Another method of computing the junction temperature is shown in Equation 2 and Equation 3.

$$T_{junction} = T_{board} + PD * (\theta_{JS})$$ Equation 2

$$T_{board} = T_{ambient} + PD * (\theta_{BA})$$ Equation 3

Where:

T_{board} denotes PCB temperature at a point on the top PCB layer below the PowerPSoC.

Θ_{JS} denotes thermal resistance from device junction to thermal pad

θ_{BA} denotes thermal resistance from board to ambient.

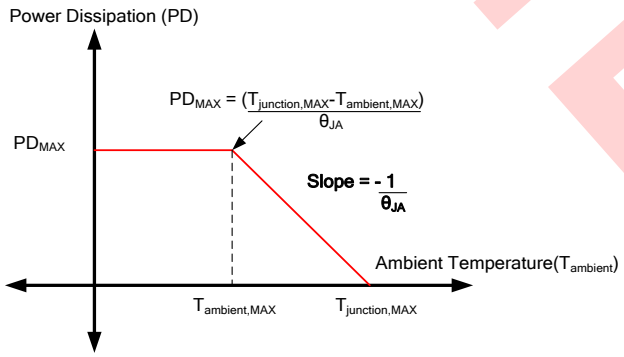
2.1.4 Ambient Temperature

Ambient temperature or surrounding temperature affects the maximum junction temperature. The maximum ambient temperature value from the device datasheet can be used along with thermal resistance θ_{JA} to de-rate the maximum power dissipation above maximum ambient, as shown in Figure 2-2.

Consider the following example to understand the relationship between ambient temperature and power dissipation.

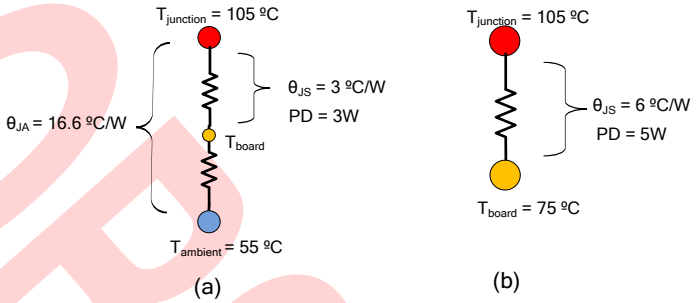
In Figure 2-3 (a), θ_{JA} is 16.6 °C/W, $T_{ambient}$ is 55 °C, and power dissipation is 3 W. However, the board temperature T_{board} is not specified. In Figure 2-3 (b), θ_{JS} is 6 °C/W, T_{board} is 75 °C, and power dissipation is 5 W; $T_{ambient}$ however, is not specified. In both cases, the junction temperature is maintained at 105 °C.

Figure 2-2. Maximum Power Dissipation De-rating



Thermal resistances may be specified on the datasheet in one or both ways, shown in Figure 2-3. However, it is often unclear whether a particular thermal resistance should be used for $T_{junction}$ estimation. It is also unclear whether temperature should be measured at ambient, case, or board. The answer lies in determining path of least thermal resistance and deriving temperature drops along that path.

Figure 2-3. Example Datasheet Specifications



For PowerPSoC, θ_{JS} should be considered for $T_{junction}$ estimation. PowerPSoC is designed to dissipate almost 96 percent of the heat through the exposed thermal pad (integrated into the device package) to the PCB.

Comparing Figure 2-3 (a) and Figure 2-3 (b), it can be seen that the T_{board} is 96 °C (based on application of Equation 2,) for Figure 2-3 (a), while it is 75 °C for Figure 2-3 (b). This is despite lower values of θ_{JS} and PD for the Figure 2-3 (a) scenario – indicating that the board layout and thermal management in Figure 2-3 (b) is good enough to keep the board temperature at 75 °C. For Figure 2-3 (a), it is not possible to dissipate 5 W through a system while retaining the junction at 105 °C. Either θ_{JA} or $T_{ambient}$ needs to be changed. In most cases it is easier to reduce θ_{JA} by modifying the board design – for instance, using more copper or aluminum.

If it is not possible to change θ_{JA} or $T_{ambient,}$ then power dissipation must be de-rated using θ_{JA} as illustrated in Figure 2-2.

2.2 PowerPSoC Thermal Model

Typically, the majority of heat transfer in a PowerPSoC dc-dc Converter PCB is in the form of conduction. There is also a small amount in the form of convection and radiation. Using a regular PCB to model thermal resistances (as shown in Figure 2-1) is complex because a number of factors affect heat flow. Some of these factors are:

- Power dissipation
- Air velocity and direction
- PCB orientation, size, component density, and mounting
- Copper thickness, number of copper layers
- Die size
- Environment (ambient temperature)

This dependence on various factors leads to variation in specifications and test methodologies among manufacturers. The Joint Electron Device Engineering Council (JEDEC) has standardized the test procedure[1].

The thermal model for Cypress's PowerPSoC family was simulated using a JESD51-7 standard FR4 PCB with four metal layers, 2 oz copper weight on outer layers, and 1 oz on inner layers. Thermal via array below the device is laid out according to package manufacturers' recommendations[2]. The simulation results are shown in Table 2-1.

Table 2-1. Thermal Resistances for PowerPSoC

Package	Body Size	Air Flow	Θ_{JA}	Θ_{JC}	Θ_{JS}
QFN-56	8 mm x 8 mm (1 mm thick)	0 m/sec	16.6 °C/W	Not Applicable	2 °C/W

In Table 2-1:

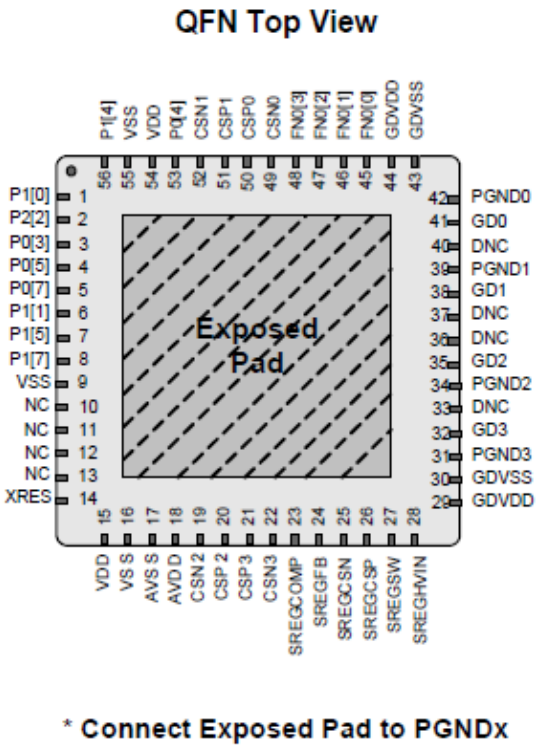
θ_{JA} denotes thermal resistance from device junction to ambient. It depends on the package, board, airflow, radiation, and system characteristics. Typically, effects of radiation are negligible.

Note The PowerPSoC family datasheet lists a value for natural convection only (no forced air).

θ_{JC} denotes thermal resistance from device junction to device case. Case is specified at a point on the outer surface of the package. It depends on package design and materials used. In the absence of a heat sink to case, a very small percentage of the heat dissipates through the top surface of the package. Hence, θ_{JC} is not relevant for PowerPSoC based systems because the PCB is used as a heat sink to dissipate heat through the exposed thermal pad.

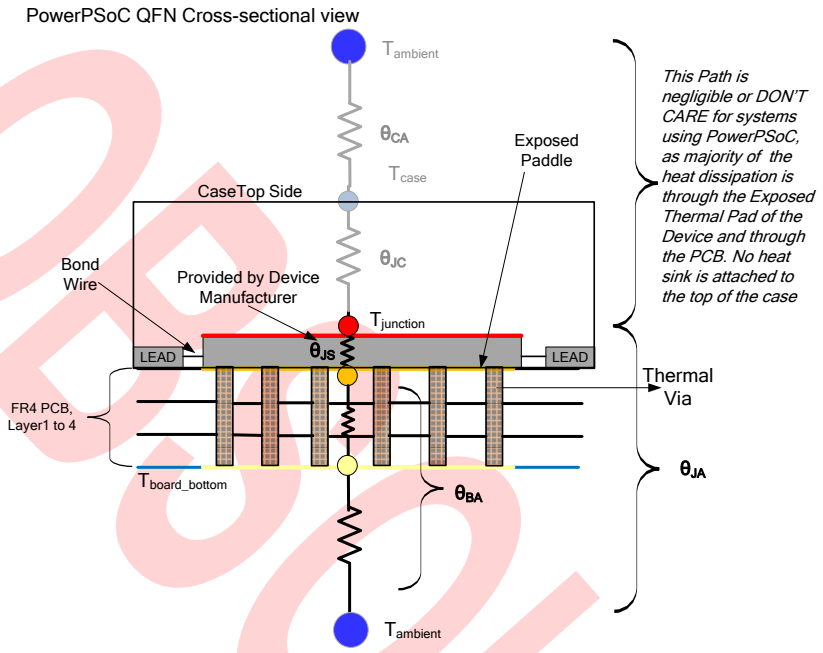
θ_{JS} denotes thermal resistance from device junction to solder, which connects the device thermal pad (as shown in Figure 2-4) to the board. This parameter includes thermal resistance from PowerPSoC's junction to a reference point on the bottom of the package through a solder point to the board under the package. θ_{JS} parameter is important for devices in leadless packages that have a thermal attachment mechanism.

Figure 2-4. PowerPSoC Thermal Pad



The PowerPSoC thermal model is shown in Figure 2-5.

Figure 2-5. PowerPSoC Thermal Model

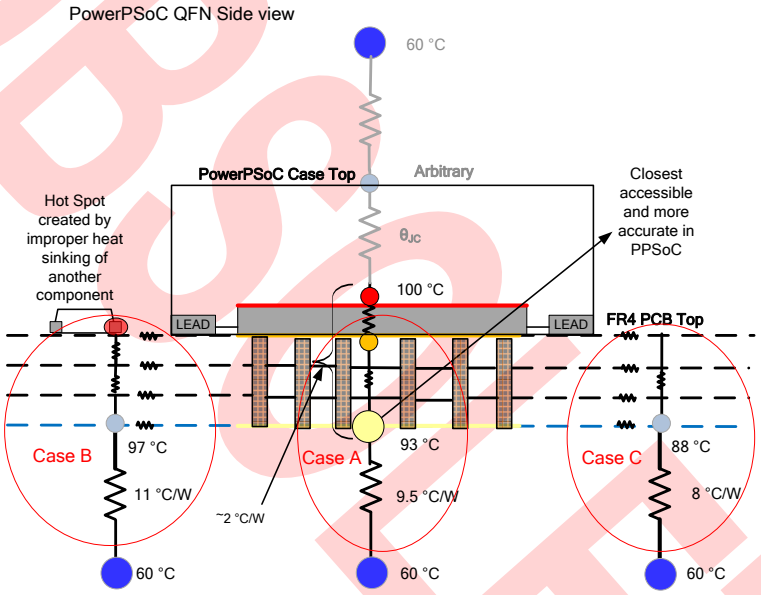


2.2.1 Accurately Estimating $T_{junction}$

$T_{junction}$ can be accurately estimated if an appropriate measurement point on the board is chosen. If valid thermal resistances and board effects are not accounted for, the measurement will be erroneous. Consider the following example to understand how to make an accurate $T_{junction}$ measurement.

For this example, θ_{JS} is equal to 2 °C/W (neglect thermal resistance through the thermal via array for this example); PD is 3.5 W. The intent is to retain $T_{junction}$ at 100 °C at a $T_{ambient}$ of 60 °C. θ_{BA} varies when measured across different points, as shown in Figure 2-6. Using Equation 2 and Equation 3, $T_{junction}$ and T_{board_bottom} across the different points can be computed. T_{board_bottom} is the board temperature at a point on the bottom layer of the board just below the PowerPSoC.

Figure 2-6. Accurate θ_{JS} Estimation



As seen, every point can be at a different temperature depending on factors such as board design, airflow, component orientation, and hot spots created by another component in the proximity of the measurement point. In Case B, a hot spot created by another component increases the bottom layer board temperature. In Case C, the bottom layer board temperature measured away from the device is lower due to the effect of board spreading resistance. Power conversion systems have other power components (power rectifiers, inductors, and so on) that produce a fair amount of heat. If the measurement is not made at the appropriate point, interaction between multiple heat sources can lead to measurement errors. Therefore, when measuring junction temperature for PowerPSoC, the point at which the reading is most accurate is Case A (marked with a yellow circle). This point is on the bottom layer of the PCB that is connected to the PowerPSoC's exposed paddle through an array of thermal vias. Thermal vias offer very low thermal resistance.

Note The procedure to calculate thermal resistance of the thermal via array is outlined in the Illustrated Step-by-step Thermal Calculations section.

It can be inferred that θ_{JS}, bottom layer board temperature, and resistance of the thermal via array are the key considerations when computing junction temperature for PowerPSoC.

2.3 Thermal Considerations

Historically, thermal design is meant for finding out which of the components in the system generated the most heat and also coupling them to a heat sink. However, with power systems shrinking in size and becoming more cost sensitive, heat sinks have become a less attractive option. There is a need to use the PCB as a heat sink. Heat transfer through the PCB, similar to any other heat sink, is primarily in the form of conduction along the surface, and secondarily through convection and lastly through radiation to the ambient.

PowerPSoC is packaged in a QFN package with an integrated thermal pad on the bottom. The thermal pad provides a very low thermal-resistance path to conduct heat out of the device. Without this thermal pad, the thermal impedance of the package would be quite high and it would be unable to handle the power dissipation normally associated with its functioning. The heat is conducted to the structure that is attached to thermal pad. Typically, the pad connects to a copper landing on the PCB through a solder joint, effectively turning the PCB into a heat sink. In PowerPSoC, thermal pad is also electrically connected to power ground. (Refer to the PowerPSoC family datasheet for details on electrical specifications.)

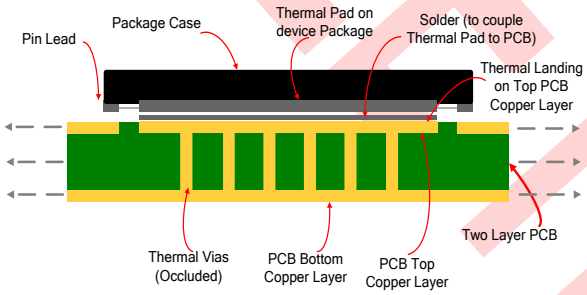
It is important to ensure that the device is both thermally and electrically coupled to the PCB for optimum performance and system reliability. Not only does the heat need to conduct through the PCB, it must also effectively transfer into the surroundings as well as away from the device. Hence, it is critical to ensure robust thermal pad and PCB design. One challenge that immediately presents itself is that it is difficult (nearly impossible) to spread the heat on the top layer where the thermal pad is attached to the PCB. Thermal pad is completely surrounded by device pins, which have electrical connectivity requirements on the same layer. As a result, it is imperative to use the array of vias as depicted in the following section.

Note For designs using the PowerPSoC gate drivers to drive external MOSFETs, the heat generation primarily shifts to the external MOSFETs. Hence, guidelines recommended for MOSFET thermal landing layout should be considered while laying out the circuits.

2.4 Thermal System[3, 4]

- The QFN device and the surrounding PCB area under the package is essentially the “thermal system”, which optimizes heat conduction as shown in Figure 2-7.

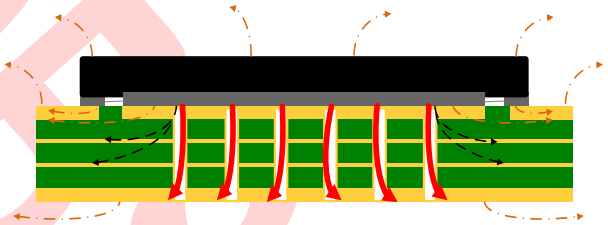
Figure 2-7. Thermal System Cross-sectional View



- The system consists of the exposed thermal pad integrated on the bottom of the QFN package, a thermal landing on the PCB top layer, an array of vias designed to effectively transfer heat from the top to the bottom layer of the PCB, and a layer of solder paste (interface material) is used to couple the pad to the landing.

- Heat flow paths can be thought of as lumped heat flow paths as shown in Figure 2-8. Although this is not an accurate model for heat flow, it emphasizes the fact that most of the heat is conducted through the via array into the PCB.
- The goal of a good thermal design should be to optimize the various heat flow paths:
  - Heat flow through the thermal vias
  - Heat flow through PCB area surrounding the device
  - Heat flow into the ambient or system enclosure

Figure 2-8. Heat Flow Paths



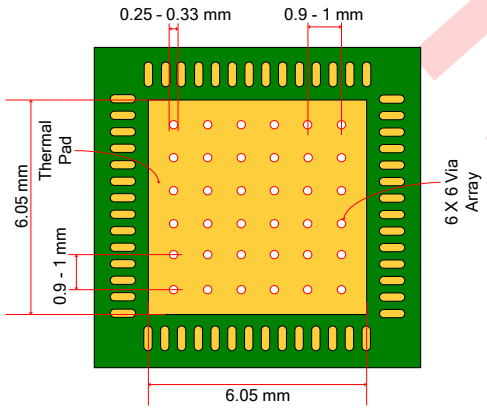
2.5 Optimizing Heat Flow Paths

2.5.1 Heat Flow through Thermal Vias[2, 4]

Layout the thermal landing carefully, because it is part of the most critical path for heat conduction. Here are guidelines for a good thermal landing layout.

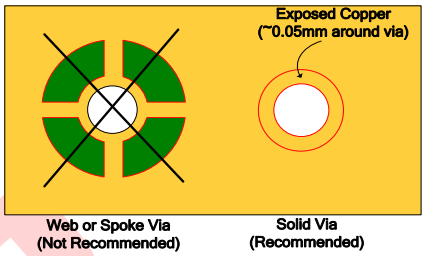
- Size of thermal landing on top layer of the PCB should be 6.05 mm x 6.05 mm. A similar copper pour should also be on the bottom layer, which should ideally extend into a large copper plane without any cuts or breaks.
- Copper thickness of 35 micron (1 oz. copper clad) is recommended when device dissipation is below 3 W, and 70 micron for higher dissipation levels.
- A 6 x 6 via array (36 vias in total) should be used, as shown in Figure 2-9.
- The optimum number of vias recommended to achieve good thermal performance is 36.
- Via diameter: 0.25 to 0.33 mm (to minimize solder wicking); spacing between adjoining via centers: 0.9 to 1.0 mm as shown in Figure 2-9.

Figure 2-9. PowerPSoC Landing Pattern



- No thermal relief (web or spoke connections) on vias. There should be a continuous copper ring around the vias as shown in Figure 2-10.

Figure 2-10. Thermal Via



- Do not completely cover vias with solder mask as it can lead to excessive voiding.
- Vias should be internally plated with copper and filled with solder to avoid wicking. They may be filled with thermally conductive materials such as copper and silver epoxy to further improve thermal conductivity. Details on via filling are discussed later.

2.5.2 Heat Flow through PCB Area Surrounding the Device[2, 3]

Heat conduction through the top copper plane is compromised by signal routing.

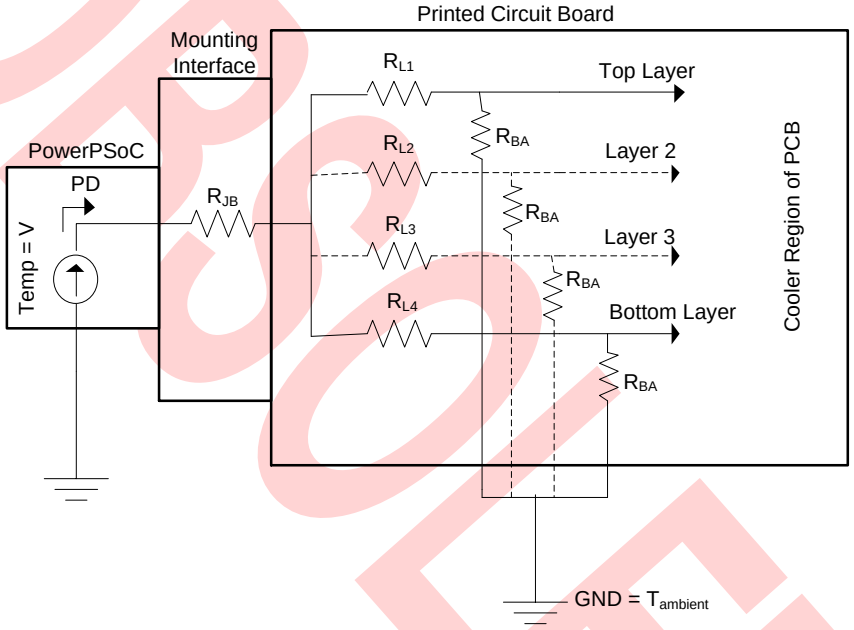
Thermal conductivity of the plane can be improved by filling unused PCB areas surrounding the device with copper. Note that copper pours should connect to appropriate electrical connections.

The thermal landing on top layer of the PCB should be connected to power ground copper pours to improve heat conductivity and satisfy electrical specifications for PowerPSoC. Further, thermal landing must be connected to power ground copper pours, if possible, on all inner and outer layers to maximize heat conduction through the PCB – this is illustrated in Figure 2-14.

2.5.3 Heat Flow into the Ambient or System Enclosure

Effectively removing heat away from the device and into the ambient or system enclosure is dictated by PCB construction. The number of PCB layers, weight of copper on each layer, trace width, trace length, and trace and component placement plays an important role due to their influence on heat flow through the PCB. Figure 2-11 shows an electrical analogy for a thermal system. Power dissipated in the device can be modeled as a current source and temperature as an electrical voltage. The thermal resistances are modeled as resistors and the circuit can be solved for voltages that are analogous to temperatures. If the system is enclosed, thermally coupling the PCB to the enclosure maximizes heat transfer. Each of these PCB design criteria are discussed in detail.

Figure 2-11. Electrical Analogy for a Thermal System



2.5.3.1 Number of PCB Layers

Increasing copper layers in a PCB improves conductivity. There can be as much as a 20 °C reduction in $T_{junction}$ when layers are increased from two to four[4]. However, it should be recognized that the capability of inner layers to disperse heat is limited and adequate number of thermal vias have to be added to bring the heat out to outer layers.

Recommendation: For systems with total PowerPSoC dissipation greater than 5 W, use four layers. If having four layers is not an option, other cooling techniques may have to be explored.

Hint: A PowerPSoC based system driving four channels with six 700 mA white LEDs each and a chip efficiency of 93 percent, dissipates approximately 5 W assuming a floating load buck topology with an operating switching frequency slightly under 2 MHz and conduction duty cycle of 75 percent.

2.5.3.2 Copper Thickness

This denotes the copper thickness for PCB layers. Increasing the thickness lowers the thermal resistance. For cost sensitive designs, increasing copper thickness may be a good alternative for increasing the number of layers to optimize thermal performance.

Recommendation: Use 2 oz copper plating for outer layers in designs with total PD greater than 3 W.

2.5.3.3 PCB Size[5]

Large boards have greater thermal mass. Recall that heat travels from the device to the PCB and then laterally conducts through the PCB surfaces. We can estimate a first pass lateral conductivity for a given PCB size by performing a few simplified calculations.

Consider a 2" x 2" (50.8 mm x 50.8 mm) board, 2 layers with 100% copper coverage, 2 oz copper per layer (layer thickness 0.071 mm = t_{top_plane} = t_{bottom_plane}), both layers are at the same temperature, majority heat transfer is in the form of conduction, conductivity of copper is 0.386 W/mm°C (= k_{top_plane} = k_{bottom_plane}), conductivity of epoxy material is 0.00025 W/mm°C (=k_{epoxy}), board thickness of 1.52 mm gives epoxy thickness of 1.38 mm (=t_{epoxy}), T_{board} is 85 °C, and the required $T_{ambient}$ is 60 °C. The conduction is along the PCB surface as shown in Figure 2-12. Using one dimensional equations for conduction:

$$\theta_{PCB} = \left(\frac{L}{k_{eff} A} \right)$$ Equation 4

Where:

θ_{PCB} = the lumped 1D lateral resistance of the PCB surfaces.

k_{eff} = the effective thermal conductivity of the medium (PCB in this case).

A = the surface area of the medium normal to the direction of heat transfer. In our case, it is the product of length and PCB thickness.

L = the thickness of the medium.

Assuming heat flow through the PCB as one dimensional and disregarding heat flow from the side surfaces (shown in Figure 2-12), the effective thermal conductivity can be calculated as follows:

$$k_{eff} = \frac{(kt)_{epoxy} + (kt)_{top\_plane} + (kt)_{bottom\_plane}}{t_{PCB}}$$ Equation 5

Where:

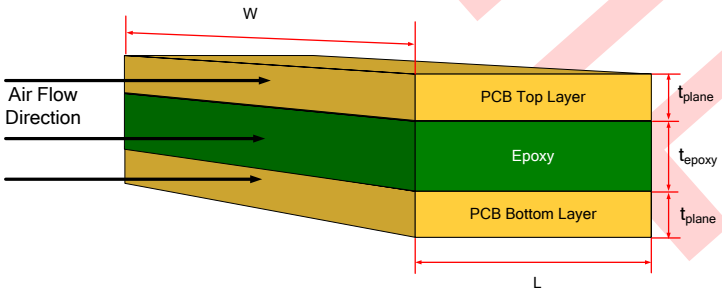
k_{epoxy}, k_{top_plane}, and k_{bottom_plane} denote thermal conductivity for epoxy and copper planes.

t_{epoxy}, t_{top_plane}, and t_{bottom_plane} denote thickness for epoxy and copper planes.

t_{PCB} denotes overall thickness of the PCB.

Therefore, k_{eff} = 0.036 W/mm°C

Figure 2-12. Heat Conduction through PCB Surface



Now we can calculate θ_{PCB} as follows:

$$\theta_{PCB} = \left(\frac{L}{k_{eff} * t_{PCB} * W} \right)$$ Equation 6

Hence θ_{PCB} = 18.30 °C/W

Using Equation 3 with a board temperature of 85 °C and ambient of 60 °C, the 2” x 2” board can dissipate 1.37 W of power. Note that assumptions made in this example are highly simplified. This calculation is used to get a first pass estimation of conductive cooling that a particular board size can provide for a given temperature rise. The equations can be modified depending on the amount of copper (% copper) for each board layer.

For example, adding two inner layers of 1-oz copper reduces the θ_{PCB} value to 12 °C/W and leads to 50 percent increase in power dissipation for the same area. If accurate modeling is required (considering the effects of traces and breaks in a continuous plane), it is recommended to simulate the system’s thermal behavior using one of the many available CFD thermal analysis tools.

Recommendation: It is good practice to perform a first pass PCB thermal estimation in the initial design stages of the system.

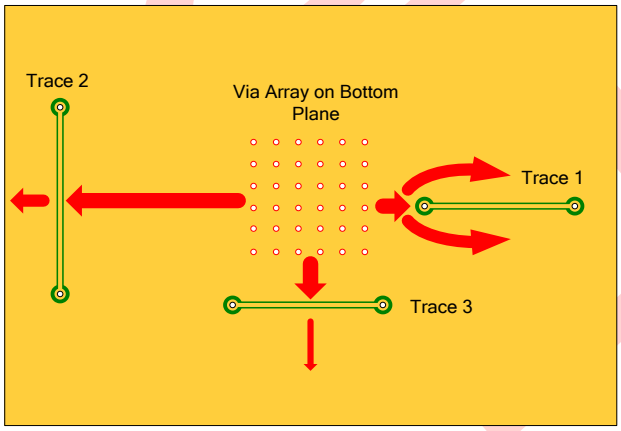
2.5.3.4 Placement of PCB Traces[4]

As shown in Figure 2-13, there are three ways to route traces on PCB layers. Placing traces close to the device must be minimized as they increase the thermal resistance and restrict heat flow away from the device. Avoid having traces on a layer that is used as a thermal plane for heat removal. If there is no option but to route on a thermal plane consider the following. Trace 3 runs parallel to the device and close to the device. So, Trace 3 significantly restricts heat flow (shown by red arrows) as it cuts the copper plane along the device periphery; Trace 2 on the other hand, being far away from the device, has a lower impact on heat flow. Trace 1 is the best option, because it cuts the plane in a perpendicular fashion with respect to the device; hence the impact on heat flow is minimal.

Note Although Trace 1 is the best routing option, placing multiple Trace 1s in parallel will have a significant negative impact on heat flow.

Recommendation: Avoid routing traces on the thermal layer. If unavoidable, use Trace 1 as an example for routing.

Figure 2-13. PCB Trace Placement



2.5.3.5 Placement of Other Components

It is important to note that placing components close to the device not only restricts heat flow but can also create hot spots, if the component itself produces a fair amount of heat.

A topic not covered in detail in this chapter is the effects of other heat sources in various power system PCBs. It is assumed that the PCB contains only the dc-dc conversion circuitry with PowerPSoC as the primary power dissipating component. For systems that have, for instance, the ac-dc system or LED loads integrated onto the same PCB, PowerPSoC may no longer be the focus of the thermal design. Large LED loads, for instance, produce a lot of heat and therefore become the focus of thermal design. In cases where LEDs are the focus of thermal design, it is good practice to thermally couple the thermal pad of PowerPSoC to the heat sink used for the LEDs. However, ensure that there is electrical isolation.

Note Although it is recommended that other components should not be placed close to the device, there may be critical components that cannot be placed far away from the device due to electrical considerations. For example, in a dc-dc converter system the switching diode and inductor cannot be placed far away from the PowerPSoC device to optimize the high current loops. The system design must consider effects of all components on overall thermal performance.

Recommendation: Do not place components close to the device unless unavoidable. If unavoidable, carefully consider the effects of these components in your thermal analysis.

2.5.3.6 Trace Length and Width

To effectively lower temperatures, longest and widest possible traces should be used. This facilitates maximum heat transfer away from the device. Again, it may not be possible to increase lengths for traces that connect critical components, due to electrical considerations. For example, the high current loops in a dc-dc converter cannot have long traces and should be routed using traces as short as possible. One way to improve thermal performance for this scenario is to make the traces wider.

Recommendation: Use long and wide traces whenever possible.

2.5.3.7 Board Geometry and Aspect Ratio

Generally board geometries and aspect ratios are governed by system level and structural constraints. However, uniform geometries and aspect ratios enable effective electrical and thermal layouts facilitating optimum component placement.

For example, a 4” x 4” square PCB has better thermal performance when compared to a 1” x 16” PCB having the same surface area, assuming the heat source is at the center of the board.

Recommendation: Use uniform geometries and aspect ratios whenever possible.

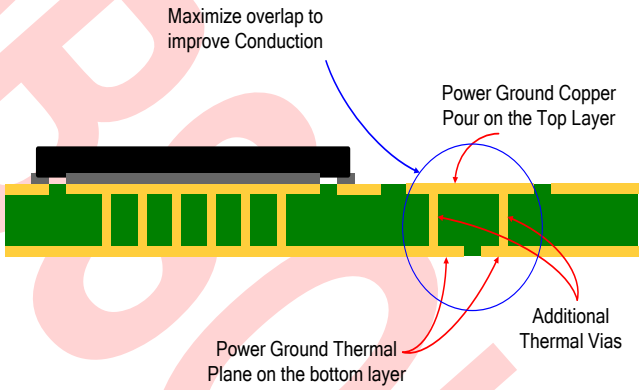
2.5.3.8 Use of Additional Thermal Vias

Thermal vias, similar to the ones used for the thermal landing, can be used to connect internal and/or external thermal planes whenever electrically possible. This helps maximize the continuous copper plane area for heat conduction. Whenever possible, the overlap between planes should be maximized as shown in Figure 2-14.

Note Placing too many vias can hurt thermal performance because it depletes the continuous plane and may cause mechanical instability.

Recommendation: Use optimum number of vias to connect thermal planes and maximize overlap between thermal planes.

Figure 2-14. Additional Thermal Vias



2.5.3.9 Use of Thermal Isolation Cuts [3]

Sometimes the overall performance of the PCB can be enhanced by carefully placing isolation cuts in the PCB to segregate components that can afford to run at higher temperatures. A component rated at a high temperature and dumping a lot of heat into the PCB can be isolated such that its heat does not affect other components that cannot tolerate high temperatures. Also, careful placement of components depending on the air flow direction can be made such that heat generating components are not placed upstream of other components.

Recommendation: These are advance techniques and should be carefully considered on a case-by-case basis. For thermally sensitive designs, a detailed thermal simulation should be performed.

2.5.3.10 Effectively Coupling PCB to System Enclosure[3]

When the PCB is thermally saturated and the component temperatures are still too high, at the maximum obtainable system air velocity, other means of conducting heat from the PCB to even larger area system structures are required. The chassis or enclosure of the system, often the largest surface area structure in the system, is usually exposed to the ambient air. It often makes a good sink for heat that cannot be dissipated by the PCB alone. Mechanisms to conduct heat into the chassis or enclosure include chassis screws, gap fillers, connectors, and side rails.

Recommendation: Always try and thermally couple the PCB to the system chassis or enclosure to maximize heat conduction to the ambient.

2.6 Key PCB Manufacturing Considerations from a Thermal Standpoint[2, 4]

2.6.1 Solder Mask

All copper areas should be covered by solder mask (to avoid electrical hazards), except:

- Thermal landing used to mount the device on the board
- Thermal copper pour on the bottom plane if an external heat sink needs to be attached
- Any copper required to couple the PCB to the system enclosure.

Opening solder masks may improve thermal performance, but safety considerations should take priority.

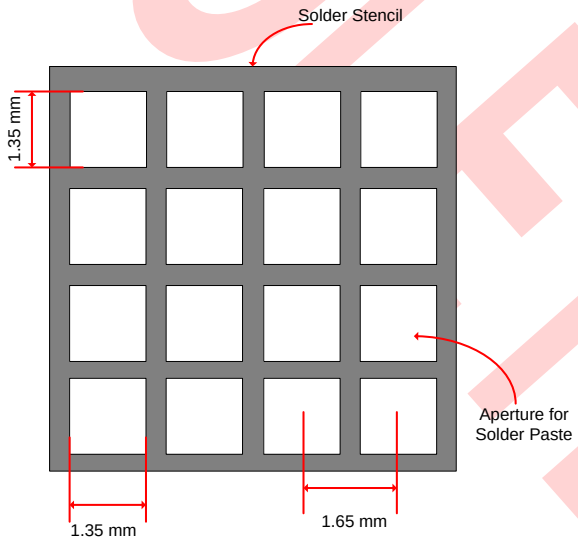
2.6.2 Thermal Pad Connectivity

To ensure that heat is effectively removed from the package and to have a reliable electrical connection, the thermal pad must be soldered to the thermal landing. The amount of solder paste must be carefully controlled as less paste leads to voiding and more paste leads to the component floating in a pool of solder, causing bad pin to pad connectivity.

It is therefore recommended that a solder stencil with smaller multiple openings be used instead of one big opening. This results in 50 percent to 80 percent coverage. However, it is better to have about 75 percent coverage.

Figure 2-15 shows an example stencil with approximately 80 percent solder coverage. Area of the stencil matches the thermal pad area. It is good practice to X-RAY a few boards initially, to ensure the manufacturing process results in minimum voids at the interface junction between the PowerPSoC and the PCB.

Figure 2-15. Example Solder Stencil



Coverage: 80%

2.6.3 Thermal Via Fill Material

Thermal vias plated with copper must be filled with solder because it minimizes wicking and improves conductivity. If further reduction in thermal resistance is required, vias can be filled with copper or any of the thermally conductive materials available. Filling vias however, is expensive and is only recommended for highly sensitive designs where the added cost is bearable.

2.7 Illustrated Step-by-step Thermal Calculations

Consider a dc-dc LED driver system rated to deliver a maximum power of 20 W to the load. dc-dc switching power converters have conversion efficiencies above 90 percent; however, let us consider a conservative system efficiency of 85 percent. This results in a worst-case power dissipation of approximately 3.53 W. Depending on the choice of external components (low dissipation), switching frequency (high), and operating conditions (high duty ratio), there is a possibility that 90 percent of the total system power loss could happen in the PowerPSoC device alone. Hence, the worst-case power loss for PowerPSoC is 3.2 W.

As shown in Figure 2-1, the primary heat transfer path for the PowerPSoC is through the thermal vias and eventually through the PCB into the surroundings by means of conduction, convection, and radiation. This path primarily constitutes two thermal resistances: θ_{JS} and θ_{BA}. θ_{JS} is specified as 2 °C/W for PowerPSoC. θ_{BA} is a complex resistor because it depends on various PCB design characteristics as discussed earlier. The system designer has control over this resistance and to optimize heat transfer, this resistance must be optimized.

As shown in Figure 2-16, θ_{BA} is further broken up into four lumped resistors (for simplicity):

$$\theta_{BA} = \theta_{BB'} + \theta_{cond} + (\theta_{conv} // \theta_{rad}) \qquad \text{Equation 7}$$

Where:

$\theta_{BB'}$ = Thermal resistance of the thermal via array along the thickness of the board (B-B').

θ_{cond} = Lumped resistance of the PCB along the surfaces. This governs lateral heat conduction through the PCB.

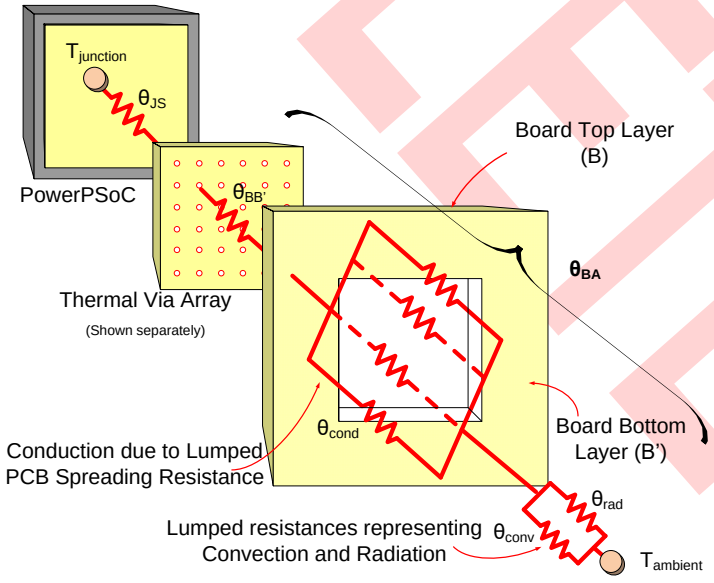
Note The value of this resistor is optimistic because it is based on simplified assumptions. PCB spreading resistance effects and effects of traces are not considered.

θ_{conv} = Lumped thermal resistance due to natural convection of heat from the PCB to the ambient.

θ_{rad} = Lumped thermal resistance due to radiation of heat from the PCB to the ambient.

The last two resistances act as parallel paths for heat dissipation, with convection path as the more dominant path.

Figure 2-16. Primary Heat Transfer Path

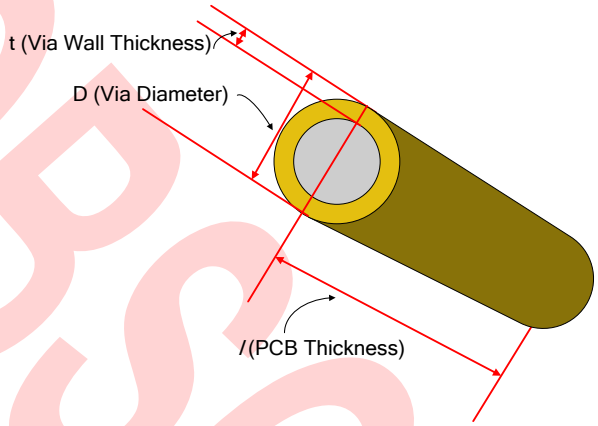


The steps to calculate each part of θ_{BA} follows:

Step 1: Calculating $\theta_{BB'}$

For PowerPSoC, it is recommended to have 36 thermal vias with diameter of ~0.25 mm. Via length is the same as the PCB thickness of 1.52 mm. Assume the via is plated to 1 oz copper (thickness: 0.036 mm) and internally filled with solder.

Figure 2-17. Thermal Via Dimensions



Using thermal conductivity for copper of 0.386 W/mm°C and 0.050 W/mm°C for solder. The thermal resistance of a single via is calculated as follows:

$$\theta_{VIA,solder} = \left(\frac{l}{k_{solder} * \Pi * \left(\frac{D - 2*t}{2} \right)^2} \right)$$

Equation 8

$$\theta_{VIA,wall} = \left(\frac{l}{k_{cu} * \Pi * \left(\left(\frac{D}{2} \right)^2 - \left(\frac{D - 2*t}{2} \right)^2 \right)} \right)$$

Equation 9

$$\theta_{VIA} = \theta_{VIA,solder} \,||\, \theta_{VIA,wall}$$

Equation 10

Where:

$\theta_{VIA,wall}$ = thermal resistance of the via wall.

$\theta_{VIA,solder}$ = thermal resistance of solder fill in the via.

θ_{VIA} = thermal resistance of a single copper plated, solder filled via.

k_{cu} and k_{solder} = thermal conductivity for copper and solder.

Other variables, as described in Figure 2-17.

Using Equations 8, 9, and 10, θ_{VIA} is 143.5 °C/W. Note that this figure is dominated by $\theta_{VIA,wall}$ which is 162.7 °C/W and the solder fill plays a limited role in reducing the thermal resistance further. Thermal resistance can be further reduced by increasing plating thickness or filling the vias with copper or any other thermally conductive material.

Finally, the thermal resistance for the entire array can be thought of as a parallel network of 36 such single via resistances.

Hence $\theta_{BB'}$ = 3.99 °C/W.

Step 2: Calculating θ_{cond}

As described earlier, lateral thermal resistance for a PCB can be estimated using the formula:

$$\theta_{PCB} = \left(\frac{l}{k_{eff} A} \right)$$ Equation 11

Where:

θ_{PCB} = The lumped 1D lateral resistance of the PCB surfaces.

k_{eff} = The effective thermal conductivity of the medium (PCB in our case).

A denotes the surface area of the medium normal to the direction of heat transfer. In the example case, it is the product of length and PCB thickness.

ℓ = The thickness of the medium.

Step 3: Calculating θ_{conv} and θ_{rad}

As almost 96 percent of the heat in PowerPSoC is transferred through the thermal via array, eventually, majority of it is conducted through the PCB. Heat transfer by natural convection and radiation is minimal and can be neglected for simplicity. However, equations are provided for both natural convection and radiation. Detailed calculations are beyond the scope of this chapter. Refer to References [5] for details.

$$\theta_{conv} = \left(\frac{1}{h_{conv} * A_{surf}} \right)$$ Equation 12

$$\theta_{rad} = \left(\frac{1}{h_{rad} * A_{surf}} \right)$$ Equation 13

Where:

h_{conv}, h_{rad} = The convection and radiation heat transfer coefficients.

A_{surf} = The heat transfer surface area.

Now that we are equipped with all the basic tools, let us get back to the example. Assume the device junction is at 90 °C and work our way outwards using Equation 2. The heat flow is through the series network of θ_{JS} (2 °C/W) and $\theta_{BB'}$ (3.99 °C/W) and with a power dissipation of 3.2 W, results in a board temperature (at a point on the bottom layer, just below the device) of ~71 °C. Furthermore, using the PCB as a heat sink further cooling is provided by means of conduction, convection, and radiation to ensure that the θ_{PCB} allows maintaining this PCB temperature (~71 °C) at the worst case ambient temperature.

2.8 Summary

With systems increasing in power densities, it is important for system designers to think about thermal analysis as early as the initial design phase rather than treat it as an afterthought.

The thermal model for the device and one-dimensional (1D) equations for heat transfer provide a good tool for first pass thermal performance estimation. Based on this first pass analysis, the system designer may decide to perform detailed thermal modeling and simulation for the system before making crucial design decisions.

In PowerPSoC based designs, the PCB can and must be effectively used as a heat sink. PCB layout should not only consider electrical performance, but also the thermal performance of the system.

At times the designer must consider thermal versus electrical layout recommendations, which may be conflicting. Depending on the overall impact, either the thermal or the electrical recommendation can take priority.

2.9 Disclaimer

The techniques presented in this chapter are only meant for first pass thermal estimation. There is no single generalized method to calculate the combined impact of all the variables. Therefore, system designers are encouraged to use sophisticated CFD tools to model final component temperatures for their particular systems.

The chapter focuses primarily on the use of PCB as a heat sink. If using the PCB as a heat sink is not sufficient, other cooling techniques may have to be considered. These techniques are beyond the scope of this document.

In this document, “system” refers to a dc-dc converter. For systems having higher integration levels such as ac-dc circuitry or LED loads on the same PCB, techniques presented in this chapter may not apply. The focus of thermal analysis in this document revolves around PowerPSoC being the primary heat source.

Topics such as use of external heat sinks, forced convection, thermal interface materials, and specialized metal boards, are beyond the scope of this chapter.

2.10 References

1. Relevant Standards: JESD51, JESD51-1, JESD51-2, JESD51-3, JESD51-5, and JESD51-7, available at www.jedec.org
2. Application Note: *Surface Mount Assembly of Amkor’s MicroLeadFrame Packages* – Amkor Technology, September 2008
3. Chapter 17: Printed Circuits Handbook (McGraw Hill Handbooks) – 6th Edition, Darwin Edwards, Clyde F. Coombs, Jr., 2008
4. Application Note: *Thermal Considerations for QFN packaged Integrated Circuits* – Cirrus Logic, July 2007
5. Chapter 15: Heat Transfer – A Practical Approach (McGraw Hill Science) – 2nd Edition, Yunus A. Cengel, August 2002

3. PowerPSoC® PCB Design Guidelines for LED Driver Circuits

This chapter discusses component placement, signal routing, power routing, power paths, and thermal dissipation in the design of PCBs for LED drivers. The same guidelines apply for single or multiple LED drivers using a single PowerPSoC. Each section provides information on specific needs during the design process.

It is necessary for a PCB designer to understand that each circuit and design has its own critical parameters. A LED driver circuit is no exception, as there are significant levels of current flowing and switching throughout the circuit.

To understand an LED driver circuit, consider a switching voltage regulator. The difference between a switching voltage regulator and an LED driver is that a switching voltage regulator controls an output voltage, while an LED driver controls an output current.

For designers familiar with switching voltage regulator design, designing a power-LED driver using PowerPSoC should be an easy process, because many of the guidelines for a successful design are identical.

Even for designers less familiar with power electronics design, the PowerPSoC simplifies most of the design with its high integration of power components.

This chapter starts with a generic list of guidelines. These guidelines are explained in detail using an example of a single-channel floating-buck LED driver. Single-channel Boost LED driver, single channel Buck-Boost LED driver, and a four-channel LED driver design are all described subsequently in this document.

3.1 Guidelines and Checklist

Following are the key guidelines that can also serve as a checklist for PCB layout using the PowerPSoC:

1. Component selection and placement
   - Place key components close to each other
     a. Look for critical triangle
   - Use Kelvin sense resistor
   - Use appropriate power filters (ferrite beads)
   - Use test points at signals of interest, place them appropriately and match with ground test points
2. PCB selection and trace routing
   - Use copper sized for power
   - Use copper pours and copper thieving
   - Optimize via usage for power, control and signals
   - Optimize trace length and routing
   - Evaluate current loops
     a. Look for critical loops
   - Kelvin sense lines routed differentially
   - Kelvin sense lines isolated from cross coupling
3. Grounding
   - Digital, analog, power, and star ground
   - Consider return (ground) current

- Follow power and ground guidelines

4. Thermal aspects
   - Evaluate power losses in key components
   - Evaluate thermal dissipation
   - These guidelines are explained below using the example of a floating-buck LED driver.

3.2 Floating-Buck LED Driver

Figure 3-1. Single Channel Floating-Buck LED Driver

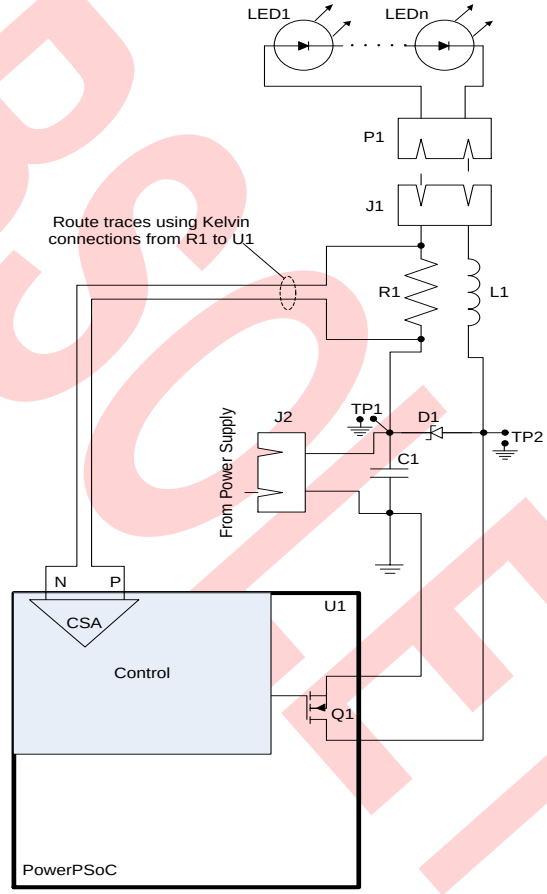


Figure 3-1 shows a generic diagram for a single channel floating-buck LED driver. The channel power components consist of

- Decoupling capacitor (C1),
- Sense resistor (R1),
- LED load (LED1 through LEDn),
- Freewheeling diode (D1),
- Inductor (L1), and
- Low side N-Channel MOSFET (Q1, which is within PowerPSoC)

Also shown are input power connector (J2), LED load connector (P1 and J1), test points (TP1 and TP2), and PowerPSoC LED controller (U1). For the purpose of this chapter, consider Q1 as separate from U1 when, in fact, Q1 is part of U1 (PowerPSoC).

This LED driver has two operating modes, when Q1 is ON and when Q1 is OFF.

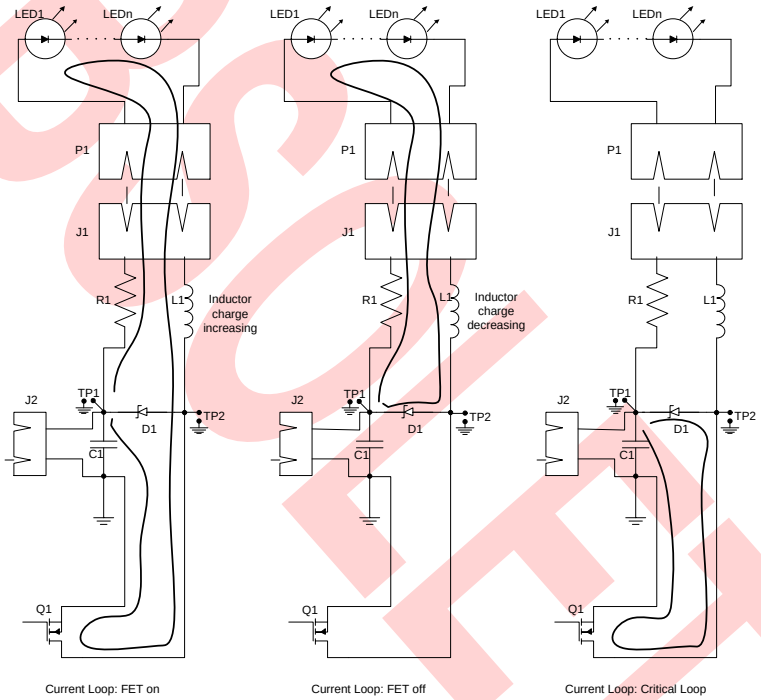
When Q1 is ON, the flux on L1 builds and the current loop is from C1, through R1, through LED load, through L1, through Q1, and finally back to C1. This loop is 'Current Loop: FET ON' (see Figure 3-2).

When Q1 is OFF, the flux on L1 decreases and the current loop is C1, through R1, through LED load, through L1, through D1, and back to C1. This loop is 'Current Loop: FET OFF' (see Figure 3-2).

The third loop in shown Figure 3-2 is 'Current Loop: Critical Loop' is the area that must have close attention during component placement. Three components Q1, C1, and D1 form a "Critical Triangle" defining the critical loop. Keeping this triangle small is critical, as it is where the power switching is most evident. When Q1 is ON, all the current flows through Q1 and ground, back to C1 and no current flows through D1; alternatively, when Q1 is OFF, all the current flows through D1 and none through Q1.

The critical triangle area is where the transition between the two modes happens. Minimizing the critical loop area reduces the ground bounce. Ground bounce is undesirable as it can cause system accuracy and stability problems.

Figure 3-2. Floating-Buck Current Loops



3.3 Components Guidelines

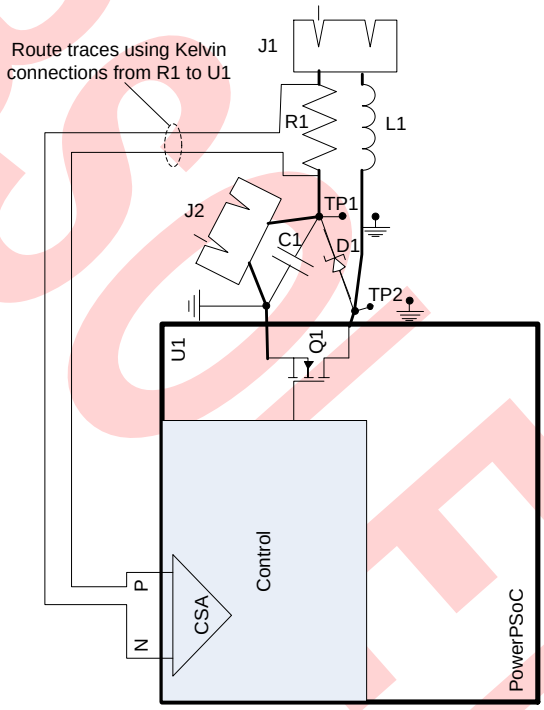
This section discusses placement of key components, Kelvin sense resistor connections, test point placement, and test point placement for ground.

3.3.1 Place Key Components Close to Each Other

In Figure 3-1, C1, D1, and Q1 define the critical triangle area. For these three components, place them close to each other, on the same side of the PCB, use no vias, and keep the copper interconnects short.

Figure 3-3 is similar to Figure 3-1, which is redrawn allowing the critical triangle relationship of C1, D1, and Q1 to be easily portrayed in a schematic representation.

Figure 3-3. Single Channel Floating-Buck Redrawn for Relative Component Association



3.3.2 Test Points at Signal of Interest

In Figure 3-3, test points (TP1 and TP2) are close to the points in the circuit being measured. This is to highlight the need to place a test point connection as close to the measured point as possible.

Figure 3-4 shows a poor placement of test points in layout. In this diagram, placement of TP1 is not correct as it is at the end of a long trace. The use of a long trace connecting a test point to the point of interest causes problems with signal reflection and acts as an antenna on the PCB - radiating signals to surrounding systems. The importance of not creating antennas is very critical, especially with signal nets that have large dv/dt. Placement of TP2 is also not correct, as it is not near the anode of D1.

Figure 3-4. Test Point Usage - Poor Implementation

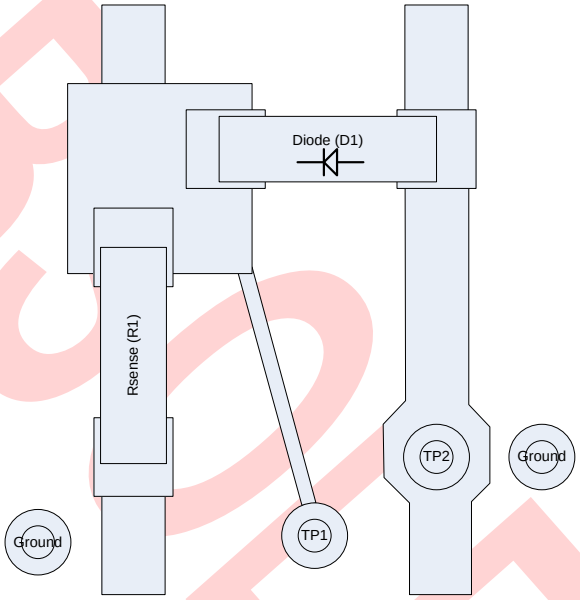
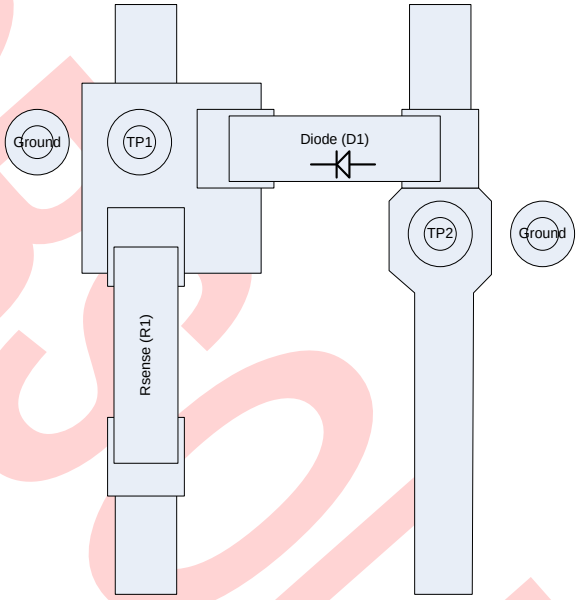


Figure 3-5 shows good placement of test points. In this diagram, the placement of TP1 and TP2 are correct according to the schematic that is showing TP1 close to the junction of R1 and D1, and TP2 is near the anode of D1.

Often, test points are accommodated as an afterthought on the layout and this can lead to poor implementation as shown in Figure 3-4. In such cases, having test points is worse than not having test points. It is preferable to have test point planning integral to the layout plan so that right trade-offs can be made.

Figure 3-5. Test Point Usage - Good Implementation



3.3.3 Test Points Matched with Ground Test Points

In Figure 3-1, there is a ground connection shown near each test point. This is to highlight the need to place a ground test point connection as close to the test point as possible and not to use a long (3-6 inch) ground lead. Check your test equipment specification to determine the spacing recommended for test signal to ground.

3.3.3.1 Use Kelvin Sense Resistor

In Figure 3-1, a note for the connections from R1 to U1 indicates 'route traces using Kelvin connections', Figure 3-6 and Figure 3-7 show two implementations of Kelvin sense lines.

Figure 3-6 shows an incorrect design for Kelvin sense lines. The connections for the sense lines are not located at the pads of R_{sense}. As the Kelvin sense lines measure a small voltage across a small resistance (0.1 to 0.2 Ω typical); any small resistance in the trace between the Kelvin connection and the R_{sense} component also has a small voltage drop across it. That additional drop causes measurement errors.

Figure 3-6. Kelvin Sense Lines - Incorrect Design

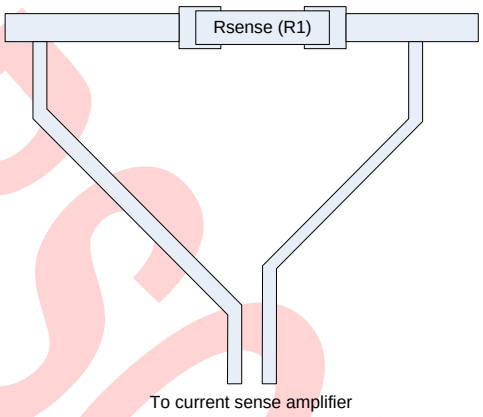
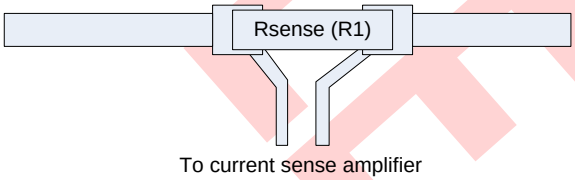


Figure 3-7 shows a correct design for Kelvin sense lines. The connections for the sense lines are located at the inner edge of the pads of R_{sense}. This is the best connection point for the Kelvin sense lines, as the voltage measured is the voltage developed across R_{sense}.

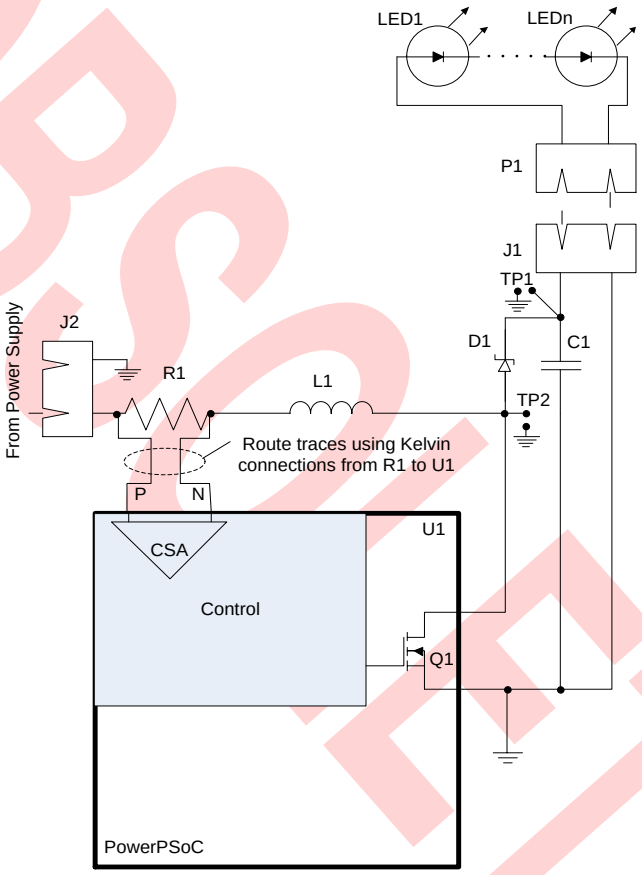
Figure 3-7. Kelvin Sense Lines - Correct Design



3.4 Boost Topology

Figure 3-8 shows a generic diagram for a single channel boost LED driver. The channel power components (same as floating-buck LED driver) consist of decoupling capacitor (C1), sense resistor (R1), LED load (LED1 through LEDn), freewheeling diode (D1), inductor (L1), and low side N-Channel MOSFET (Q1). Also shown are input power connector (J2), LED load connector (P1 and J1), test points (TP1 and TP2), and PowerPSoC LED controller (U1).

Figure 3-8. Single Channel Boost LED Driver

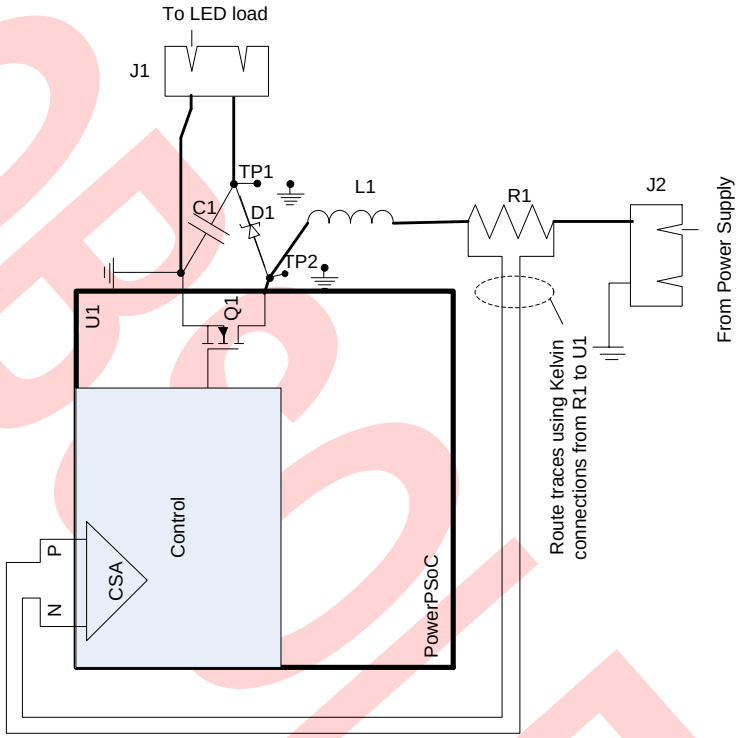


In Figure 3-8, C1, D1, and Q1 define the critical triangle area. For these three components, place them close to each other, on the same side of the PCB, use no vias, and keep the copper interconnects short.

Figure 3-9 is similar to Figure 3-8, which is redrawn to portray the critical triangle relationship of C1, D1, and Q1 in a schematic representation.

The critical triangle components are arranged in the same manner as in a floating-buck LED driver.

Figure 3-9. Single Channel Boost Redrawn for Relative Component Association

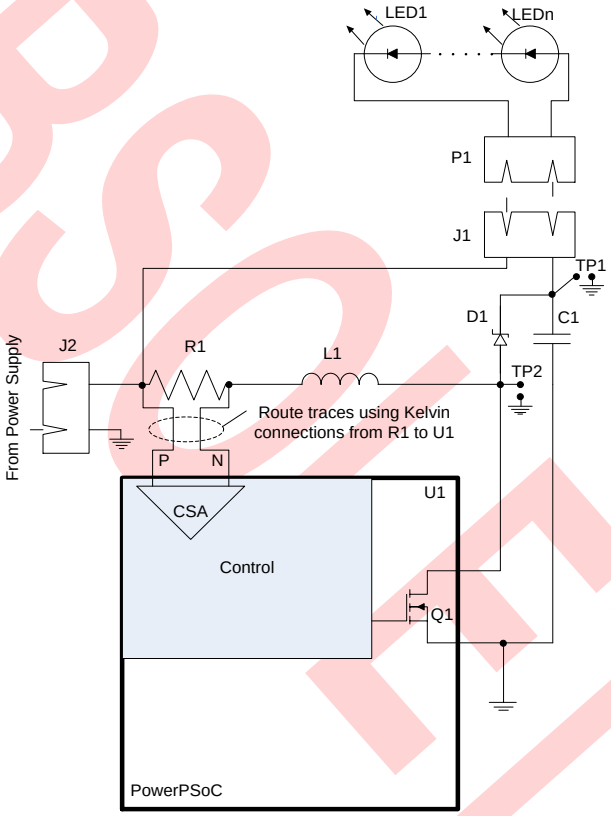


3.5 Buck-Boost Topology

In Figure 3-8, C1, D1, and Q1 define the critical triangle area. For these three components, place them close to each other, on the same side of the PCB, use no vias, and keep the copper interconnects short.

Figure 3-10 shows a generic diagram for a single channel buck-boost LED driver. The channel power components (same as floating-buck LED driver) consist of decoupling capacitor (C1), sense resistor (R1), LED load (LED1 through LEDn), freewheeling diode (D1), inductor (L1), and low side N-Channel MOSFET (Q1). Also shown are input power connector (J2), LED load connector (P1 and J1), test points (TP1 and TP2), and PowerPSoC LED controller (U1).

Figure 3-10. Single Channel Buck-Boost LED Driver

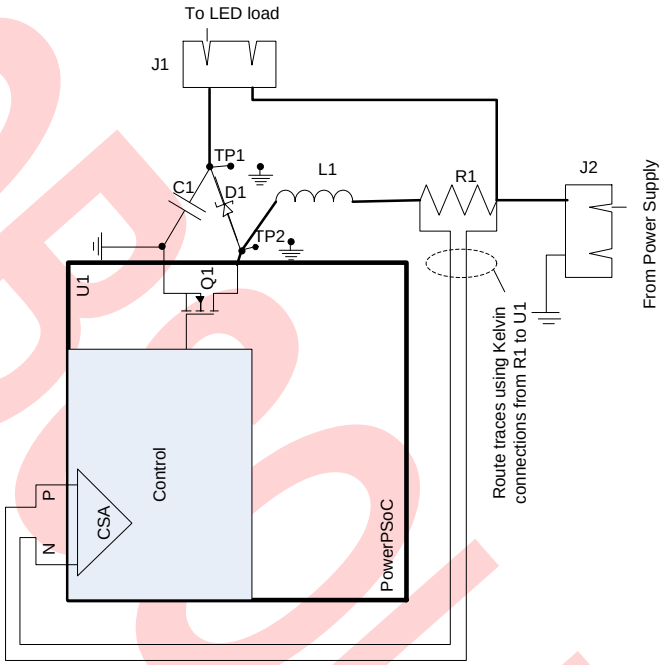


In Figure 3-10, C1, D1, and Q1 define the critical triangle area. For these three components, place them close to each other, on the same side of the PCB, use no vias, and keep the copper interconnects short.

Figure 3-11 is similar to Figure 3-10, which is redrawn portraying the critical triangle relationship of C1, D1, and Q1 in a schematic representation.

The critical triangle components are arranged in the same manner as in a floating-buck LED driver.

Figure 3-11. Single Channel Buck-Boost Redrawn for Relative Component Association



3.6 PCB Guidelines

The guidelines for LED driver PCBs are similar to those for analog PCBs. They cover choice of substrate material, copper weight and trace size, copper pours, via use, trace length, sense wires, and signal crosstalk.

3.6.1 PCB Substrate

Normally, the PCB substrate material is FR4 epoxy-glass. An alternative is to use a metal-core PCB substrate. Metal-core PCB is useful for designs that are dense for power dissipation and require extra metal core to remove the heat from critical components.

3.6.2 Use Copper Sized for Power

Copper weight is one of the design parameters, where the choice is between options (½-ounce, 1-ounce or higher), based on power/current requirements, cost, personal preference, or company requirements.

In digital designs, trace width is another design parameter accepted at default parameter or a trace width that works globally for system components. It is often the parameter sacrificed to address space constraints. However, with power applications, it is important to determine required trace widths for reliable operation of the circuit.

There are several online resources to calculate trace width based on copper weight, current capacity, and temperature rise. Use the following equations for internal and external traces[1].

Trace Cross-section Area

$$Trace_{cross-section} = h * w \quad \text{Equation 14}$$

External Trace Power

$$I_{max} = 0.048 * \Delta T^{0.44} * (h * w)^{0.725} \quad \text{Equation 15}$$

Internal Trace Power

$$I_{max} = 0.024 * \Delta T^{0.44} * (h * w)^{0.725} \quad \text{Equation 16}$$

In the equations:

I_{max} is the maximum current in Amps the trace can handle.

ΔT is the increase in trace temperature due to current flow. Recommendation is to limit the temperature increase between 10 °C and 20 °C.

h is the height of the copper. ½-ounce copper is 0.675 mil (17 microns); 1-ounce copper is 1.35 mil (35 microns); 2-ounce copper is 2.7 mil (70 microns).

w is the width in mil of the copper trace.

(**Note** 1 mil = 0.001 inch = 0.0254 mm = 25.4 microns)

An example for trace width calculation is:

I_{max} = 1 A, ΔT = 20 °C, copper weight = 2 ounce (2.7 mil), external layer.

Using Equation 15:

$$I_{max} = 0.048 * \Delta T^{0.44} * (h * w)^{0.725}$$
$$1 = 0.048 * 20^{0.44} * (2.7 * w)^{0.725}$$
$$1 = 0.048 * 3.736 * (2.7 * w)^{0.725}$$
$$1 = 0.1793 * (2.7 * w)^{0.725}$$
$$5.576 = (2.7 * w)^{0.725}$$
$$10.7 = 2.7 * w$$
$$w = 3.96\,(in\_mils)$$

3.6.3 Copper Pour

When determining the copper size for a higher power signal, the required trace width is often 0.050 inches (1.27 mm) or more. Trace widths of this size are very difficult to route between and around components. The alternative solution is to use copper pours for these electrical connections. The copper pours work around the uniform thickness requirements of a trace and allow selective widening of trace at available spaces.

A copper pour is a polygon placed on any PCB layer. The polygon size covers an area that allows connections of all pins for a specific signal (typically a power or ground signal that connects many components).

There may be one or more copper pours, on the same or different signal layers, in a design. Each copper pour provides any one or a combination of the following benefits.

- Reduces power loss of interconnects
- Improves thermal dissipation
- Provides EMI shielding
- Improves PCB fabrication (copper thieving)

3.6.4 Copper Thieving

Copper thieving is a term used by PCB fabrication companies. When a PCB has copper thieving applied, small squares of copper remain on the board in the large areas where no copper was originally present. The process has a dual improvement for the fabrication company. During the plating process, the copper plating is more even throughout the PCB and the etchant (copper removal chemical) lasts longer, as creation of the PCB removes less copper.

Copper thieving is a good concept as the PCB fabrication company has less waste and more profit, while the user gets a higher quality and less expensive board.

However, when a designer allows a PCB fabrication company to add copper thieving, there is no guarantee that the design performs according to the requirements. Therefore, the designer should solve the copper thieving question and maintain design control by adding copper pours to the layout before releasing for PCB fabrication.

3.6.5 Optimal Use of Vias

Vias are one of PCB design's facilities that engineers typically overuse or use incorrectly when designing a power electronics board (or in this chapter, an LED driver system). They offer convenience during layout, but can lead to poor circuit performance.

When idealized, one can think of vias as having zero effect on a design. This is far from reality, as vias have capacitance, inductance, and resistance. Some disadvantages of vias:

- Capacitance causes an edge rate to decrease; inductance delays a signal; and resistance causes a signal to decrease in amplitude.
- Placing vias reduces the space available for traces. When reducing this space, a signal may need a circuitous and longer route leading to system noise and signal degradation.
- Placing vias reduces the area through which ground currents can flow. Ground currents flow using the path of least resistance and placing a via in the direct path causes the ground current path to be indirect, thus adding unnecessary noise to the system ground.

If a via is used, ensure that the system performance is not affected; additional effort during placement and routing can avoid potential problems.

3.6.6 Placing Power Vias for Decoupling

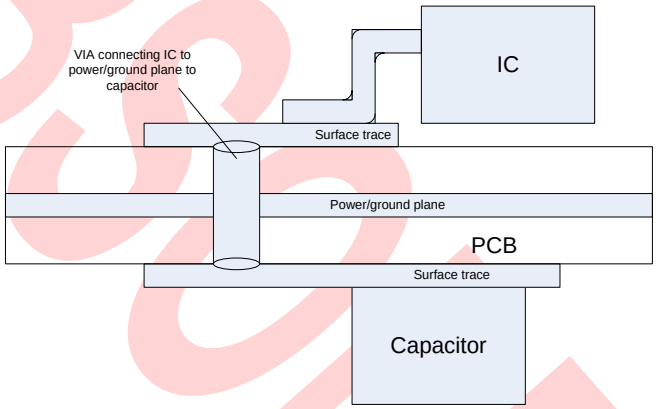
Although avoiding the use of vias is difficult when connecting from a power/ground plane to surface-mount components, let us evaluate their effectiveness for decoupling.

A typical example of placing vias is connecting a power plane to a decoupling capacitor and power pin of an IC. There are a minimum of three cases (and many more derivatives) for placing vias connecting a decoupling capacitor and an IC's power pin to a power or ground plane.

The capacitor and IC are on opposite sides of the power or ground plane as shown in Figure 3-12.

This implementation is almost the same as using no capacitor. As the power or ground plane is between the IC (current load) and the capacitor, the power or ground plane sources the majority of power directly. The capacitor is now acting as bulk power storage as opposed to the noise filter needed. This implementation is not the correct method to connect decoupling capacitors.

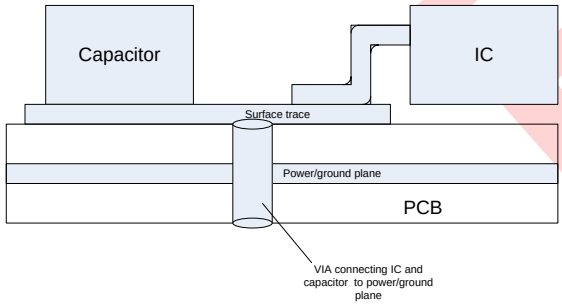
Figure 3-12. Capacitor, IC, and Via Orientation 1



Capacitor and IC on same side of power or ground plane, with via placed between them for connection to power or ground plane as shown in Figure 3-13.

This implementation is slightly better than not using a capacitor. As the power or ground plane via connection is between the IC (current load) and the capacitor, the power or ground plane sources the power in parallel with the capacitor. In this orientation, the capacitor accomplishes only a partial functionality.

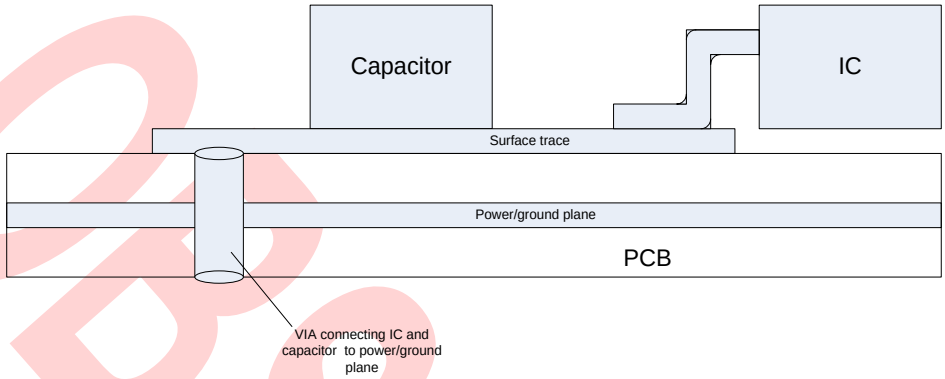
Figure 3-13. Capacitor, IC, and Via Orientation 2



Capacitor and IC on same side of power or ground plane, with the capacitor placed between the IC and the via connecting to the power or ground plane as shown in Figure 3-14.

This is the best implementation. As the capacitor is between the power or ground plane via and the IC (current load), the capacitor is the first source of power for the IC. This allows the capacitor to function as required. It prevents unwanted power noise from reaching the power or ground plane and affecting other system components.

Figure 3-14. Capacitor, IC, and Via Orientation 3



In some cases, multiple decoupling capacitors are used for a power pin to handle different transients. Place the capacitor with the smaller value closer to the pin so that it can respond to the high-frequency power demands quicker than larger capacitors placed further away, to handle the lower-frequency power demands before the power gets into the rest of the system.

3.6.7 Via Size

The size of vias is another design parameter often accepted at its default value. For generic applications, smaller vias are preferred for space consideration while maintaining manufacturability.

Vias are designed for different uses such as basic signal, power control, or power. Just as trace width is determined for specific currents, vias also need to be defined for a specific use.

1. A via used for a basic signal interconnect may be small, such that its size is at the lower limits for manufacturability. A via size may be 10/15 (hole/pad size in mils) or 15/20 for basic signal interconnect.
2. A via used for power control may be slightly larger, based upon the amount of current passing through it. A power control via size may be 15/20 or 20/25.
3. A via use for power may be sized even larger depending upon the level of current that it passes. A power via size may be 15/20, 20/25, 25/30, or larger.

To calculate via current yourself, use the following equation:

Via Circumference (mils)

$$C_V = (T_V + D_V) * \pi$$ Equation 17

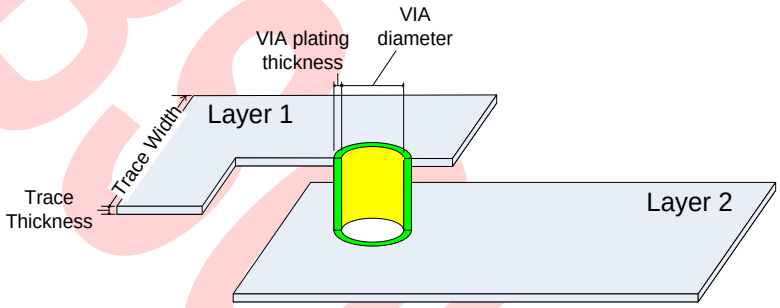
C_V is Circumference of via.

T_V is the via plating thickness.

D_V is the via diameter after plating. This value is typically the value specified as the hole-diameter for the PCB fabrication. The PCB fabricator overdrills the hole and then plates back to the specified hole-diameter.

Circumference is calculated from the center of plating on one side of the via directly across to the center of plating on the opposite side of the via. (½ via plating + via diameter + ½ via plating) = (via plating + via diameter)

Figure 3-15. Cutaway View of a Via



With the via circumference calculated, use that value as w (the width) and use the via plating thickness as h (the height) to determine the via's cross-section

Via Cross-section Area

$$VIA_{cross-section} = h * w \text{ (mils)}$$ Equation 18

h is the Via plating thickness (T_V)

w is the Via circumference (C_V)

For via to handle the same current as the trace it is used in, the via cross-section must be equal to or greater than the trace's cross-section.

An example for via calculation is:

Via diameter = 15 mil, Plating thickness = 1 mil

Using Equation 17 to calculate via circumference (in mils)

$$Cv = (Tv + Dv) * \pi$$
$$Cv = (1 + 15) * \pi$$
$$Cv = 16 * \pi$$
$$Cv = 50.27$$

Using Equation 18 to calculate via cross-section (sq. mils)

$$VIA_{cross-section} = h * w$$
$$VIA_{cross-section} = 1 * 50.27$$
$$VIA_{cross-section} = 50.27$$

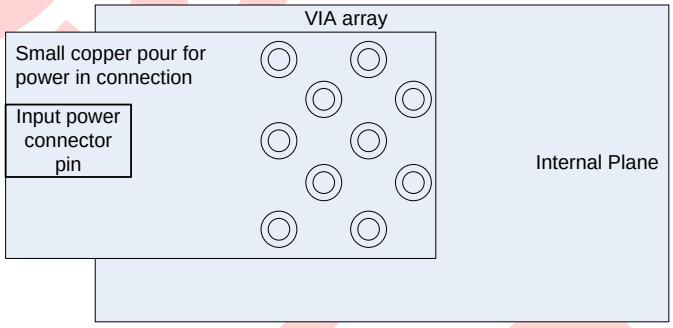
This is equivalent to a 35 mil wide trace with 1 oz copper.

3.6.8 Via Quantity

So far, we have discussed using vias one at a time. However, you can parallel vias similar to any basic electrical circuit paths.

Figure 3-16 is an example where parallel vias are used to connect a surface mount connector to a power or ground plane. Using a single via to pass large current quickly damages it due to excessive heat. Further, it also increases the noise on the power or ground plane. Placing several vias in parallel provides many paths for current flow between the connector and the power plane, and increases heat dissipation paths and decreases noise.

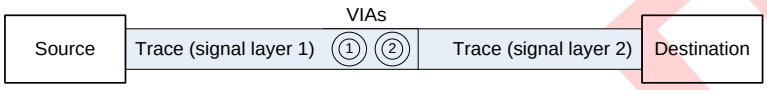
Figure 3-16. Via Array for Power or Ground Plane Connection



Another, not-so-obvious example is using multiple vias interconnecting signal layer changes for power control nets. For example, when driving the gate of a FET, often 1 A or more of gate current flows in the trace connecting the driver to the FET during the t_{on} and t_{off} transition of the FET.

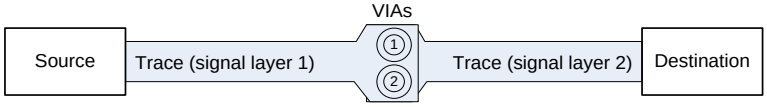
In Figure 3-17, an example of two vias in a power control trace shows an ineffective method of paralleling vias. As the current passes via1, the available trace width is narrowed due to the loss of surface copper related to the via hole. This leads to increased impedance and ineffectiveness of via2, end result is that the effect of paralleling is lost. The problem occurs twice in this example, one on each layer. As the signal travels from the source, the narrowing occurs as the signal passes via1 to via2. After the signal passes through the vias, a second narrowing occurs as the signal travels from via1 past via2 to the destination.

Figure 3-17. Two Vias in Power Trace - Poor Implementation



In Figure 3-18, an example of two vias in a power control trace shows a more effective method of paralleling vias. The narrowing of traces problem shown in Figure 3-8 is no longer present as the current passes to and from both vias equally with no restriction.

Figure 3-18. Two Vias in Power Trace - Good Implementation



3.6.9 Thermal Power Connections

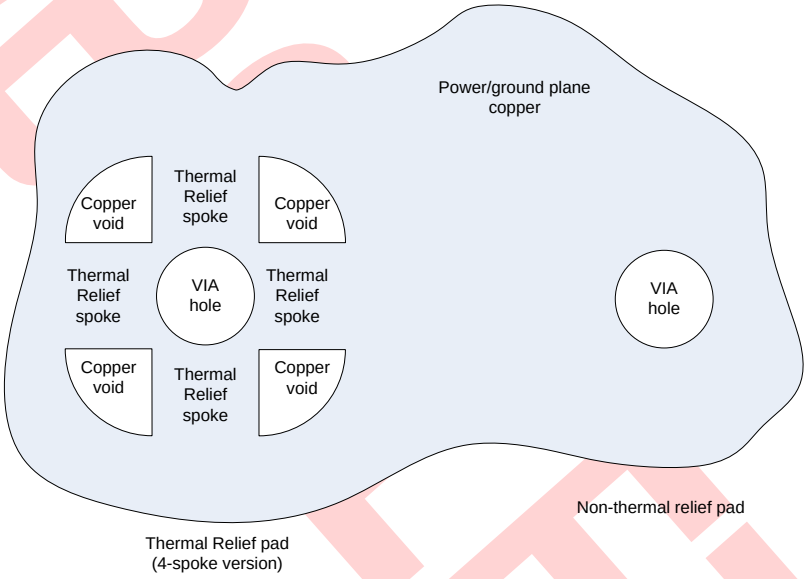
When connecting a component pin to a power or ground plane (or to large copper pours), a thermal connection is often used.

In a thermal connection, the amount of heat necessary to rework a component is much less than if the connection to the power or ground plane is solid or non-thermal relief style.

Figure 3-19 shows two power or ground interconnect styles, a thermal relief style and a non-thermal relief style. The thermal relief style connection has a general appearance of a wheel, where removal of small sections of the power or ground plane copper forms a small thermal isolation around the central connection hole. The remaining 'copper spokes' make the connection to the power or ground plane.

When using thermal relief connections, the designers must evaluate the size and quantity of spokes for thermal capacity just as they evaluate trace widths for power capacity.

Figure 3-19. Power or Ground Connection Styles



3.6.10 Minimize Trace Length

System performance and reliability improves when interconnecting traces are short.

A long trace has power loss associated with voltage drop directly related to the trace length. When power is lost in the trace, system power efficiency is lower.

Longer traces cause problems routing additional traces, require additional vias, reduce the area for component placement, and increase the system cost because a larger PCB is required.

3.6.11 Prioritize Trace Routing

Minimizing all traces is often not possible, as placement of key components require some traces to be longer than desired. In this case, it is necessary to prioritize or rank the importance of trace routing.

Table 3-1 shows a prioritization of nets. This table is an example; evaluate your design for importance of each net.

Table 3-1. Net Usage Prioritized

Priority	Net Usage
1	Analog (AC)
2	Analog (static/DC)
3	Power (high current)
4	Power control (high current switching)
5	Digital signals (high speed - MHz)
6	Digital signals (low speed - kHz)
7	Digital signals (static/DC)

3.6.12 Route Sense Lines Differentially

Correct routing of the Kelvin sense lines is important in closed loop systems where the current regulation is performed after sensing the current across a sense resistor. The voltage delta between the differential sense lines is often less than 100 mV, so a 2 to 3 mV system noise can affect the sense accuracy by 5 percent. Noise on the sense lines causes additional inaccuracies, as the system constantly corrects for the sensed noise.

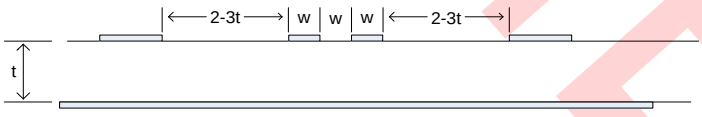
Attention to routing of sense lines prevents noise and allows simple, effective, and easy system operation. Methods for prevention of noise on sense lines include:

- Net spacing,
- Shielding,
- Avoidance of vias and
- Isolation from nets that have high dv/dt during operation.

Often, differential sense lines are routed with a separation between them equal to one trace width (W) and the next closest trace a minimum of two (prefer three) times the distance (t) to the closest layer.

Additional improvements include keeping the layer below the sense lines unbroken and placing a guard-ring around the sense lines.

Figure 3-20. Sense Line Spacing



An example of sense line spacing is if the differential sense lines are 10 mils in width (W), the spacing between the two tracks is 10 mils. And the spacing between the signal layer the sense lines are on to the copper layer immediately below is 20 mils (t), then the next closest trace is 40-60 mils (2 to 3 times t).

3.7 Power Guidelines

This section discusses power filters, power loss, power vias, current loops, and current flow.

3.7.1 Power Domains (Filtering)

In a system, there can be one or more power domains: analog, digital, power control, DC power, and switched power.

In each power domain, despite DC requirements, there is certain AC content (in the form of ripple and noise). This AC content ranges from low magnitude (10 mV) and low frequency (1 Hz) ripple for an analog supply to a high magnitude (200 mV) and high frequency (2 MHz) ripple for a switching power supply.

Many of the power domains are often at the same DC level (+5.0 V). To save the cost of adding separate voltage regulators to the design for each power domain, voltage regulators can be combined. To prevent high-frequency noise from a noisy section crossing into a quiet section, a high-impedance path between power domains is often provided by low-cost ferrite beads.

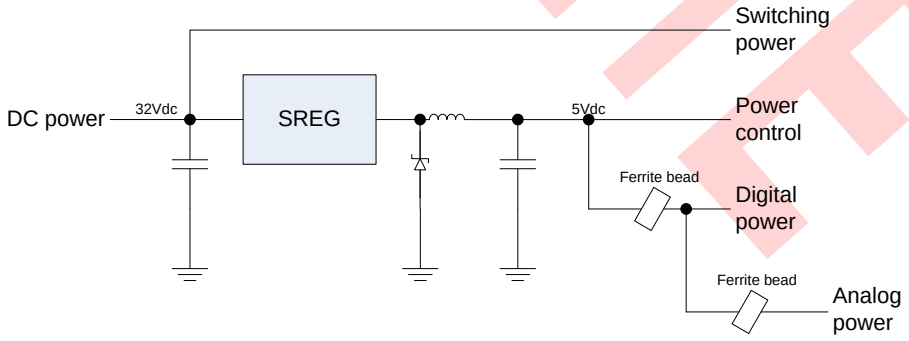
When designing, decide which power domain is critical and needs a separate supply or can use ferrite beads. Table 3-2 gives an example of supply prioritizing for noise. The supply domain that has the greater need for low noise has the smaller number.

Table 3-2. Supply Domain Noise

Noise Priority	Supply Domain
1	Analog
2	Digital
3	Power control
4	Switching power
5	DC power

Figure 3-21 is an example of connecting power domains using ferrite beads. In the diagram, DC power arrives from an external supply to drive the switching power and the SREG (switching regulator) in the PowerPSoC. The output of SREG connects directly to the high current (power control) domain. To keep the power noise of the power control from affecting the digital power, a ferrite bead isolates the digital power domain. Further isolating the analog power domain is another ferrite bead between the digital power and analog power. The analog power must be the least noisy domain, so this connection scheme has isolated from the power control domain by connecting to the digital domain.

Figure 3-21. Power Domain Connection



3.7.2 Power and Voltage Loss

This section discusses trace resistance and the associated voltage or power loss associated with the resistance of the copper[2].

Trace Resistance (Ω/inch)

$$R = \frac{L * 0.65866 * 10^{-6}}{w * h}$$ Equation 19

R = trace resistance in ohms.

L is the length of the trace in inches.

$0.65866*10^{-6}$ is resistivity of copper on a PCB.

w is the width in inches of the PCB trace.

h is the height in inches of the PCB trace:

½-ounce copper is 0.000675 inches

1-ounce copper is 0.00135 inches

2-ounce copper is 0.0027 inches

Trace Voltage Loss

$$V_{loss} = R * I$$ Equation 20

R is the trace resistance from Equation 19.

I is the current flowing through the trace.

Trace Power Loss

$$P_{loss} = V_{loss} * I$$ Equation 21

V_{loss} is the trace voltage loss from Equation 20.

An example of trace resistance, trace voltage loss, and trace power loss is given next:

Trace length = 2 inches, Copper weight = 2-ounces, Trace width = 10 mil. Current = 1 A.

Use Equation 19 to calculate trace resistance in Ω.

$$R = \frac{L * 0.65866 * 10^{-6}}{w * h}$$

$$R = \frac{2 * 0.65866 * 10^{-6}}{0.010 * 0.0027}$$

$$R = \frac{1.31732 * 10^{-6}}{27 * 10^{-6}}$$

$$R = 48.79 * 10^{-3}$$

Use Equation 20 to calculate the voltage loss in Volts.

$$V_{loss} = R * I$$

$$V_{loss} = 48.79 * 10^{-3} * 1$$

$$V_{loss} = 48.79 * 10^{-3}$$

Use Equation 21 to calculate the power loss in Watts.

$$P_{loss} = V_{loss} * I$$
$$P_{loss} = 48.79 * 10^{-3} * 1$$
$$P_{loss} = 48.79 * 10^{-3}$$

This calculated loss of about 50 mW is significant. There may be many more such traces and cumulative loss can far exceed the loss budget of the circuit. It should be noted that the PCB trace loss is generally ignored in initial circuit design calculations, where only component losses are computed. Additionally, the 50 mV computed voltage drop along the trace can result in signal loss in big circuits and is not advisable. In this example, there is a need to increase the trace width by at least 3x (and/or reduce trace length by similar ratio) to reduce the voltage drop and the power losses.

3.7.3 Multiple Vias for Power

Use multiple vias when connecting from a surface-mount power component to a power or ground plane. Using one via to pass amps of current quickly burns out the via or has a very large voltage drop passing through it. This allows system noise to easily get into the power or ground plane. In this case, placing several vias in parallel provides many via paths for the current to flow from the power component to the power plane as shown in Figure 3-16.

The following two sections walk you through calculating the current that a via can easily pass.

For a Thermal Relief Via:

- Use Equation 17 to calculate via circumference
- Use Equation 18 to calculate the via cross-sections.
- Use Equation 16 to calculate the maximum surface via current – note that a via is treated as equivalent to an internal layer. Record this value for final comparison with ‘Thermal via current’.
- Use Equation 15 to calculate the thermal spoke cross-section.
- Multiply the thermal spoke cross section by the number of thermal spokes for that via.
- Use Equation 14 to calculate the maximum Thermal via current.
- Use the smaller value of ‘surface via current’ or ‘Thermal via current’ as the maximum via current.

For a Non-Thermal Relief Via:

- Use Equation 17 to calculate via circumference.
- Use Equation 18 to calculate the via cross-section.
- Use Equation 16 to calculate the maximum via current.

3.7.4 Evaluate Current Loops

When a ground plane is used for the return path of currents, the flow of current has to be analyzed carefully.

Current flows in two paths: the path of least resistance and the path of least impedance. This does not mean that current selects one of the two paths and only flows in that path. Current constantly transitions (or divides proportionally) between the two paths based upon system operation.

The path of least resistance is a straight line between two points. This is the path during DC or static operation shown in Figure 3-22.

The path of least impedance is the path directly below a signal during its transition. This is the path during AC or switching operation shown in Figure 3-22.

In Figure 3-22, the area between DC and AC is the transition time when current is changing paths between least resistance and least impedance. This transition time between DC and AC can be the most troublesome as there is minimal control over the return path.

The available control mechanisms (star ground and ground plane cuts) are presented in the next section.

Figure 3-22. Signal and Current Path

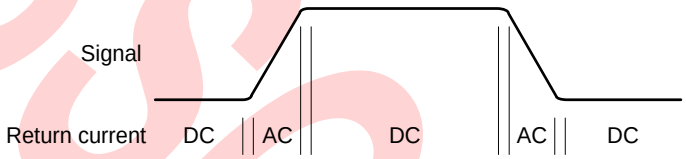
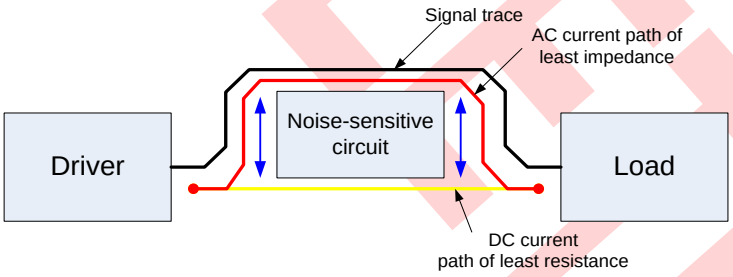


Figure 3-23 is an example of current flow path in a board. In the example, there are three blocks, driver, load, and noise-sensitive circuit. Connecting the driver and load is a signal trace. Shown in the example are two return paths, an AC current path of least impedance and a DC current path of least resistance. Looking at this diagram, the current flow paths appear acceptable. What is not shown is as the signal (in Figure 3-22) changes state, the current passes through the noise-sensitive circuit, not once, but twice for every signal transition as shown by the transition space in Figure 3-22.

Figure 3-23. Current Flow Path Diagram



3.8 Common (Ground) Guidelines

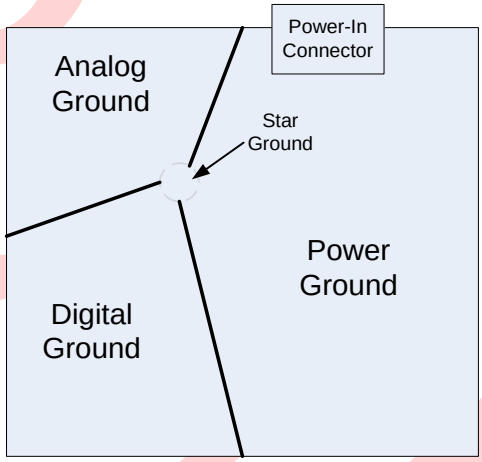
This section discusses star ground and ground planes.

3.8.1 Digital, Analog, Power, and Star Ground

Using a ‘star ground’ in a system is one method of preventing ground currents affecting noise-sensitive circuits. Star ground, also called reference ground, is the one point in a system where all the ground domains such as analog, digital, and power connect.

Figure 3-24 is an example of a star ground implementation. The example shows three grounds (analog, digital, and power) connected together at a single point in the system.

Figure 3-24. Star Ground Example

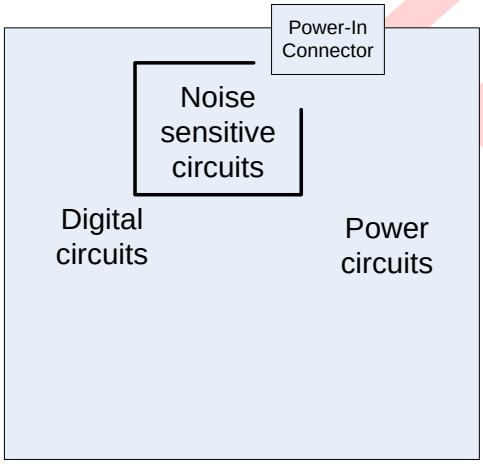


3.8.2 Ground Plane Cuts or Voids

Another method to control ground currents is selectively place openings or voids in the ground plane. The openings affect the current by forcing it to flow in a specific path, around or away from noise sensitive circuits.

Figure 3-25 is an example implementation for selectively placing a cut in the ground plane. The example shows three grounds (analog, digital, and power) all on the same ground plane reference, with a cut placed around the noise sensitive (analog) circuits forcing the ground return currents to flow around the critical area.

Figure 3-25. Ground Plane Cut Example



3.9 Thermal Dissipation Guidelines

The EPAD connection of the PowerPSoC must connect to copper on both sides of the PCB for solid thermal dissipation. To connect both sides of the PCB, place 16 vias (4x4 array) in the area for EPAD attachment. The fabrication of the PCB needs to specify filling these 16 vias. The reason for filling the vias during fabrication is that during the assembly process, when the solder is reflowed for device attachment, if the vias are not filled, the solder is pulled away from the PowerPSoC by the solder flowing into the non-filled vias. Filling the vias during the PCB fabrication process prevents the solder from flowing away and keeps a solid thermal connection between the PowerPSoC EPAD and the PCB copper.

More details about the PowerPSoC thermal dissipation are included in a separate chapter in this document.

3.10 Example PCB layout

Cypress's CY3268 (PowerPSoC demo board) implements a four-channel 300 mA LED current system using two layers. Also implemented on the CY3268 system are other functions, such as on-chip debug (OCD), in-system serial programming (ISSP), and CapSense.

Figure 3-26 shows the top layer and its silkscreen. Viewing the top layer, one can identify

1. the use of copper pour to minimize power and voltage loss in the system,
2. placement of critical components to minimize the critical triangle loops, and
3. placement of input power (CON1) to minimize the high power current flow affecting the low power digital and analog circuits.

The critical triangle components (all placed on the top layer) are:

- Channel 0: U2, D5, C21, and C17
- Channel 1: U2, D3, C19, and C15
- Channel 2: U2, D7, C27, and C28
- Channel 3: U2, D6, C24, and C25

At the bottom of Figure 3-26 are the five CapSense buttons to control the LED intensity.

Figure 3-26. CY3268 PCB - Top Layer

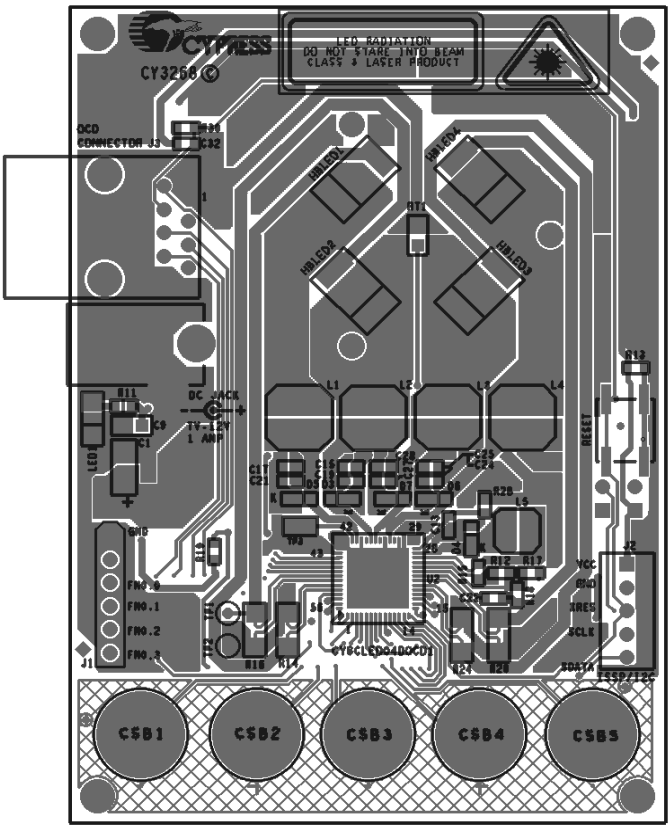


Figure 3-27 shows the bottom layer and its silkscreen. The bottom view is similar to looking through the PCB from the top for easy reference of interconnects between the top and bottom layers. One can identify the use of copper pour for heat dissipation for the four LEDs and PowerPSoC. Also note that there is no copper below the CapSense; the PCB fabrication cannot place copper thieving on the PCB.

Figure 3-27. CY3268 - Bottom Layer

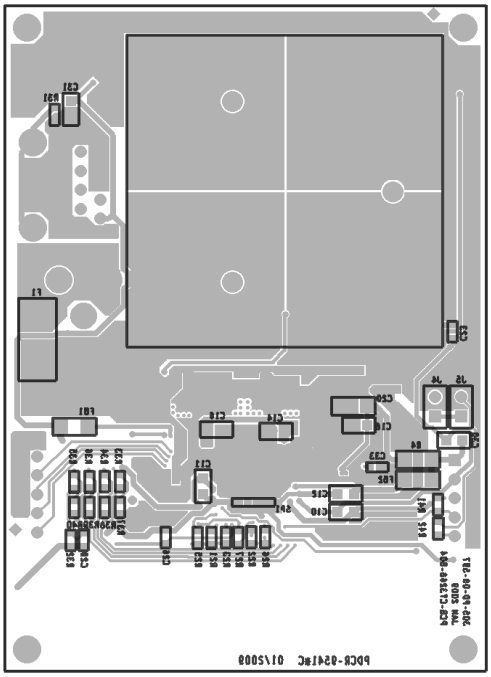


Figure 3-28. Photograph with a Close-up View of CY3268 Board

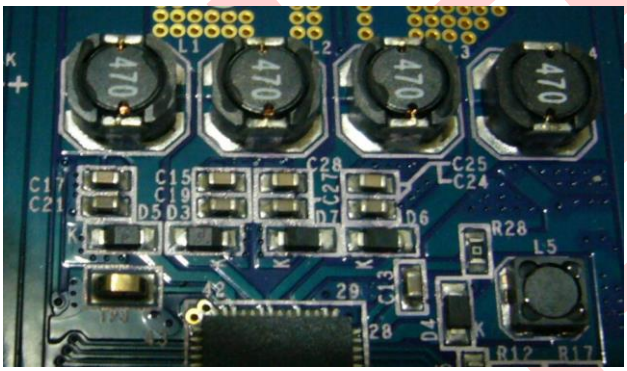


Figure 3-28 shows a close-up view of the CY3268. Notice placement of the filter capacitor, diode and MOSFET in each channel to form a critical triangle with minimum loop area.

For additional information on the CY3268 demo board, visit Cypress's website.

3.11 Summary

This chapter provides expert advice, guidelines, and information on PCB design for LED power drivers using PowerPSoC (CY8CLED0xD/G0x). It discusses component placement, signal routing, power routing, power paths, thermal dissipation, and driver testing.

3.12 References

1. IPC-2221 based trace width calculations: http://www.desmith.net/NMdS/Electronics/TraceWidth.html
2. http://www.eeweb.com/toolbox/trace-resistance

4. Minimizing Power and Ground Transients in LED Driver Circuits

This chapter provides information on PowerPSoC power and ground domains, transient suppression and noise filtering techniques using decoupling capacitors and ferrite beads. It describes how to select a decoupling capacitor and provides examples to calculate the minimum capacitance based on system parameters. A section on ferrite beads is also included.

The power information provided defines four PowerPSoC domains:

1. High voltage device drain (HVDD),
2. Gate drive voltage device drain (GDVDD),
3. Voltage device drain (VDD), and
4. Analog voltage device drain (AVDD).

The ground information provided defines four basic PowerPSoC domains:

1. High voltage supply source (HVSS),
2. Gate drive voltage supply source (GDVSS),
3. Voltage supply source (VSS), and
4. Analog voltage supply source (AVSS).

A fifth optional ground domain, Quiet voltage supply Source (QVSS), is also described. QVSS is defined as a star or quiet ground used as a common reference within the system.

4.1 Power Domains

There are four power domains used by the PowerPSoC: High Voltage (HVDD), Gate Drive (GDVDD), Digital (VDD), and Analog (AVDD). Most PowerPSoC system designs operate well with one +5 V power plane and when all +5 V power pins (GDVDD, VDD, and AVDD) are connected directly to the plane:

- HVDD domain is the voltage used to power LED strings, current sense amplifiers (CSAs), and SREG (5 V Switching Regulator inside the PowerPSoC). This voltage ranges from 7 V through 32 V depending upon system requirements. This voltage connects to the CSAs, the LED string anode, (typically through a current sense resistor), and the SREG input. Each LED string driver requires up to 1 A current. The SREG is capable of supplying up to 250 mA. If the SREG supplies 250 mA, the input source current is slightly less than 200 mA when the HVDD is low (7 V) and much less when the HVDD is high (32 V).There are five connections to the HVDD power domain on PowerPSoC: four CSAs (four LED channels) and one SREG.
- GDVDD domain is the voltage used to power the N-Channel MOSFET gate drivers used during regulation of current through the LED strings. The voltage for this domain is nominally 5 V. If driving external N-Channel MOSFETs, the transient current can be up to 1 A per channel with the average current typically less than 50 mA per channel. Using the internal N-Channel MOSFETs, the peak gate current can be up to 0.25 A per channel with average current typically less than 10 mA per channel. The CY8CLED0xD/GOx has two PowerPSoC pins connecting to GDVDD power domain. Both pins must connect to GDVDD.
- VDD domain is the voltage used to power the digital portion and basic analog portion of the PowerPSoC. The voltage for this domain is nominally 5 V. The maximum average current is 50 mA. There are two PowerPSoC pins connecting to VDD power domain. Both pins must connect to VDD.

- AVDD domain is the voltage used to power the analog block portion of the PowerPSoC. The voltage for this domain is nominally 5 V. The maximum average current is 25 mA. This domain is for analog system ADC and DAC accuracy. There is one PowerPSoC pin connecting to AVDD power domain.

Figure 4-1 is a schematic representation of the recommended distribution and interconnect for the four power domains. The ferrite beads shown are optionally used for a system that is particularly concerned with EMI affecting the PowerPSoC operation and accuracy. The ferrite beads are not required for the PowerPSoC to operate or regulate current through the LED arrays. The block labeled SREG, the diode, the inductor, and the SREG capacitor are part of the SREG circuit detailed in Figure 4-2.

Figure 4-1 also shows an interconnect diagram for recommended power connections. HVDD arrives from an external or on-board power supply. SREG uses HVDD to create a regulated 5 V supply for all the 5 V power domains. In some systems, an external 5 V regulator is used in place of SREG (for higher current requirements). The GDVDD domain has the highest transient currents and connects to the SREG output. The SREG output needs a 10 µF (minimum) bulk storage capacitor for noise filtering.

An optional ferrite bead for reducing EMI effects can be used for connecting VDD to GDVDD, which attenuates the transient noise from GDVDD to VDD. The ferrite bead reduces coupling of the GDVDD domain noise to the VDD and AVDD power domains.

Similarly, an optional ferrite bead for reducing EMI effects can be used for connecting AVDD to VDD, which attenuates the VDD noise and transient GDVDD noise getting into AVDD. The ferrite bead reduces coupling of the GDVDD and VDD domain noise to the AVDD power domain.

The decoupling capacitors shown on each power domain are local to each power pin within the domain. There may be more than one decoupling capacitor per power domain.

Figure 4-1. Basic Power Interconnect

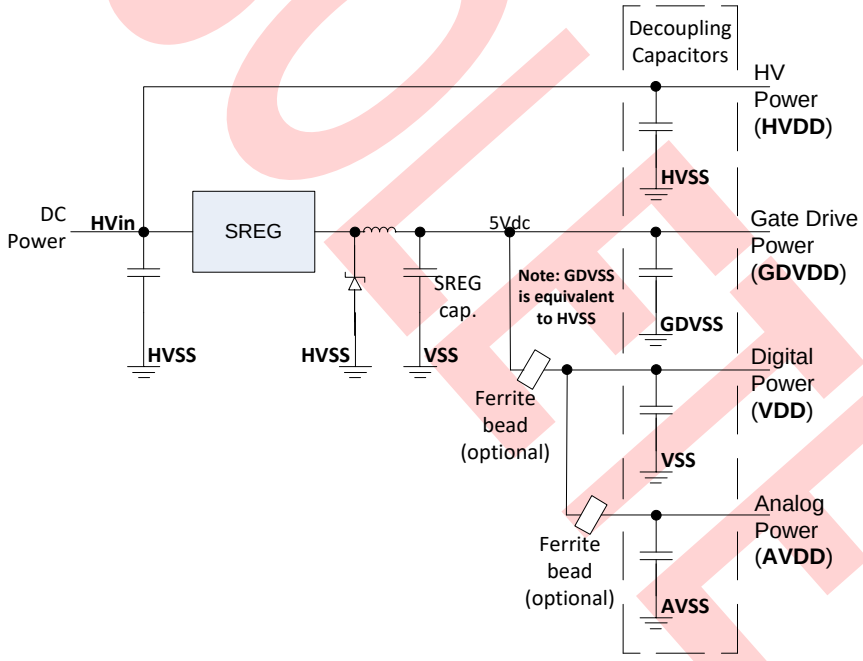
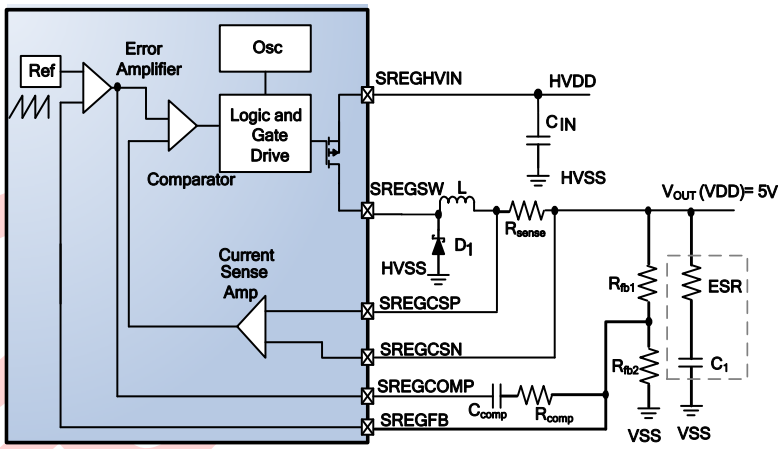


Figure 4-2. SREG Circuit



4.2 Ground Domains

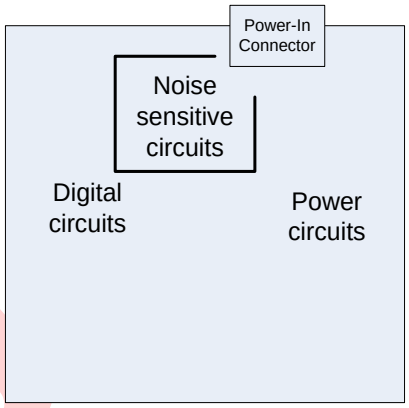
There are four ground domains used by the PowerPSoC: High Voltage (HVSS), Gate Drive (GDVSS), Digital (VSS), and Analog (AVSS). An optional quiet/star ground (QVSS) can be used to isolate EMI currents in the ground plane. Most PowerPSoC system designs operate well with one ground plane and with all ground pins (HVSS, GDVSS, VSS, and AVSS) connected directly to the plane.

The HVSS and GDVSS domains are the grounds used to return the HVDD power and GDVDD power respectively. They are often combined for layout integrity. HVSS provides a return point for the individual N-Channel MOSFET source connections and the load current. GDVSS provides a return for the gate drive current used for external N-Channel MOSFETs. The HVSS and GDVSS domains have the highest system transient currents and hence require tight layout and sufficient bypassing. The transient currents are associated with N-Channel MOSFETs turning ON and OFF during LED current regulation. The transient currents can be as high as 1 A per channel for 10 to 20 ns. There are 6 PowerPSoC connections to HVSS+GDVSS ground domain: two GDVSS pins and four PGND pins (one for each channel). In addition, the external power grounds (at filter capacitors) should also be connected to the HVSS plane and the external SREG components should be returned to the GDVSS pins. The VSS domain is the ground used to return the digital portion of the PowerPSoC. There are three PowerPSoC pins connecting to the VSS ground domain.

The AVSS domain is the ground used to return the analog portion of the PowerPSoC. There is one PowerPSoC pin connecting to the AVSS ground domain.

Figure 4-3 shows a ground concept in which no QVSS is used and all grounds are treated as one. This concept makes no distinction between HVSS, GDVSS, VSS, and AVSS. In this concept, consider component placement and the flow of ground plane currents. In Figure 4-3, a cut is placed in the ground plane around the area where noise sensitive circuits are placed. The cut leaves a small connection between ground for the sensitive circuit and other power grounds (very close to the input power connector). However, it forces ground current from the digital and power circuits to flow around the sensitive circuit. The sensitive ground remains unaffected by transient currents.

Figure 4-3. Unified Ground Connection



For systems where high-frequency currents are flowing in the ground plane, an optional system-level star ground (QVSS) can be implemented. The use of QVSS reduces the effect of transient currents in the HVSS ground domain from affecting the VSS and AVSS ground domains. Further splitting of the Power Ground into HVSS and GDVDSS domains is also possible.

In operation, QVSS ground domain is one point in the system where all ground domains connect. This point ensures that the transient power from one domain does not affect any other ground domain.

To understand how star ground works to minimize the effect of transient HVSS current on VSS or AVSS domains, remember that current is similar to a river and always takes the path of least resistance between any two points. It also expands beyond the path of least resistance during times of large transient current. Current causes the ground domain to change reference level, just as a river overflows its banks during heavy rainfall and expands its flow path.

Star ground forces the transient currents to stay within defined boundaries or follow a path of higher resistance until reaching the sensitive circuit area. When the current surge reaches the star ground, the higher resistance path has minimized the transient effect to a manageable level.

Figure 4-4 shows a star ground implementation. In this diagram, three major ground domains—analog, digital, and power—connect through a common point on a ground plane. The separation between the ground domains is selective cuts placed in the ground plane. Figure 4-4 shows the ground domains on one layer in a board design. This is just one method of implementing a star ground. The ground domains need not be on the same layer; they can be placed on different PCB layers with a single connection point placed to connect all ground domains.

Figure 4-4. Star Ground Connection

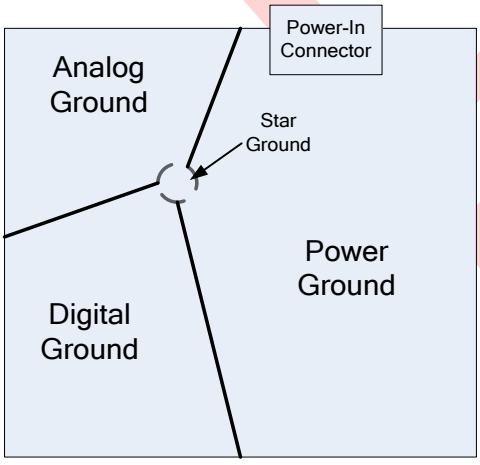
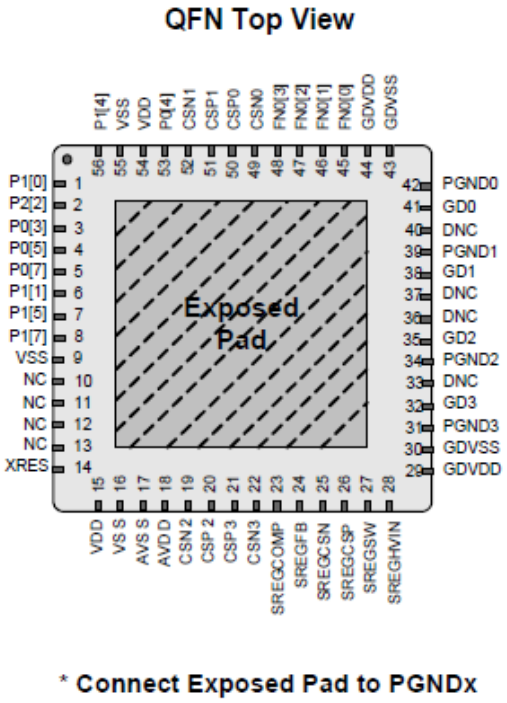


Figure 4-5 shows the footprint or land pattern of PowerPSoC. The large pad (EPAD) in the center is the thermal dissipation interface for PowerPSoC. The EPAD also connects to ground (die substrate) of PowerPSoC. Connect the EPAD to High-voltage ground (HVSS).

Figure 4-5. PowerPSoC Footprint on PCB



4.3 Decoupling Capacitors

Decoupling capacitors serve as localized sources of instantaneous power in a system. They provide immediate power until the main power supply can react. They also provide power during transient power demands. When selecting decoupling capacitors in a design, choose capacitors with the following parameters:

- X7R (or better) temperature coefficient,
- Ceramic or MLCC composition,
- Voltage rating above maximum expected,
- Low ESR and low ESL.

A good policy is to select the highest capacitance in the smallest package. Selecting the smallest ceramic or MLCC package minimizes the ESR and ESL properties for better decoupling performance.

The basic equations to calculate minimum decoupling capacitance required for a buck converter system operation are as follows. These can be suitably modified for other topologies by considering voltages across the inductor:

$$\text{Capacitance equation: } C = \frac{I \bullet dt}{dv} \qquad \text{Equation 22}$$

$$\text{Inductance equation: } dt = \frac{Ldi}{V_{HIGH} - V_{LOAD}} \qquad \text{Equation 23}$$

Where,

I = current

L = inductance

C = capacitance

V_{HIGH} = input voltage maximum

V_{LOAD} = load voltage

di = change in current or current ripple

dv = change in voltage or voltage ripple

dt = change in time

Equation 22 is the fundamental equation that describes the required capacitance (C) to keep the ripple (dv) within acceptable levels when instantaneous current (I) is supplied by the decoupling capacitor for a given duration (dt). In addition, normal duty cycle and frequency relationships are applicable as follows:

t_{on} = on time

t_{off} = off time

period = $t_{on} + t_{off}$

duty cycle = t_{on}/*period*

f = frequency = 1/*period*

Figure 4-6. Floating-buck LED Driver - Capacitance Selection

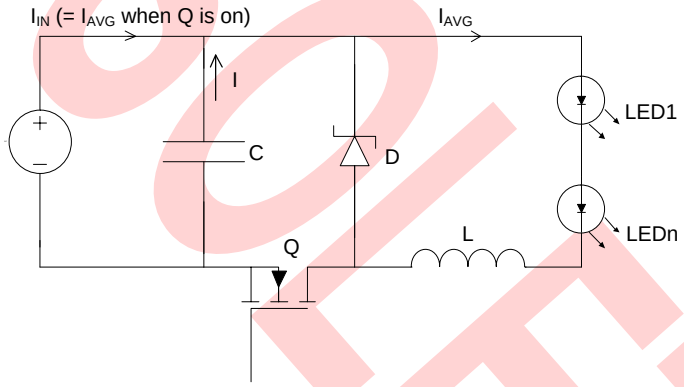


Figure 4-6 provides a schematic representation of the components and parameters involved in choosing a decoupling capacitor for the floating-buck LED driver.

The key components are the input decoupling capacitor (C), output inductor (L), switch (Q), and diode (D).

The key parameters are DC voltage (V_{HIGH}), load voltage (V_{LOAD}), V_{RIPPLE}, I_{RIPPLE}, I_{AVG}, I_{PK}, I, duty cycle, and inductor size.

- DC voltage (V_{HIGH}) is the maximum input supply level.
- Load voltage (V_{LOAD}) is the voltage developed across the LED string during operation at I_{AVG}.
- V_{RIPPLE} is the percent of change allowable for DC voltage. The decoupling capacitor is designed to meet this parameter (higher capacitance value leads to lower ripple).
- I_{RIPPLE} is the amount of ripple current allowed through the LED load, expressed as a percentage of average load current
- I_{AVG} is the average load current. It equals the supply current when the switch is closed. This parameter is used in calculations to determine steady state decoupling capacitance.
- I_{PK} is the peak current during a transient event or occurrence. I_{PK} is used when the concern is to stabilize power during a transient event. Use I_{PK} when the I_{AVG} is low, but high transient currents are expected, such as on GDVDD when driving external FETs.
- I is the current in the decoupling capacitor and is given by Equation 24.

$$I = I_{AVG} * I_{RIPPLE}$$ Equation 24

- Duty cycle is the ratio of 'time on' to total time for one switching period. For these calculations, maximum duty cycle is the parameter used, as it means the longest on time. For a buck converter, duty cycle is typically V_{LOAD}/V_{IN}.
    - Inductor size is the value of the inductor selected to set the switching frequency and load current.

The following six examples walk you through the parameters and calculations for decoupling capacitor selection. The capacitor calculation provides the minimum capacitance required to meet the system voltage, ripple current, frequency, and duty cycle parameters. During system design, insert the parameters for your system and recalculate for proper decoupling capacitor size.

4.3.1 High Voltage (Channel) Input Decoupling Example – No Dimming

This calculation is for one channel. Without dimming requirement, there are no abrupt changes in the load current, so the current demand from decoupling capacitor is moderate.

Intensity = 100%

High voltage = 32 V

Load voltage = 24 V

V_{RIPPLE} = 2%

I_{RIPPLE} = 30%

I_{AVG} = 1 A

Channel regulation frequency = 2 MHz

Duty cycle = 75%

Applying Equation 24:

$$I = 1A * 30\%$$

$$I = 0.3A$$

For the decoupling capacitor in Figure 4-6, dv is determined by the input voltage times the ripple and dt is determined by duty cycle times the switching period. Hence, applying Equation 22:

$$C_{channel} = \frac{0.3A(\frac{1}{2MHz})(0.75)}{(32 * 0.02)}$$

$$C_{channel} = \frac{0.3(500n)0.75}{0.64}$$

$$C_{channel} = \frac{112.5n}{0.64}$$

$$C_{channel} = 175.781\,\text{nF}$$

$$\text{Use standard value for C}$$

$$C_{channel} = 220\,\text{nF}$$

4.3.2 High Voltage (Channel) Input Decoupling Example – Dimming

When dimming is used, the LED current can transition from 0 to peak quickly. The rate of change is controlled by the inductor size and during the ramp-up time, the difference in current is supplied by the decoupling capacitor. This calculation is for one channel turning on (0 to I_{PEAK} current transition).

Inductor = 10 µH

High voltage = 32 V

Load voltage = 24 V

V_{RIPPLE} = 2%

I_{RIPPLE} = 30%

I_{AVG} = 1 A

The change in current during such transition is given by Equation 25:

$$di = I_{AVG} + \frac{(I_{AVG} * I_{RIPPLE})}{2}$$ Equation 25

Applying Equation 25 to the above example:

$$di = 1A + \frac{(1A * 30\%)}{2}$$

$$di = 1.15A$$

Next, applying Equation 23:

$$dt = \frac{10uH(1.15A)}{32V - 24V}$$

$$dt = \frac{11.5u}{8}$$

$$dt = 1.4375\,us$$

Finally, applying Equation 22:

$$C_{channel} = \frac{1.15A(1.4375us)}{(32V * 0.02)}$$

$$C_{channel} = \frac{1.6532u}{0.64}$$

$$C_{channel} = 2.584\,\text{uF}$$

$$\text{Use standard value for C}$$

$$C_{channel} = 3.3\,\text{uF}$$

Based on this result, it is apparent that the requirement for decoupling capacitor goes up more than 10-fold (from 220 nF to 3.3 µF) when dimming is taken into account.

4.3.3 High Voltage (SREG) Input Decoupling Example

Note The CY8CLED0xD/G0x datasheet recommends 1 µF input decoupling capacitance. The CY8CLED0xD/G0x characterization always uses a 1-µF input capacitor. This example shows how to calculate the SREG input capacitance if you decide not to follow the data sheet recommendations.

High voltage = 32 V

Output voltage = 5 V

V_{RIPPLE} = 2%

SREG output I_{AVG} = 0.25 A

SREG switching frequency = 1 MHz

SREG efficiency = 80% (worst case)

Duty cycle = 16%

$$SREG\ P_{IN} = \frac{SREG\ P_{OUT}}{efficiency} = \frac{250mA * 5V}{0.80} = 1.56W$$

$$SREG\ I_{IN} = \frac{SREG\ P_{in}}{High\ Voltage} = \frac{1.56W}{32V} = 49mA$$

Applying Equation 22:

$$C = \frac{49mA(\frac{1}{1MHz})(0.16)}{(32 * 0.02)}$$

$$C = \frac{49m(1u)0.16}{0.64}$$

$$C = \frac{7.84n}{0.64}$$

$$C = 12.25\,\text{nF}$$

$$\text{Use standard value for C}$$

$$C = 15\,\text{nF}$$

4.3.4 Gate Driver Input Decoupling Example

This calculation is for one channel.

Gate drive voltage = 5 V

V_{RIPPLE} = 2%

I_{AVG} = 0.1A, I_{PEAK} = 1 A

Transient current time = 20 ns

Applying equation 22:

$$C_{channel} = \frac{1A(20ns)}{(5 * 0.02)}$$

$$C_{channel} = \frac{20n}{0.1}$$

$$C_{channel} = 200\,\text{nF}$$

$$\text{Use standard value for C}$$

$$C_{channel} = 220\,\text{nF}$$

When decoupling for four channels, multiply the minimum capacitance value (200 nF in the previous calculation) by four (the number of channels), and then divide by the number of pins near the decoupling capacitors (two for PowerPSoC).

$$C = \frac{C_{channel} * channel}{pins}\ \text{per pin}$$

$$C = \frac{200n * 4}{2}$$

$$C = \frac{800n}{2}$$

$$C = 400\,\text{nF}$$

$$\text{Use standard value for C}$$

$$C = 470\,\text{nF per pin}$$

4.3.5 Digital Decoupling Example

VDD voltage = 5 V

V_{RIPPLE} = 2%

I_{AVG} = 50 mA (worst case)

PSoC frequency = 24 MHz

24 MHz duty cycle = 50%

Applying Equation 22:

$$C = \frac{0.05A(\frac{1}{24MHz})(0.5)}{(5*0.02)}$$

$$C = \frac{0.05(41.67n)0.5}{0.1}$$

$$C = \frac{0.05(20.83n)}{0.1}$$

$$C = \frac{1.0417n}{0.1}$$

$$C = 10.42\,\text{nF}$$

$$\text{Use standard value for C}$$

$$C = 15\,\text{nF}$$

When decoupling for the two PowerPSoC V_{DD} pins, divide the minimum capacitance value (10.42 nF in the previous calculation) by two (the number of V_{DD} pins).

$$C\ per\ pin = \frac{C}{pins}$$

$$C\ per\ pin = \frac{10.42n}{2}$$

$$C\ per\ pin = 5.21\,\text{nF}$$

$$\text{Use standard value for C}$$

$$C\ per\ pin = 6.8\,\text{nF}$$

4.3.6 Analog Decoupling Example

AVDD voltage = 5 V

V_{RIPPLE} = 2%

I_{AVG} = 25 mA (worst case)

PSoC frequency = 24 MHz

24 MHz duty cycle = 50%

Applying Equation 22:

$$C = \frac{0.025A(\frac{1}{24MHz})(0.5)}{(5*0.02)}$$

$$C = \frac{0.025(41.67n)0.5}{0.1}$$

$$C = \frac{0.025(20.83n)}{0.1}$$

$$C = \frac{0.521n}{0.1}$$

$$C = 5.21\,\text{nF}$$

$$\text{Use standard value for C}$$

$$C = 6.8\,\text{nF}$$

When placing the decoupling capacitors, follow the guidelines given in the PCB layout chapter of this document.

4.4 Ferrite Beads

The use of ferrite beads in effectively suppressing conducted EMI is the focus of this brief note. Using filters at the input and output sections of an EMI generating circuit is a simple approach to mitigating the problem.

The ferrite bead is a component that does the job of a low-cost filter. Ferrite beads are available as compact cylindrical ferrites wound with one or more loops of copper wire, or in more recent forms as chip inductors. Effectively, they are inductors with low Q factors, in contrast with air-cored coils (used in RF applications) which are high Q in nature. Although they possess stray capacitance, ferrite bead inductors exhibit resistive properties at high frequencies which attenuate EMI noise currents by dissipating their energy as heat. In PowerPSoC circuits, they are used to filter supply lines, the +5 V domains - VDD and AVDD.

Parameters to note while selecting ferrite beads are:

- Inductance
- Rated current, this is determined by the wire size or gauge used inside the inductor
- Saturation current, this is a function of the ferrite material – it is the current magnitude when flowing through the coil beyond which it is unable to set up any more magnetic flux in the ferrite
- DCR max, this is the maximum DC resistance of the coil, useful in determining winding or resistive losses
- Impedance over frequency, the impedance of a ferrite bead inductor tends to peak slightly and then roll off at high frequencies. This data is usually available in graphical form; you can choose an inductor whose impedance is still increasing over the frequency range of interest.

For PowerPSoC, the base frequency of concern is 24 MHz for VDD to AVDD and 2 MHz GDVDD to VDD and AVDD, (typical EMI spectrum is across 2 ranges: 150 kHz – 30 MHz for conducted emissions and 30 MHz – 3 GHz for radiated emissions).

For further reading:

- How to choose Ferrite components for EMI suppression: http://www.fair-rite.com/newfair/pdf/CUP%20Paper.pdf
- Understanding Ferrite bead inductors: http://www.murata.com/products/emc/knowhow/pdf/23to25e.pdf

4.5 Summary

This chapter provided detailed information and examples for PowerPSoC power, ground, and filtering. Information on power domains voltage and current, ground domains use and interconnect, and examples to determine decoupling capacitor values provide a thorough understanding of PowerPSoC requirements.

5. System Level ESD Considerations for a PowerPSoC® Based LED Driver

In the past, designers of lighting systems did not need to consider system-level ESD as incandescent and magnetically ballasted discharge lamps are robust by nature. Even discharge lamps with electronic ballasts, such as CFL lamps, provide adequate system level ESD performance. Much of their robustness comes from the use of a large glass envelope around the light source and a sealed plastic envelope around the drive electronics making it impossible for ESD events to reach the drive electronics.

With LED light sources, there is a need to keep the LEDs cool. This means attaching the LEDs to a large heat sink that is often part of the external surface of the lamp or fixture. This provides a direct path for system-level ESD events to enter the driver, and makes control circuitry that is directly connected to the LEDs particularly vulnerable to damage. When designing LED based lamps or fixtures, the designers must consider system level ESD.

The first step a designer must take is to review specs IEC61547 and IEC61000-4-2 and decide the level of the system's ESD performance required. During the design phase, it is important to include appropriate safeguards for system level ESD. After the design is complete, the finished system must be tested to ensure it meets the required system level ESD performance.

The following sections detail circuit and system level safe guards for a PowerPSoC based LED driver.

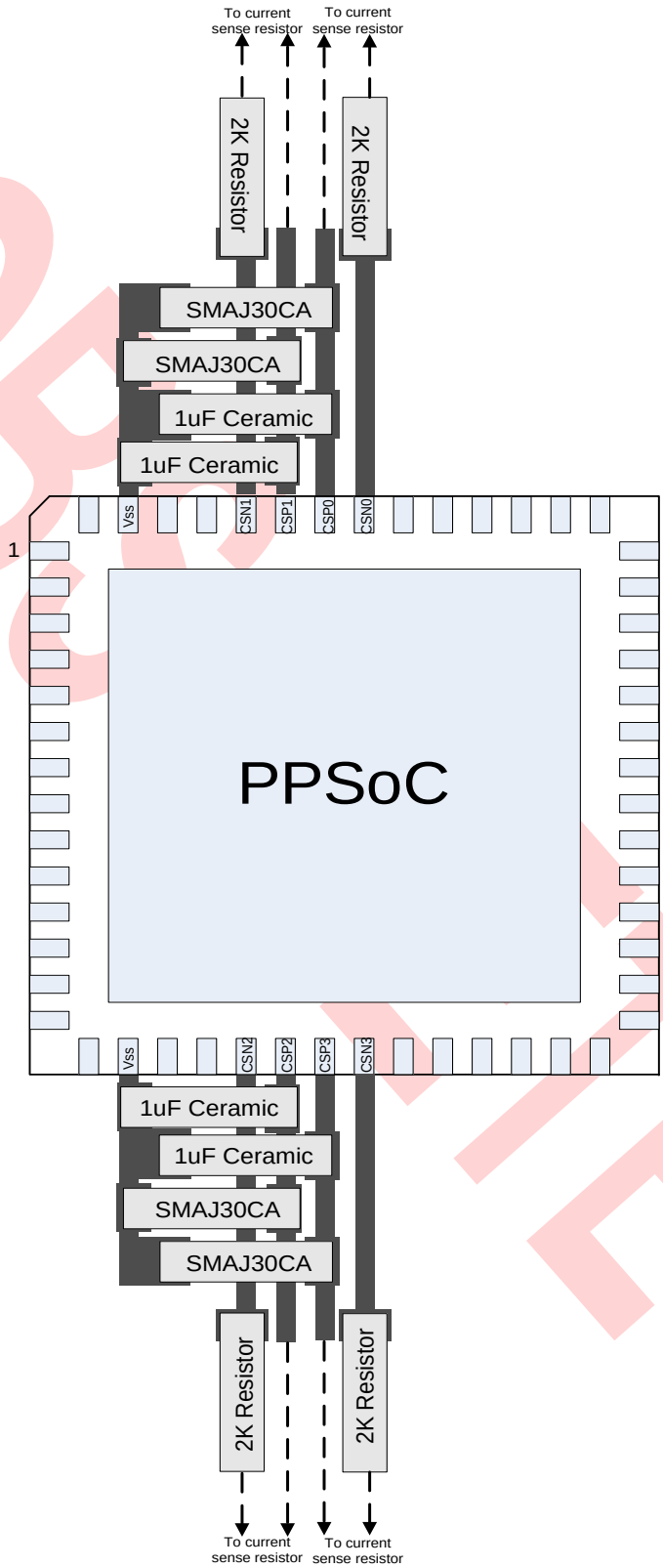
5.1 Circuit Level Improvements

System-level ESD events are large common mode events to the driver and should have little impact. However, the fast rise time of system-level ESD events and circuit imbalances allow some of this common mode signal to appear as a differential mode signal.

The main path for ESD voltage spikes to enter most LED based systems is through the LEDs themselves. These are often physically mounted to a heat sink that forms part of the external surface of the fixture. During a system-level ESD event, extremely fast voltage transients may couple to the LED+ and LED- nets. In PowerPSoC based solutions, if these voltage transients exceed the absolute maximum values given in its datasheet, damage may occur to the PowerPSoC device. To prevent such damage, two types of defense must be used.

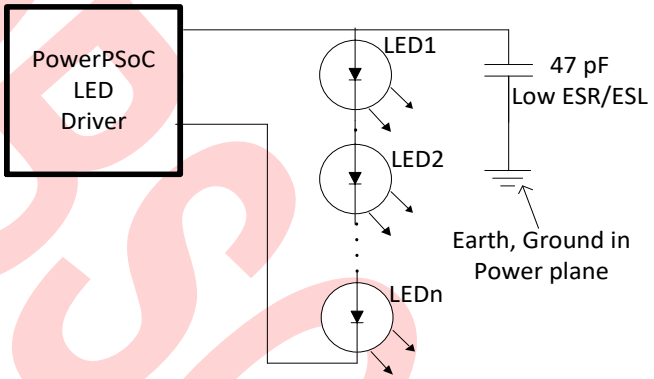
1. The first defense is at the PowerPSoC device itself. A low ESR/ESL capacitor and a TVS are required on sensitive pins to limit voltage spikes.
    a. One 1 µF ceramic capacitor and one SMAJ30CA TVS must be connected in parallel between each CSPx pin and the nearest V_{SS} pin.
    b. These components must be connected to the device pins with minimum series resistance and inductance.
    c. They must be placed on the same side of the PCB as the PowerPSoC device and located as close as possible to it. Traces must be as short and wide as possible with no vias.
    d. Connection of the capacitor and TVS to the CSPx trace must be part of the trace to the sense resistor, not a separate trace. See layout example shown in Figure 5-1.

Figure 5-1. Physical Locations for System-level ESD Components Around PowerPSoC Device



2. The second defense is at the interface between the LEDs and driver.
    a. Y-connected capacitors must be added from the LED leads to earth or, if earth is not available, to a ground or power plane.
    b. These capacitors shunt the voltages spikes on the LED leads to earth, ground, or a power plane and away from the PowerPSoC device pins.
    c. They must be connected as close to the LED connections as possible.
    d. Use a 47 pF low ESR/ESL capacitor from an LED string connecting to earth or ground/power plane. See Figure 5-2.

Figure 5-2. Using a Decoupling Cap to Steer ESD Away from PowerPSoC Pins



3. For systems that have long traces from the current sense resistor to the CSPx / CSNx pins, a resistor of at least 2 kΩ must be included in series with the CSNx pin. This resistor must be located at the PowerPSoC device's end of the trace, as shown in Figure 5-1.

Figure 5-1 illustrates the required components to provide the most robust system from ESD events. Another key task is to outline and identify the placement of the critical components before layout to reduce the risk of multiple board spins.

If system cost is critical then initial system level ESD tests may be done without any of the components populated. To improve such a system that does not meet system level ESD requirements, take a 2-step approach:

1. First, add all the capacitors and resistors, then
2. Add the TVS if performance needs to be further improved.

5.2 System Level Improvements

Two factors complicate system-level ESD performance:

1. Fixtures are typically comprised of many individual pieces of metal assembled using inexpensive manufacturing process,
2. Earth connections are often neglected

A proper fixture design can help reduce the need to populate some or all of the components mentioned in the previous section. The goal is to prevent the ESD voltage from coupling or arcing to any node or component in the driver circuitry. This can be achieved in several ways.

1. Using insulating surfaces:
    a. The most obvious, but usually less practical, method is to make all external surfaces insulating. If this method is used, the insulation material must have the necessary voltage rating, while being resistant to scratches, which can expose the underlying surface.
    b. A layer of paint, anodizing, or other surface treatments do not provide this level of protection.
    c. Care must also be taken to ensure there are no gaps, joins, or seams that might allow an ESD event to arc to any conducting surface on the driver.

2. Using metallic surfaces:
    a. For most systems, completely insulating all metal surfaces is not viable. In these cases, all metal objects in the fixture, such as heat sink and case, must be electrically bonded together and connected to earth to improve system ESD performance.
    b. It is important that the connections be low impedance, not just low ohmic connections. This means individual pieces of metal must be connected together using grounding braid or multiple nuts and bolts with star washers on both sides.
    c. While thin wire, screws, pop rivets, or bolts without washers may provide a low ohmic connection, they do not provide the low impedance necessary during ESD transients.
3. Using spacings:
    a. One last point to remember is that all insulating materials breakdown with sufficient electric field strength.
    b. For instance, air starts being conductive with field strength of about 3 kV/mm. This means appropriate gaps must be maintained between the external conductive surfaces and driver components, and the internal PCB traces.
    c. Do not expect solder resist or standard plastic coverings on components such as electrolytic capacitors to provide sufficient insulation.

5.3 Summary

Designers must consider system-level ESD at the beginning of the design of LED based lighting systems. Adding a few inexpensive components around a PowerPSoC device while ensuring proper fixture construction as outlined in this document leads to a final system with the most robust system-level ESD performance.

Revision History

Document Revision History

Document Title: AN52209 - CY8CLED0xx0x PowerPSoC® – Hardware Design Guidelines Document Number: 001-52209		
Revision	**Issue Date**	**Description of Change**
**	16/03/2009	New application note
*A	04/03/2009	Release to external website
*B	02/11/2011	Corrected grammar and typographic errors for easier understanding.
*C	06/28/2012	Converted Application Note to Design Guide. Updated content to integrate application notes AN53127, AN68806, and AN53781.
*D	03/28/2014	No technical updates. Completing Sunset Review.
*E	05/05/2015	Updated Template and Figure 5-1.
*F	03/18/2016	Updated section 3.6.10 Changed title to AN52209 - CY8CLED0xx0x PowerPSoC® – Hardware Design Guidelines
*G	02/02/2021	Obsolete this application notes as it uses obsolete Power PSoC part.