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Spec No: 001-14865

Spec Title: AN5093 - CYPRESS MOBL(R) DUAL-PORT  
100-BALL VFBGA PRINTED CIRCUIT  
BOARD (PCB) LAYOUT GUIDELINES

Replaced By: NONE

## AN5093

## Cypress MoBL® Dual-Port 100-Ball VFBGA Printed Circuit Board (PCB) Layout Guidelines

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**Associated Project:** No

**Associated Part Family:** NA

**Software Version:** NA

**Related Application Notes:** None

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MoBL® Dual-Port is a specialty memory product offered by Cypress Semiconductor targeted for handheld applications. It provides a flexible processor interconnect solution that is low-power and high-bandwidth.

### Introduction

The MoBL Dual-Port device is in a 6 × 6 mm, 100-ball VFBGA package that meets the needs of space-sensitive printed circuit board (PCB) designs. This application note provides guidelines for designing a PCB with a MoBL Dual-Port device.

### PCB Layout Terminology

This section defines common terms used in PCB layout design with the Cypress MoBL Dual-Port 100-ball VFBGA.

#### Escape Routing

Escape routing is the method used to route each signal from the package to another element(s) on the PCB.

#### Multi-Layer PCB

Multi-Layer PCB is an industry-standard method to allow escape routing for high pin count packages like BGAs. This is achieved by routing signals on various numbers of PCB layers.

#### Vias

Vias, or plated through holes, are used in multi-layer PCBs to electrically connect signals between layers. Common via types are: through via, blind via and embedded via. Through via interconnects signals between top and bottom layers including all inner layers of a multi-layer PCB. Blind via interconnects from top or bottom layer to an inner PCB layer. Embedded via interconnects between numbers of inner PCB layers.

#### Via Capture Pad

Vias are connected electrically to PCB layers through via capture pads that surround each via.

#### Micro-Vias

Micro-vias are defined by IPC-2315 and IPC-6012A standards, as vias that are equal to or less than 0.15 mm (6 mils) in diameter and have a target via capture pad equal to or less than 0.36 mm (14 mils).

#### Surface Land Pad

Surface land pads are the areas on the PCB to which the BGA solder balls adhere. The size of these pads affects the space available for vias and for the escape routing. In general, two different surface land pad designs are: non-solder mask defined (NSMD) and solder mask defined (SMD).

#### Non-Solder Mask Defined (NSMD) Pad

For NSMD pads, the solder mask opening is larger than the copper pad. The copper surface of the land pad is completely exposed, which provides greater area for the BGA solder ball to adhere.

#### Solder Mask Defined (SMD) Pad

For SMD pads, the solder mask overlaps the copper surface of the land pad. This overlapping provides greater adhesion strength between the copper pad and the PCB's epoxy/glass laminate, which can be important under extreme bending and during accelerated thermal cycling tests. However, the solder mask overlap reduces the copper surface area for the BGA solder ball adhesion.

## Stringer

Stringers are interconnect segments that electrically connect via capture pads and surface land pads.

## 100-ball VFBGA Package Overview

The MoBL Dual-Port is available in a 100-ball VFBGA package. Table 1 summarizes the critical dimensions used for the PCB layout design. Detailed package information is available in the device data sheet.

Table 1. MoBL® Dual-Port 100-ball VFBGA Dimensions

Parameter	Size
Package Size	6 × 6 × 1 mm
Ball Count	100 (10 × 10 Matrix)
Ball Pitch	0.50 mm
Ball Diameter	0.30 mm
Ball Pad Diameter	0.270 mm

## Layout Guidelines

For a typical PCB design for BGA packages, following factors are considered:

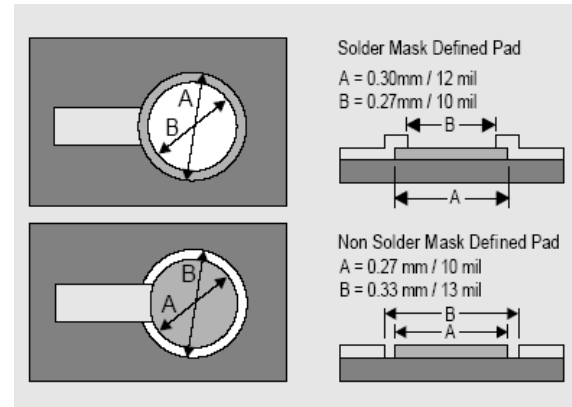
- Surface land pad dimension
- Via layout and dimension
- Signal-line space and trace width
- Escape routing

### Surface Land Pad Dimension

A 1:1 ratio between the package pad and PCB land pad joint area is desirable to balance the stress during temperature cycling. For an NSMD pad, it is necessary to have a clearance around the copper pad and the solder mask to account for mask registration tolerances (typically 0.060 mm to 0.075 mm) and to void any overlap between solder joint and the solder mask. In general, SMD pad is recommended for handheld applications because of its stronger pad adhesion that provides higher thermal and mechanical reliability.

Figure 1 summarizes the recommended dimensions of both SMD and NSMD pads for the PCB layout.

Figure 1. SMD and NSMD Pad Dimensions



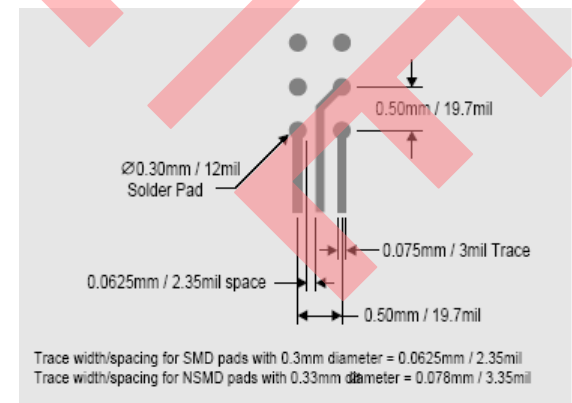
### Via Layout and Dimension

The size and layout of via and via capture pads affect the amount of space available for escape routing. For the MoBL Dual-Port, a micro-via in the center of the surface land pad (via-in-pad technology) is recommended. The micro-via drill hole diameter should be equal to or less than 0.150 mm (6 mils). The drill hole should be plugged and planarized to create a flat surface. This prevents solder from wicking through the holes during the assembly process.

### Signal Line Space and Trace Width

The ability to perform escape routing is defined by the width of the trace and the minimum space required between traces. For the MoBL Dual-Port, a 0.075-mm (3-mil) trace is preferable. Only one trace can be routed between surface land pads or via capture pads. Recommended line space and trace width are illustrated in Figure 2.

Figure 2. Line Space and Trace Width for SMD Pads



The three-mil trace is only applicable to BGA area that has routing space constraints. To increase manufacturability of the PCB and ensure better yields, necking down traces can be used. As illustrated in Figure 3, once the trace exits the BGA pads, standard trace and space geometry can be used.

Figure 3. Necking Down Traces

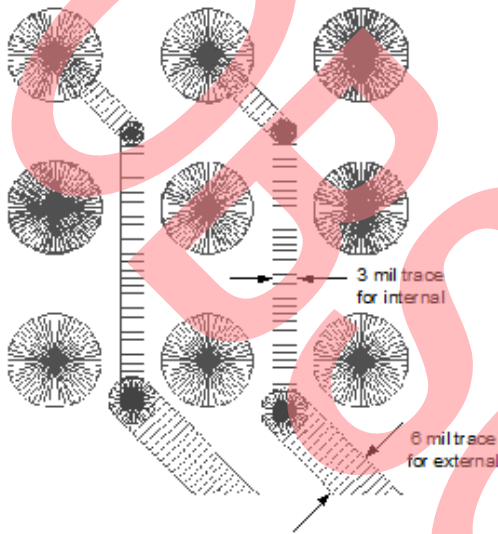
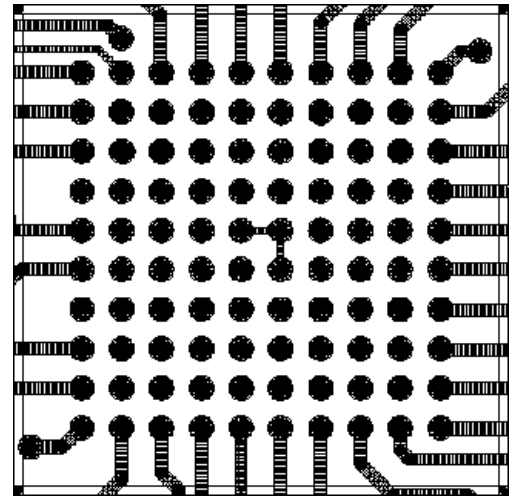


Figure 4. First Signal Layer



Signals in row two and up can be routed on two other signal layers as shown in Figure 5 and Figure 6. These signals require via-in-pads. Signals in row two can use standard 0.15-mm (6-mil) trace because row one is not present in these two signal layers. However, signals in rows three to five require 0.075-mm (3-mil) traces to route between via capture pads and escape from the BGA area. Again once signals leave the BGA area, standard 0.15-mm (6-mil) trace can be used.

## Escape Routing

The MoBL Dual-Port has five rows of solder balls counted from the outer most row towards the center of the package. This requires a minimum of three signal layers for escape routing.

For row one (outer most row) as shown in Figure 4, the signal can be directly accessed on signal layer one. Standard trace width of 0.15 mm (6 mils) can be used. Via-in-pads are not needed.

Figure 5. Second Signal Layer

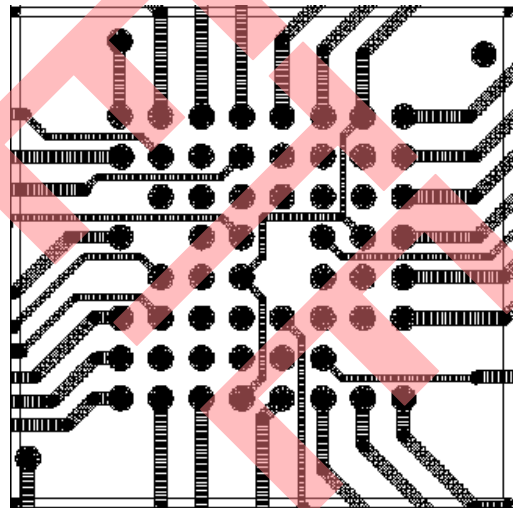
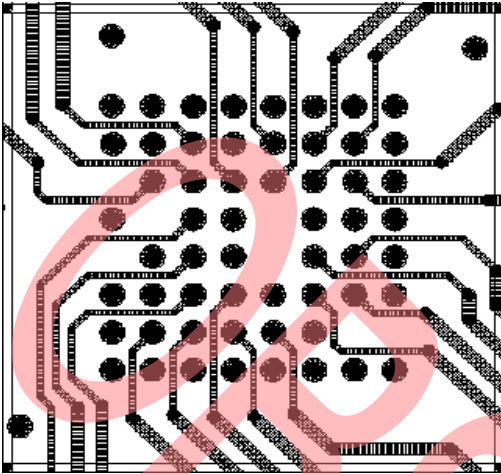


Figure 6. Third Signal Layer



## References

Cypress Semiconductor, CYDM256B16, CYDM128B16, CYDM064B16, CYDM128B08, CYDM064B08, 1.8 V, 2.5 V, 3.3 V 4K/8K/16K x 16 and 8K/16K x 8 MoBL® Dual-Port Static RAM Data Sheet, September 2005

Larry W. Burgess & Paul D. Madden, Designing and Fabricating Multi-Depth Via-in-Pad PCBs, IPC Printed Circuits Expo, April 1998

Yuan Li, Anil Pannikkat, Larry Anderson, Tarun Verma, Bruce Euzent, Building Reliability Into Full-Array BGAs, 26th IEMT Symposium, December 2000

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## Summary

High-density PCB with the MoBL Dual Port's 100-ball VFBGA package can be manufactured with high yields if the necessary process controls or monitors are in place. Recommendations of this documentation will help ensure a higher degree of success in the manufacture of assemblies that contain the MoBL Dual-Port device.

## Document History

Document Title: AN5093 - Cypress MoBL® Dual-Port 100-Ball VFBGA Printed Circuit Board (PCB) Layout Guidelines

Document Number: 001-14865

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	993800	HKH	04/19/2007	Existing Application Note in the web - Added Spec No. and new disclaimer and also updated the copyright date. Please post in the web - overwrite the existing AN5093 file.
*A	3246116	HKH	05/02/2011	Updated to new template.
*B	4396229	RAJV	06/02/2014	Updated to new template. Completing Sunset Review.
*C	5848922	RAJV	08/09/2017	Obsolete document. Completing Sunset Review.



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