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Spec No: 001-14805

Spec Title: MIGRATING FROM CYPRESS  
CYDMXXXAXX MOBL(R) DUAL-PORTS TO  
CYDMXXXBXX MOBL DUAL-PORTS -  
AN5075

Sunset Owner: Veerappan Rajaram (RAJV)

Replaced By: None

## AN5075

## Migrating from Cypress CYDMxxxAxx MoBL<sup>®</sup> Dual-Ports to CYDMxxxBxx MoBL Dual-Ports

**Author: Hingkwon Huen****Associated Project: No****Associated Part Family: NA****Software Version: NA****Related Application Notes: None**

To get the latest version of this application note, or the associated project file, please visit <http://www.cypress.com/go/AN5075>.

The Cypress CYDMxxxAxx and CYDMxxxBxx MoBL<sup>®</sup> Dual-Ports are high-speed, low-power interconnects that provide two independent ports with simultaneous read/write access to the shared memory core. Both devices have full asynchronous operation and on-chip arbitration logic. The devices also offer features such as the Input Read Registers (IRR) and Output Drive Registers (ODR).

### Introduction

For the CYDMxxxAxx MoBL Dual-Ports, the user supplies a single VCC for both the core voltage and I/O operations, while the CYDMxxxBxx MoBL Dual-Ports support independent core and I/O voltages. That is, the core of the CYDMxxxBxx MoBL Dual-Port can be at a voltage level that is lower than or equal to the I/O voltages, which offers greater power savings. Additionally, the two ports can be connected to buses working at different voltages, thus avoiding the need for level shifters. There are three sets of power pins in the CYDMxxxBxx MoBL Dual-Ports: V<sub>DDIOL</sub>, V<sub>DDIOR</sub>, and V<sub>CC</sub>.

### Compatibility Guidelines

To migrate a design that currently implements the Cypress CYDMxxxAxx MoBL Dual-Port to CYDMxxxBxx MoBL Dual-Port, simply connect the three sets of power pins (V<sub>DDIOL</sub>, V<sub>DDIOR</sub> and V<sub>CC</sub>) on the CYDMxxxBxx MoBL Dual-Port to the voltage supply that is connected to the V<sub>CC</sub> on the CYDMxxxAxx MoBL Dual-Port. Therefore, in terms of voltage supplies, the new CYDMxxxBxx MoBL Dual-Ports are drop-in replacements of the original CYDMxxxAxx MoBL Dual-Ports.

Another improvement between the two revisions of MoBL Dual-Port is the IRR feature. This difference only applies to the CYDM256A16, CYDM256B16, CYDM128A08 and CYDM128B08 devices. For CYDM256A16 and CYDM128A08, both IRR and ODR features are unavailable. That is, for these two devices, SFEN can be tied to V<sub>CC</sub>. On the new CYDM256B16 and CYDM128B08, only the IRR is unavailable (for A13L and A13R), while the ODRs can still be accessed. That is, in order to plan for migration and take advantage of the ODR feature on the new CYDM256B16 and CYDM128B08 MoBL Dual-Ports, the SFEN pin should not be tied to V<sub>CC</sub>, but driven by the processing element. This gives the flexibility to enable ODRs after the migration happens. Table 1 lists the signal equivalents of the CYDMxxxAxx and CYDMxxxBxx MoBL Dual-Ports.

Table 1. CYDMxxxAxx and CYDMxxxBxx MoBL Dual-Port Signal Equivalents

CYDMxxxAxx Signals	CYDMxxxBxx Signals	Function
$\overline{CE}$	$\overline{CE}$	Chip Enable
R/ $\overline{W}$	R/ $\overline{W}$	Read Write Enable
$\overline{OE}$	$\overline{OE}$	Output Enable
A[13:0]	A[13:0]	Address
I/O[15:0]	I/O[15:0]	Data
$\overline{SEM}$	$\overline{SEM}$	Semaphore Enable
$\overline{UB}$	$\overline{UB}$	Upper Byte Select
$\overline{LB}$	$\overline{LB}$	Lower Byte Select
$\overline{INT}$	$\overline{INT}$	Interrupt Flag
$\overline{BUSY}$	$\overline{BUSY}$	Busy Flag
IRR[1:0]	IRR[1:0]	Input Read Registers
ODRR[4:0]	ODRR[4:0]	Output Drive Registers
$\overline{SFEN}$	$\overline{SFEN}$	Special Function Enable
M/ $\overline{S}$	M/ $\overline{S}$	Master/Slave Select
V <sub>CC</sub>	V <sub>CC</sub>	Core Power
V <sub>CC</sub>	V <sub>DDIOL</sub>	Left Port I/O Voltage
V <sub>CC</sub>	V <sub>DDIOR</sub>	Right Port I/O Voltage
GND	GND	Ground
NC	NC	No Connect

## Summary

The Cypress CYDMxxxBxx MoBL Dual-Port SRAMs are drop-in replacements of the CYDMxxxAxx MoBL Dual-Ports. Migration enables more features and flexibility, as the CYDMxxxBxx MoBL Dual-Ports offer both ODR feature in the highest density devices, as well as independent voltages in the memory core and the two I/O ports.

## References

Cypress Semiconductor, 1.8 V 4K/8K/16K x 16 and 8K/16K x 8 MoBL Dual-Port Static RAM Data Sheet, May 2005.

Cypress Semiconductor, 1.8 V 4K/8K/16K x 16 and 8K/16K x 8 Split-Voltage MoBL Dual-Port Static RAM Data Sheet, May 2005.

## About the Author

Name: Hingkwan Huen.

## Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	989800	HKH	04/18/2007	Existing Application Note in the web - Added Spec No. and new disclaimer and also updated the copyright date Please post in the web- overwrite the existing AN5075 file
*A	3246100	HKH	05/02/2011	Updated in new template.
*B	4396111	RAJV	06/02/2014	Updated in new template. Completing Sunset Review.
*C	4460946	RSKV	07/30/2014	Obsolete document.

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