THIS SPEC IS OBSOLETE

Spec No: 001-50741

Spec Title: ISSUES IN GANGING HSB PINS ON CY14B104L/CY14B104N

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Issues in Ganging $\overline{HSB}$ Pins on CY14B104L/CY14B104N

AN50741

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Application Note Abstract

This application note discusses potential issues that occur when ganging $\overline{HSB}$ pins of multiple CY14B104L and CY14B104N devices.

Introduction

Applications may use multiple CY14B104L and CY14B104N devices to increase memory width. In doing so, it may seem appropriate to connect the $\overline{HSB}$ (Hardware Store Busy) pins of these devices so that the MCU issues a single signal to initiate Hardware Store in all nvSRAMs. However, this ganging of $\overline{HSB}$ pins can cause them to be indefinitely held LOW due to the variations in the STORE/RECALL timing of individual nvSRAM devices. Hence, the $\overline{HSB}$ pins fail to switch HIGH after completion of the nonvolatile operation and inhibit memory Read and Write operations. For this reason, it is recommended that each $\overline{HSB}$ pin be connected to separate controller I/Os.

$\overline{HSB}$ Pin

The $\overline{HSB}$ pin of nvSRAM is an I/O pin used to signal a STORE/RECALL cycle in progress or initiate a hardware store operation. When a STORE/RECALL operation is in progress, the $\overline{HSB}$ pin is driven LOW by the device and all reads and writes are inhibited. When no STORE/RECALL operation is in progress, the $\overline{HSB}$ pin acts similar to an open drain pin pulled up by a weak internal pull up. The pin can then be driven LOW externally to initiate a conditional Hardware Store operation. If at least one write is performed since the last STORE/RECALL operation, a Hardware Store is initiated and the HSB output becomes active (LOW) for t_{STORE} duration. However, even if no Hardware Store is initiated, the HSB pin output becomes active and keeps the pin LOW for t_{DELAY} duration.

If the Hardware Store Busy feature is not used, it is recommended to leave the $\overline{HSB}$ pin open. Refer to the product data sheet for more information.

Variation in t_{STORE} Duration

The $\overline{HSB}$ pin is pulled LOW internally for t_{STORE} duration to indicate a STORE operation. However, due to process variations, the t_{STORE} parameter can vary between devices. This implies that the $\overline{HSB}$ may be pulled LOW for slightly varying times in two different devices. Due to the output behavior of $\overline{HSB}$, this may cause an issue when $\overline{HSB}$ pins of multiple devices are tied together.

To understand this issue, consider two CY14B104L devices 'A' and 'B', with the $\overline{HSB}$ pins tied together. There are two possible cases as illustrated in Figure 1 and Figure 2:

Figure 1. Store Cycles in Both nvSRAMs are Identical

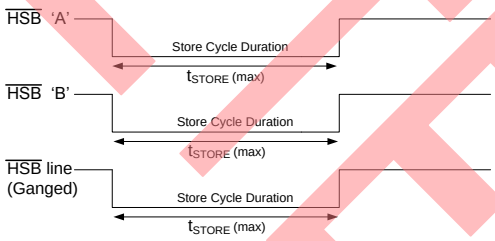
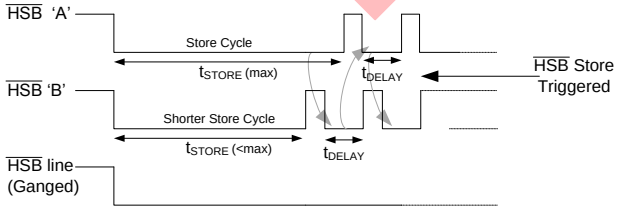


Figure 2. Store Cycle in One of the nvSRAMs is Shorter



Case 1: Equal Store Cycle Duration

If the store cycles in both devices are identical (Figure 1), ganging the $\overline{HSB}$ pins together does not cause any problems. The equal t_{STORE} ensures that both $\overline{HSB}$ pins are pulled HIGH by the devices simultaneously.

Case 2: Unequal Store Cycle Duration

When store cycle durations of the two devices are not equal, they may go in an infinite loop causing the $\overline{HSB}$ line to be held LOW. In the example shown in Figure 2, the device 'B' has a shorter STORE cycle and hence releases its $\overline{HSB}$ pin before device 'A'. As the $\overline{HSB}$ line is being pulled LOW by 'A', it causes the device 'B' to see a LOW signal on its $\overline{HSB}$ pin and initiate a Hardware Store cycle. Though device 'B' does not perform a new STORE operation because no Write has happened since the last STORE, the $\overline{HSB}$ line is internally held LOW for t_{DELAY} duration. When device 'A' completes its STORE cycle, the $\overline{HSB}$ line is held LOW by device 'B' and may trigger another Hardware STORE cycle in 'A'. This sequence can repeat indefinitely and causes the devices to go in a loop with the $\overline{HSB}$ pin held LOW infinitely. This inhibits all normal Read or Write operations.

This example shows only two devices, but the same phenomenon is valid even for more than two nvSRAM devices with ganged $\overline{HSB}$ pin. This issue hampers the normal operation of nvSRAM and therefore, ganging of $\overline{HSB}$ must be avoided.

Summary

Ganging $\overline{HSB}$ pins when using multiple CY14B104L and CY14B104N devices on the same board is not recommended. However, the future die revisions of this device will allow this option. If you wish to use 4 Mbit nvSRAMs with ganged $\overline{HSB}$ pins, design your boards for the devices - CY14B104LA and CY14B104NA.

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2624476	GSIN	12/18/08	New application note
*A	3249443	GVCH	05/05/11	Obsolete spec: Product pruned

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