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Spec No: 001-66418

Spec Title: AN5072 - ATA BUS SHARING WITH THE EZ-USB(R) AT2LP(TM)

Sunset Owner: RAMA SAI KRISHNA VAKKANTULA (RSKV)

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# ATA Bus Sharing with the EZ-USB® AT2LP™

## AN5072

**Author**: Narayana Murthy M
**Associated Project**: No
**Associated Part Family**: CY7C68300C/301C/320C/321C
**Software Version**: None
**Associated Application Notes**: None



## Application Note Abstract

This application note explains how to share the ATA Bus when using AT2LP™. There are various factors to be considered while tristating the ATA bus in a shared BUS design and they are discussed in detail here.

## Introduction

The chips in the EZ-USB® AT2LP family (which includes part numbers CY7C68300C, CY7C68301C, CY7C68320C, and CY7C68321C), have built-in functionality that allows them to set their ATA interface pins in a high-impedance state so that another ATA master can control the bus. This allows the AT2LP to be used in any system with more than one controller connected to the ATA bus, such as a USB/1394 storage device or USB-enabled multi-media player.

The purpose of this application note is to give an overview of the features available in the AT2LP that allow for ATA bus sharing, and to give recommendations for properly implementing a shared bus design[1].

## Implementation

To properly implement a shared bus, it is essential that only one master device have control of the ATA bus at any time. The AT2LP can tristate its ATA interface pins to effectively remove itself from the ATA bus. When the ATA pins are tristated, the secondary master can have full control over the ATA bus without interference from the AT2LP.

This feature is not intended to be used to dynamically share the bus (for example, USB and FireWire™ operating at the same time). Instead, it should be used to select either the AT2LP or the secondary master under controlled circumstances, such as at power-up.

### VBUS_ATA_ENABLE

The VBUS_ATA_ENABLE pin is used to detect the presence of VBUS, and can also control the state of the AT2LP's ATA interface during chip suspend. Bit 4 of EEPROM address 0x08 defines whether or not the ATA interface pins are disabled (placed in high-Z) whenever VBUS_ATA_ENABLE is set to '0'. When this ATA_EN feature is not enabled, the ATA bus is driven by the AT2LP even when VBUS_ATA_ENABLE is not asserted.

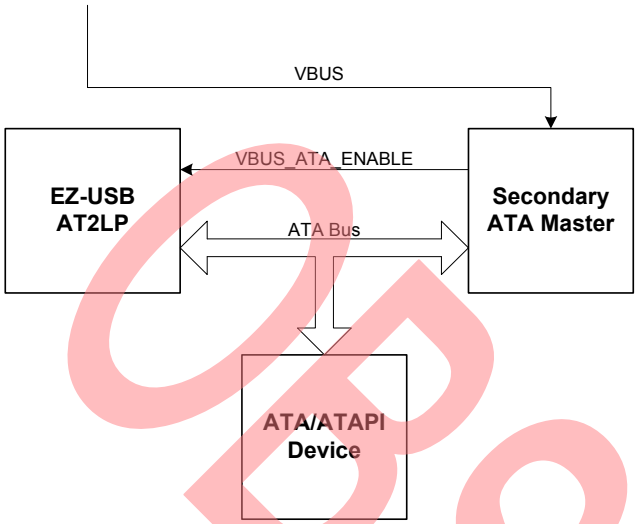
Setting VBUS_ATA_ENABLE to '1' enables the ATA interface for normal operation. Following a '1' to '0' transition on the VBUS_ATA_ENABLE pin (assuming that the ATA_EN feature is enabled), all ATA signals are tristated, the USB interface is disconnected, and the AT2LP enters a low-power state until the chip is reset or the VBUS_ATA_ENABLE pin transitions back to a '1' state.

If a '0' to '1' transition is detected and the chip is not in suspend for another reason, the AT2LP will return to a post-reset operational state and will reconnect to the USB. If the AT2LP is already in suspend for another reason during a '1' to '0' or '0' to '1' VBUS_ATA_ENABLE transition, the AT2LP will resume operation only long enough to set the ATA bus accordingly. The VBUS_ATA_ENABLE pin is sampled at a rate of 60 times per second by the AT2LP's internal logic.

The most common method for implementing the AT2LP in a shared bus environment is to have the secondary master hold VBUS_ATA_ENABLE to '0' unless +5 V is detected on the VBUS signal. When VBUS is detected, the secondary master should remove itself from the ATA bus and set VBUS_ATA_ENABLE to '1'. When VBUS is removed, either by unplugging the USB cable or shutting down the host, the secondary master can regain control of the ATA bus by setting VBUS_ATA_ENABLE to '0' again. Additionally, the secondary master may set VBUS_ATA_ENABLE to '0' at any time to remove the AT2LP from the USB, although this unsafe removal method is not recommended[2].

**Notes**
1. For clarification within this document, any device that shares the ATA bus with the AT2LP is referred to as the "secondary master."
2. Enabling or disabling the ATA interface pins during a data transfer may result in data loss, and can cause the host computer's OS to become unstable.

Figure 1. Block Diagram of a Shared Bus Design




### EEPROM Bits

If problems are encountered when the AT2LP resumes normal ATA bus operation, the features controlled by EEPROM addresses 0x05, 0x08, and 0x0E may help to correct the issue. Refer to the AT2LP datasheet for more information on these features. No other changes should be required.

## Power Considerations for the AT2LP

Depending upon the source of the device's power, certain design characteristics may be necessary to ensure that power is not consumed needlessly. Battery-powered designs are especially sensitive to power consumption, while self-powered designs may not be. Also, because of the many possible means of detecting VBUS, special care must be taken to ensure that the design does not violate the USB specification.

### Battery-powered Designs

Battery-powered applications that use the AT2LP, such as a portable MP3 player, will require that special attention be paid to the power control of the AT2LP. The AT2LP supports a low-power standby state that consumes a minimum of power when it is not in use. Cypress offers the CY7C68301C and CY7C68321C for battery-powered designs. The power consumption during chip suspend is lower in these parts, as compared to the CY7C68300C and CY7C68320C, to ensure that a minimum of power is consumed. Because leakage in the I/O cells may occur when no power is applied to the chip, removing power from the AT2LP to share the ATA bus is not recommended.

### Self-powered Designs

Applications that power the AT2LP from a source other than batteries or VBUS (such as an external wall outlet adapter), do not require any special power considerations unless a reduction in total current consumption is desired. In such a case, the same methods suggested for battery-powered designs may be utilized.

### VBUS-powered Designs

The AT2LP is fully compliant with the USB specifications for bus-powered operation. It also provides control signals to help ensure that the total design meets the bus-powered requirements. However, because the AT2LP is not active on the USB when VBUS_ATA_ENABLE is not asserted, it is not recommended that a shared-bus design be powered from VBUS.

### Other Power Considerations

Proper care should be taken to ensure that the shared bus design does not draw excessive current from VBUS. Care should also be taken to ensure that no power is applied to VBUS by the device, since only the USB host is allowed to power the bus.

Also, if an RC reset circuit is used for the AT2LP in a bus-sharing setup, the circuit's capacitor may become charged due to back-powering from the secondary master's ATA signals. Care should be taken to ensure that the capacitor is drained prior to AT2LP operation. If the capacitor is not drained when the AT2LP is powered up, a proper reset may never occur.

## Additional Resources

Visit Cypress website for the additional resources and further information:

- EZ-USB AT2LP datasheet
- Cypress Support Contact Information
- USB Specification Version 2.0

## Document History

**Document Title: AN5072 - ATA Bus Sharing with the EZ-USB® AT2LP™**
**Document Number: 001-66418**

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 3129937 | NMMA | 01/06/2011 | Created spec # for the note to be added to the spec system.<br>Added copyright details. |
| *A | 4194639 | RSKV | 11/18/2013 | Obsolete document.<br>Completing Sunset Review. |





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