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Spec No: 001-15288

Spec Title: AN5071 - EZ-USB(R) AT2LP FEATURES

Sunset Owner: Rich Peng (LIP)

Replaced By: NONE

EZ-USB® AT2LP Features

AN5071

Associated Project: No
Associated Part Family: CY7C683xx
Software Version: NA
Associated Application Notes: None

Abstract

The EZ-USB® AT2LP is a fixed-function, high-speed USB-to-ATA/ATAPI bridge. The AT2LP enhances the functionality of the AT2 family while minimizing the effect on existing designs that migrate to the AT2LP. This application note describes the features in the AT2LP that are new to the AT2 family of chips, as well as any features that may behave differently than with the previous AT2 chips.

Overview

Major items discussed in this application note include:

- Part Numbers and Package Options
- CY7C6830XC Backward Compatibility Mode
- Easier Method of Forcing Board Manufacturing Mode
- Low-Power Operation
- Compact Flash Support
- Multiple Drive Support
- GPIO Pins
- HID Interface Using GPIO Pins
- Digital Rights Management Compatibility

Details

Part Numbers and Package Options

The AT2LP family includes four different part numbers and three different package types. This allows Cypress to provide the right package options to meet our customers' various design needs. The CY7C68300C, CY7C68301C, CY7C68320, and CY7C68321 are all referred to as AT2LP, but they have slightly different pinouts and functionality.

For the purposes of this document, the CY7C68300C and CY7C68301C are hereafter referred to together as CY7C6830XC, while the CY7C68320 and CY7C68321 are referred to as CY7C6832X. The only difference between the "one-off" part numbers is in the amount of power consumed during suspend states. The greater of the two similar part numbers indicates silicon with a lower suspend current for use in battery-powered applications. All parts are now only available in lead-free packages.

The CY7C6830XC is available in 56-pin SSOP or QFN packages. It can accommodate all existing AT2 designs by utilizing Backward Compatibility Mode, or it can be configured to provide additional control signals and functionality not present in the previous AT2.

The CY7C6832X is available in either a 56-pin QFN or 100-pin TQFP. The 56-pin QFN package provides two standard GPIO pins, and three control pins with an alternate input-only HID setting. The 100-pin TQFP provides six standard GPIO pins and the ability to dynamically report as either bus- or self-powered.

Detailed descriptions of pinouts and individual pin functions are found in the AT2LP data sheet. Also, an additional description of the Backward Compatibility Mode and GPIO functionalities are described later in this application note.

CY7C6830XC Backward Compatibility Mode

The CY7C6830XC features a backward compatibility mode, which allows it to be a drop-in replacement for the AT2. During start-up, the AT2LP checks the I^2C bus for an EEPROM with a valid signature in the first two bytes. If the signature is 0x4D4D, the AT2LP configures itself for backward compatibility mode and begins normal mass storage operation. Because this signature is the same as what was required for the AT2, no changes to the EEPROM file are necessary when migrating from the AT2 to the AT2LP.

If no valid signature is found, the AT2LP enters board manufacturing test mode, which will allow the EEPROM to be programmed using the Cypress AT2LP manufacturing software. The valid EEPROM configuration bits for the AT2LP modes are described in the data sheet.

Easier Method of Forcing Board Manufacturing Mode

A simple way to force the chip into manufacturing mode has been added to the AT2LP to help speed up the development and testing process. Simply setting ARESET# to LOW at power-up will cause the AT2LP to start up in manufacturing mode. The easiest way to accomplish this using the AT2LP development board from Cypress is to remove any drives that are connected to the AT2LP and short pins 1 and 3 on the 40-pin ATA connector.

The most common method for putting the old AT2 into manufacturing mode was to disable the EEPROM at start-up, causing the AT2 to use the default descriptors contained in ROM space. The AT2LP supports the option of fusing some configuration data during factory manufacturing, so it will read the fuse area of memory if no EEPROM is detected at startup. The fuse area contains all zeros when the fuse option is not utilized, which will result in the AT2LP returning invalid configuration data when no EEPROM is present. Because of this, disabling the EEPROM on an AT2LP to force manufacturing mode is not recommended. Using a blank EEPROM will result in proper manufacturing mode operation.

Low-Power Operation

The AT2LP meets all USB bus-powered requirements for unconfigured current (100 mA) and suspend current (500 μA). The 56-pin packages use the bMaxPower value from the USB descriptors stored in the EEPROM to determine whether the device reports as self- or bus-powered. The 100-pin package uses the VBUSPWRD input pin to determine what state it reports to the host in the descriptors. Because all contemporary operating systems only check for this information once at enumeration, a change in power state will likely only be detected after a new USB enumeration is performed.

Because the AT2LP meets all bus-powered requirements, a design that utilized the drive power management features in the AT2 may now be able to qualify for bus-powered certification by simply replacing the AT2 with and AT2LP.

Compact Flash Support

The AT2LP adds support for devices that use the Compact Flash interface and support true IDE mode. This support is present in both the CY7C6830XC and CY7C6832X, regardless of its pinout or operating mode.

Because some CF devices may interfere with UDMA communication, the AT2LP can disable UDMA support for removable-media devices. Bit 3 of byte 0x0E in the EEPROM controls whether or not UDMA is to be used for removable-media devices.

Multiple Drive Support

The AT2LP supports a combination of drive configurations using the standard IDE master/slave scheme:

- 1 or 2 ATA
- 1 or 2 ATAPI
- 1 ATA + 1 ATAPI
- 1 CF
- 1 CF + 1 ATA
- 1 CF + 1 ATAPI

Note When using a CF device, the CF is always master and the ATA or ATAPI device must be set as the slave.

The number of supported devices can be fixed in the EEPROM or discovered by the AT2LP. Bits 2 and 1 in configuration byte 0x0E determine the number of attached devices assumed to be on the bus. If bit 2 is set, the AT2LP will assume that two devices are present on the bus. If only bit 1 is set, one device is assumed to be alone on the bus. If neither bit 1 nor bit 2 are set, the AT2LP will search the ATA/CF bus to detect the presence of devices.

In addition to this feature, setting bit 0 of byte 0x0E to '1' causes the AT2LP to search the IDE bus for the presence of devices each time VBUS is asserted on the VBUS detection pin. This feature allows the AT2LP to be used in designs that may incorporate removable drive bays or similar schemes. Refer to the Multiple IDE Drives Access Using AT2LP - AN63019.

GPIO Pins

The CY7C6832X supports two GPIO pins in the 56-pin package, and six GPIO pins in the 100-pin package. The individual GPIO pins can be configured as either outputs or high-impedance inputs, according to the value of byte 0x09 of the EEPROM configuration data. If configured as outputs, the state of the GPIO pins is determined by the value of byte 0x0A in the EEPROM configuration data.

Using Cypress's mass storage driver, or any driver that supports the vendor-specific commands for the AT2LP, the state of the GPIO pins can be read and controlled dynamically. The 100-pin package also provides the SYSIRQ pin, which will cause the AT2LP to return the current state of the GPIO pins to the driver through the interrupt pipe. This data can then be used by software to add extra functionality to a design.

The GPIO pins can also be configured as HID inputs, as described in the following section.

HID Interface Using GPIO Pins

If bit 7 of byte 0x08 in the CY7C6802X's EEPROM is set to a '1', the AT2LP reports itself as a composite device with both HID and mass storage interfaces. In this mode the mass storage functionality remains unchanged, but the GPIO pins are all configured as inputs and are utilized by the HID logic. A state change on any GPIO pin results in HID data being returned to the host.

In HID mode, both the mass storage and HID interfaces are compatible with native USB class drivers found in modern operating systems. Developers can use the standard driver interfaces to utilize the HID data as desired to add even more functionality to their design. More information on HID implementation is available in the AT2LP data sheet.

Digital Rights Management Compatibility

Several different methods for implementing digital rights management (DRM) are used today. The AT2LP has added features to support two of the most common methods: support for ATAPI serial number vital product data (VPD) page retrieval commands and an optional content security management (CSM) interface.

If a CSM interface is present in the USB descriptors, support for it will automatically be enabled in the AT2LP. Cypress recommends that developers wishing to implement a CSM interface use Cypress's AT2LP Blaster software, included in the CY4615B reference design kit, to configure the descriptors. Refer to the AT2LP Blaster User's Guide for more information.

Conclusion

The new features available in the EZ-USB AT2LP add even greater flexibility and performance to Cypress's EZ-USB AT2 family of parts while still allowing for drop-in replacement of the AT2 in existing designs.

As with Cypress's AT2, the AT2LP is made available with world-class development tools and software support. Visit www.cypress.com for more details and data sheet information.

Document History

Document Title: AN5071 – EZ-USB® AT2LP Features
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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1736703	KUH	11/13/2007	Obtained spec # to add to the spec system.
*A	3177098	LIP	02/18/2011	Updated links and replaced CY7C6830XB with CY7C6830XC.
*B	3348691	LIP	08/18/2011	No change. Completing sunset review.
*C	4184423	RSKV	11/06/2013	Obsolete document.

In March of 2007, Cypress recataloged all of its Application Notes using a new documentation number and revision code. This new documentation number and revision code (001-xxxxx, beginning with rev. **), located in the footer of the document, will be used in all subsequent revisions.

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