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Spec No: 001-41239

Spec Title: MIGRATING FROM CYPRESS FLEX18 / FLEX36(R) / FLEX72(TM) DUAL-PORT SRAMS TO FULLFLEX DUAL-PORT SRAMS - AN5042

Sunset Owner: Adithi Perepu (ADMU)

Replaced by: 001-89590

AN5042

Migrating from Cypress FLEx18 / FLEx36® / FLEx72™ Dual-Port SRAMs to FullFlex Dual-Port SRAMs

Author: Adithi Perepu and Reshmi R
Associated Project: No
Associated Part Family: CYDXXSXXVXX / CYDXXSXXV
Software Version: N/A
Related Application Notes: AN1043

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AN5042 discusses the features of Cypress's FullFlex Dual-Port SRAM and typical applications for which the devices are ideally suited. These devices provide an upgrade path from Cypress's previous generation FLEx18 / FLEx36® / FLEx72™ portfolio of Dual Port SRAMs For a basic introduction to the operation of Synchronous Dual-Port SRAMs, refer to AN1043 – Understanding Synchronous Dual Port SRAMs.

Introduction

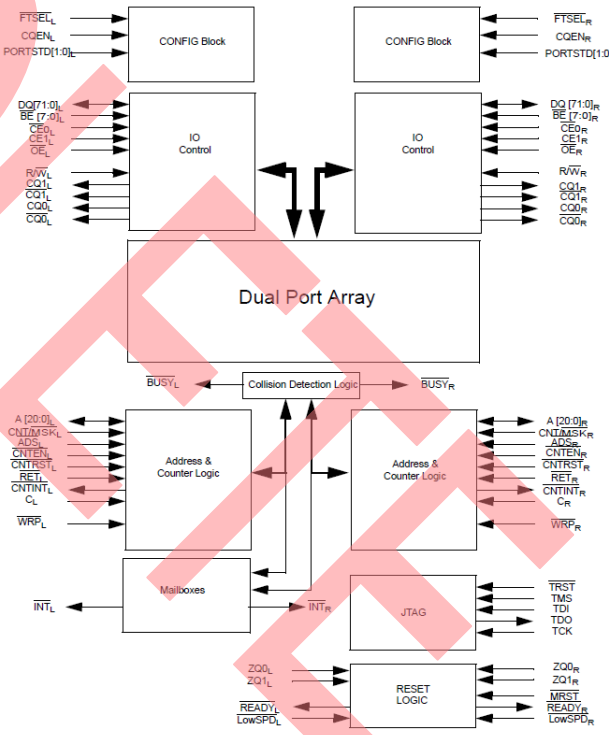
Cypress's FLEx18 / FLEx36® / FLEx72™ portfolio of high-density, high-performance synchronous Dual-Port SRAMs can operate at speeds up to 167 MHz. In the fast growing data communications market, the bandwidth requirements have increased. Cypress addresses these demands with its FullFlex Dual-Port SRAMs, which can operate up to 200 MHz. FullFlex Dual-Port SRAMs provide higher performance with enhanced features to ease system design, such as:

- Selectable I/O standards (3.3 V LVTTL, 2.5 V CMOS, 1.8 V CMOS and Extended HSTL (1.4 V to 1.9 V))
- Selectable pipeline and flow-through modes
- Speeds up to 200 MHz
- Burst counter features
- Variable Impedance Matching (VIM)
- Collision detection and
- Echo clocks to simplify data capture at the receiver

These features are discussed in detail in the following sections. FullFlex Dual-Ports have features similar to the FLEx18 / FLEx36 / FLEx72 devices, and they are offered in a variety of densities and bus width configurations. To plan for a seamless migration to the FullFlex Dual-Ports, the necessary pinout and default connections for the 484-BGA package FLEx18 / FLEx36 / FLEx72 Dual-Ports is provided in the Appendix Note that FullFlex Dual-Port SRAMs are footprint compatible with the FLEx18 / FLEx36 / FLEx72 Dual-Ports.

Figure 1 shows logical block diagram of x72 FullFlex device.

Figure 1. Logical Block Diagram of x72 FullFlex Device



Selectable I/O Standards

The FLEx18 / FLEx36 / FLEx72 Dual-Ports are 3.3 V LVTTL only devices, but the FullFlex Dual-Ports allow users to choose one of the four available I/O standards for each of two ports. This helps in interfacing host controllers with different I/O voltages, thus eliminating the need for level shifters and saving board space. The four selectable

I/O standards offered by FullFlex Dual-Port SRAMs are HSTL, 3.3 V LVTTL, 2.5 V LVCMOS, and 1.8 V LVCMOS.

The selection of I/O standard is determined by the PORTSTD0 and PORTSTD1 balls on each of the two ports. The setting determines the I/O standard used for the input clock, address, control, data and echo clock outputs for each port. See Table 1 for the specific PORTSTD[1:0] setting. These pins require LVTTL power supply.

Table 1. I/O Standards Selection*

I/O	PORTSTD1	PORTSTD0
3.3 V LVTTL	VSS	VSS
HSTL	VSS	VTTL
2.5 V LVCMOS	VTTL	VSS
1.8 V LVCMOS	VTTL	VTTL

*VTTL is same as 3.3V LVTTL power supply.

Selectable Pipeline and Flow-Through Mode

FLEx and FullFlex offer pipelined mode of operation. In addition to this, the FullFlex Dual-Port SRAMs offer selectable pipeline and flow-through modes. Flow-through mode has the advantage of having only one cycle of latency and good read-write-read turn-around operations. However, pipeline mode offers shorter access time and faster operating speed. There is also an initial read latency of one clock cycle for the pipelined mode. More details on the operating speed in both pipeline and flow-through modes is given in Speed Improvement section.

Flow-through or pipeline mode is selectable through the $\overline{FTSEL}$ ball. Tie this ball HIGH for pipeline mode and LOW for flow-through mode. FullFlex and FLEx18 / FLEx36 / FLEx72 Dual-Ports provide two pipeline stages in the pipelined mode of operation.

Speed Improvement

The FLEx18 / FLEx36 / FLEx72 family of Dual-Ports operate up to 167 MHz with two pipeline stages. With the same number of pipeline stages, the FullFlex Dual-Ports operate at frequencies of up to 200 MHz in HSTL and 1.8 V LVCMOS I/O standards, and up to 167 MHz in 3.3 V LVTTL and 2.5 V LVCMOS I/O standards. The FullFlex DualPorts have an internal DLL (Delay Locked Loop) to improve clock to data rates at high speeds. The DLL needs to be enabled by tying $\overline{LOWSPD}$ pin HIGH when operated at speeds of 100 MHz or above. The device can also be operated with the DLL disabled ($\overline{LOWSPD}$ LOW). There will be an increase in clock to valid data time in the DLL disabled mode – refer to the datasheet for more information on clock to data parameters when the device is operated in this mode.

The FullFlex Dual-Port will issue a $\overline{READY}$ signal after master reset in either 5 or 1024 clock cycles depending on the number of additional features enabled. It takes 5 clock cycles when Variable Impedance Matching (VIM) and DLL are disabled, whereas it takes 1024 clock cycles when any one of these features is used. VIM feature allows designers to adjust the impedance of the I/O driver to match the impedance of on-board traces. The FullFlex Dual-Port is not fully initialized until the $\overline{READY}$ output of each port is asserted. When $\overline{MRST}$ (Master Reset) is asserted, $\overline{READY}$ is deasserted by the FullFlex. Once $\overline{READY}$ becomes LOW, the Dual-Port SRAM is ready and a speed improvement can be achieved if the DLL is enabled ($\overline{LOWSPD}$ is tied HIGH).

Burst Counters

Each port is equipped with independent logic to support burst access to the Fullflex Dual-Ports. This logic includes a burst counter, mask register, retransmit control, counter interrupt, and address/mask readback. Direct addressing occurs by loading a new address on every cycle, done by asserting the $\overline{ADS}$ LOW on every cycle. The burst capability is utilized by loading the data packet's beginning address when $\overline{ADS}$ is LOW, followed by $\overline{ADS}$ HIGH and $\overline{CNTEN}$ LOW for the subsequent cycles. The $\overline{CNTEN}$ LOW enables the sequencing, but is ignored if a new address load is initialized ($\overline{ADS}$ being LOW). $\overline{CNTRST}$ resets the address pointer to zero, but does not disable the port from its access on that cycle. Burst read will be applicable when the dual port acts as a packet buffer in which the controller at the right port writes some data and the processor at the left port reads this data for further processing.

Table 2 shows the address counter and counter-mask register control operations for the Dual-Port.

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Table 2. Burst Counter and Counter-Mask Register Operation [1,2]

Clock	MRST	CNTRST	CNT/MSK	CNTEN	ADS	RET	Operation	Description
X	L	X	X	X	X	X	Master Reset	Reset address counter to all 0s mask register to all 1s and BUSY address to all 0s.
	H	L	H	X	X	X	Counter Reset	Reset counter and mirror unmasked portion to all 0s.
	H	L	L	X	X	X	Mask Reset	Reset mask register to all 1s.
	H	H	H	L	L	X	Counter Load	Load burst counter and mirror with external address value presented on address lines.
	H	H	L	L	L	X	Mask Load	Load mask register with value presented on the address lines.
	H	H	H	L	H	L	Retransmit	Load counter with value in the mirror register
	H	H	H	L	H	H	Counter Increment	Internally increment address counter value.
	H	H	H	H	H	H	Counter Hold	Constantly hold the address value for multiple clock cycles.
	H	H	H	H	L	H	Counter Readback	Read out counter internal value on address lines.
	H	H	L	H	L	H	Mask Readback	Read out mask register value on address lines.
	H	H	L	H	H	H	Busy Address Readback	Read out last busy address

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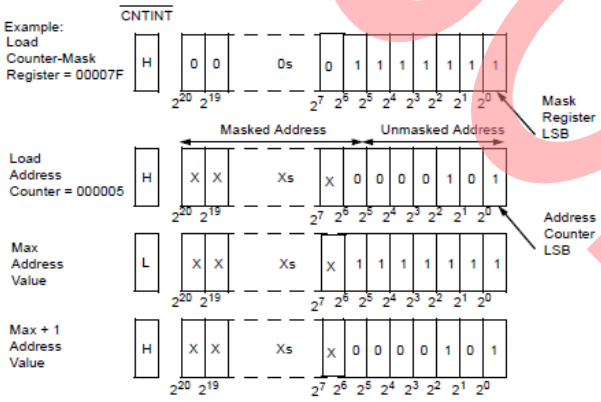
1 “X” = Don’t Care, “H” = HIGH, “L” = LOW.
2 Counter operation and mask register operation is independent of chip enables.

FullFlex Dual-Ports have two added counter functions compared to FLEx Dual-Ports: retransmit and busy address readback as described in Table 2, and this adds an additional $\overline{RET}$ ball on the device. Retransmit control provides repeated access to the same segment of memory, while busy address readback allows reading out the value contained in the busy address register to the address bus. For more information, refer to the Collision Detection section of this application note. Retransmit feature can be used in communication applications such as modems in which the data has to be retransmitted when it has been received in error or if it timed out.

The FullFlex Dual-Ports also support counter wrap-around function. When the burst counter reaches the maximum count and $\overline{WRP}$ is asserted, the next counter increment operation loads the unmasked counter bits with 0. When the burst counter reaches maximum count and $\overline{WRP}$ is deasserted, the next counter increment operation loads the counter bits with the value stored in the mirror register (Figure 2). For more information, refer to the FullFlex datasheets.

Figure 2. Programmable Counter Mask Operation with $\overline{WRP}$ Deasserted



Variable Impedance Matching (VIM)

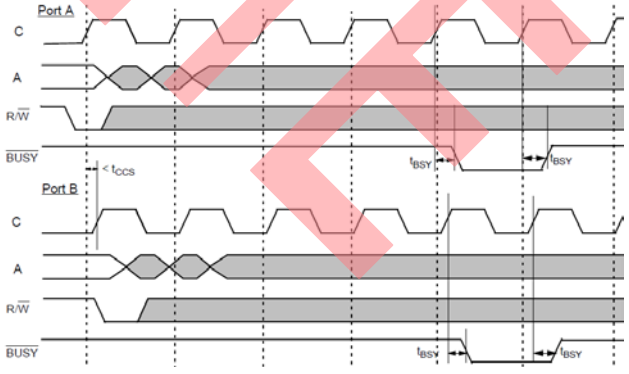
Transmission line effects are often encountered in high-speed digital designs. Impedance mismatches cause reflections on boards, which can impact a system's ability to reliably transmit and receive data. The FullFlex Dual-Ports allow designers to adjust the impedance of the I/O driver to match the impedance of on-board traces.

Each port of the FullFlex Dual-Ports has a VIM circuit. The circuitry has two ZQ balls per port and sets the output impedance for all outputs excluding JTAG outputs. A calibrating resistor (RQ) has to be connected between each ZQ pin and ground. The calibrating resistor must be five times the value of the intended line impedance being driven by the FullFlex Dual-Ports. For example, a 249 Ω resistor is required on ZQ pin to match the output impedance to the typical 50 Ω FR4 PCB trace impedance. The range of RQ needed to guarantee impedance matching is between 100 Ω and 275 Ω. Output impedance will be RQ/5 with a tolerance of ±15%. When RQ is out of the allowable range (i.e., RQ<100 Ω or RQ > 275 Ω), VIM will be disabled. The VIM circuitry also requires a calibration period of 1024 clock cycles and will not be fully functional until the calibration period has elapsed. This is indicated by the $\overline{READY}$ output for each port. When $\overline{MRST}$ is asserted, $\overline{READY}$ is deasserted. Once the Dual-Port asserts the $\overline{READY}$ signal, VIM is calibrated and ready. VIM can be disabled by either connecting the ZQ balls to VDDIO or leaving them NC.

Collision Detection

On a read or write cycle, the Fullflex Dual-Port compares the address being driven on one port with the address being used on the other. Both ports have to ensure a minimum time t_{CCS} (Clock rising edge to opposite port clock rising edge) for non-corrupted data. If a read operation is conducted from an address on one port and the other port attempts to do a write to the same address and t_{CCS} is not met, the writing port wins. The collision detection logic asserts the external $\overline{BUSY}$ signal to the losing read port synchronously on the rising edge of the fifth clock cycle that includes the collision cycle. In the case where both ports attempt to write to the same location and t_{CCS} is not met, the external $\overline{BUSY}$ signal is asserted on both ports synchronously on the rising edge of the fifth clock cycle (Figure 3). The collision detection logic will save the address in conflict to a readable register called Busy Address. In the case of multiple collisions in a row, the address of the first collision will be stored. The chip enables ($\overline{CE0}$ and CE1) must be enabled for both ports for the $\overline{BUSY}$ signal to be asserted. Refer to datasheet Table 4 (Deterministic Access Control Logic) for more details on collision detection.

Figure 3. $\overline{BUSY}$ Timing for Write-Write Collision, Clock Timing Violates tCCS, $\overline{BUSY}$ Asserted on Both the Ports



On the other hand, the FLEx18 / FLEx36 / FLEx72 Dual-Ports do not offer collision detection. When one port

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accesses a particular address, the other port cannot simultaneously write to the same address. If this is taken care of in the system design with the FLEx18 / FLEx36 / FLEx72 Dual-Ports, collision detection is not required on the FullFlex Dual-Port and the controller should never encounter a $\overline{BUSY}$ signal. If the functionality of the system can be enhanced by using collision detection in the FullFlex Dual-Ports, the controller should sample the BUSY signal and take a proper course of action. An example is to assert CNT/$\overline{MSK}$ on the losing port and read the Busy Address register.

Echo Clocks

As data rates increase, on-board delays induced by parasitic make it more difficult to provide accurate clock trees. To help alleviate this problem, the FullFlex Dual-Ports offer Echo Clocks that will re-align data lines with output clocks. In a read operation, the FullFlex Dual-Port receives an input clock that registers the address and control signals. The Dual-Port then buffers this clock and retransmits it with the data output. This buffered clock is called the Echo Clock and is provided on CQ and $\overline{CQ}$ balls. $\overline{CQ}$ is the inverted echo clock output and is 180 degree out of phase with CQ. This allows for more reliable data transfer at high speeds. Data from the memory gets latched out on the rising edge of CQ clock. The processor at the other end can use the rising edge of $\overline{CQ}$ to capture this data, ensuring enough setup and hold times. Echo Clock is enabled when CQEN is tied HIGH. Figure 4 illustrates the Echo Clock outputs.

Figure 4. Echo Clock Outputs

The Echo Clocks also require a calibration period of 1024 clock cycles and will not be fully functional until the calibration period has elapsed. This is indicated by the READY output for each port. When MRST is asserted, READY is deasserted by the FullFlex Dual-Port. Once READY becomes LOW, the Echo Clocks are initialized.

IEEE 1149.1 Boundary Scan Testing (JTAG)

The FLEx18 / FLEx36 / FLEx72 and FullFlex Dual-Ports both support IEEE 1149.1 Boundary Scan testing, but the JTAG circuitry and the software flow to access JTAG functions are different for the two device families.

From a JTAG perspective, the FLEx18 / FLEx36 / FLEx72 Dual-Ports behave like multiple JTAG devices in a serial chain. To execute JTAG testing in a scan chain, the user must merge the netlist with the printed circuit board (PCB) netlist and apply the Cypress supplied Boundary Scan Description Language (BSDL) file to each of two/four underlying devices. The BSDL file for each of the underlying devices is identical.

The FullFlex Dual-Ports are single JTAG devices with their own BSDL files. When migrating from FLEx18 / FLEx36 / FLEx72 to FullFlex Dual-Ports, the user must replace the merged FLEx18 / FLEx36 / FLEx72 netlists and BSDL files with the FullFlex Dual-Port BSDL files, and regenerate the JTAG vectors for the PCB. The four required Test Access Port (TAP) balls are at the same package ball locations for each device, thus the FLEx18 / FLEx36 / FLEx72 and the FullFlex Dual-Ports can be placed at the same location in a JTAG chain. When migrating from the FLEx18 / FLEx36 / FLEx72 to the FullFlex Dual-Ports, all required JTAG adjustments can be made in software.

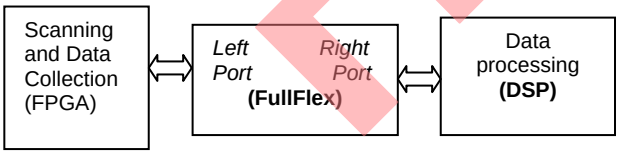
JTAG Reset

The TRST ball will perform the reset function for JTAG in FullFlex family. For seamless migration purpose, users can leave this ball to be NC.

Applications of FullFlex Dual-Port SRAM

Applications that involve data collection from different sources, high speed processing and re-distribution of the processed data over different communication channels require high-speed buffering. The FullFlex dual ports which can be operated at 200 MHz can ideally serve as the synchronous buffer, in such applications since it has independent ports which can be accessed simultaneously. Simultaneous accesses from both sides essentially eliminate the wait states that could occur while using a single port memory. Also, the additional features provided by the FullFlex Dual-Port SRAMs help in reliable data buffering and also eliminate the need for external components such as level shifters, which are normally required to interface with devices of different I/O standards.

Figure 5. Typical Application Example of FullFlex DP SRAM



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A typical example of FullFlex Dual-Port SRAM acting as a data buffer is where an FPGA collects data from multiple peripherals and has to transfer it to a DSP for data processing. The DSP may resend some of the processed data to the FPGA for transmission to other modules. In this case, the FullFlex Dual-Port SRAM acts as the interface between the FPGA and DSP and can handle the data buffering efficiently. As an example, assume the DSP operates at 1.8 V LVCMOS and the FPGA operates at HSTL I/O standard. Normally this would require additional level shifters on board for the interface. Since FullFlex can support multiple I/O standards using PORTSTD select, the need for level shifters is eliminated.

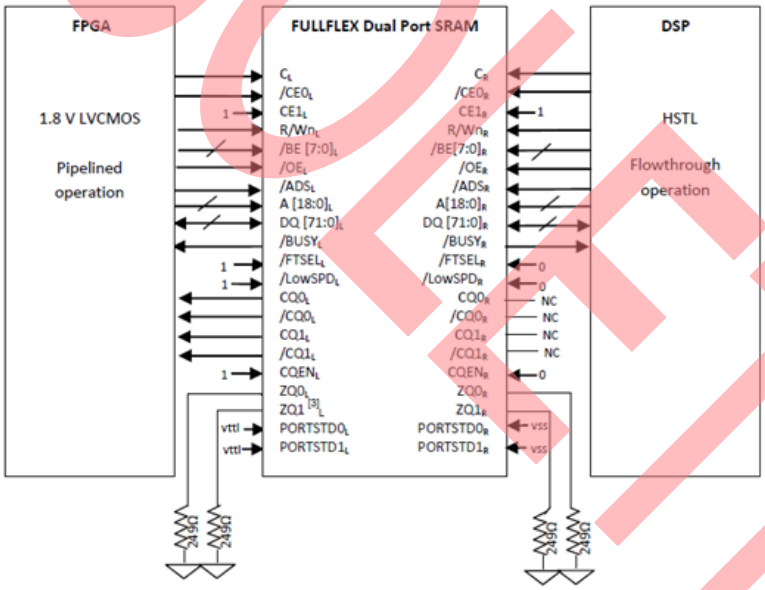
Since the FPGA has to send the processed data from the buffer to different communication channels, the left port of FullFlex DPSRAM interfaced to the FPGA can be operated in pipeline mode to increase the data throughput. The right port, interfaced to the DSP can be operated in flow-through mode. For pipelined operation, $\overline{FTSEL}_L$ has to be tied HIGH and for flow-through operation, $\overline{FTSEL}_R$ has to be tied LOW. Also, the internal DLL has to be disabled in flow-through mode by tying $\overline{LOWSPD}_R$ LOW.

Assume a scenario when the DSP is writing the processed data to the buffer and the FPGA tries to read the same location. This could result in reading corrupted data by the FPGA. The FullFlex Dual-Port SRAM has collision detection logic that helps prevent data inconsistency; FullFlex is a perfect fit for this application. The FullFlex will assert the $\overline{BUSY}$ signal to the FPGA indicating that the location is being used by the opposite port. The FPGA can read the data once $\overline{BUSY}$ is deasserted.

Since the left port operates in pipelined mode, Echo clock feature in FullFlex Dual-Port SRAMcan be used to simplify the data capture. Data from the memory gets latched out on the rising edge of CQ clock. FPGA can use the rising edge of $\overline{CQ}$ to capture this data, ensuring enough setup and hold times since the $\overline{CQ}$ rising edge will be in the centre of valid data.

Figure 6 shows the sample connection for this application, enabling all the FullFlex features discussed.

Figure 6. Sample Connections for the Application Example in Figure 5



3. The pin ZQ1 is applicable only for 36-Mbit devices. This pin is DNU for 18-Mbit and lower density devices.

4. '1' and '0' in Figure 5 stands for VDD and VSS respectively. Select appropriate VDD according to the PORTSTD selection.

5. 'NC' in the schematic stands for pins which are not connected to the board.

6. VTTL is same as 3.3 V LVTTL power supply

Conclusion

The FullFlex devices ease system design by offering a wide range of new features. The existing Cypress portfolio of high-density, high performance synchronous Dual-Ports, the FLEx18 / FLEx36 / FLEx72, provide an easy migration path to the new FullFlex Dual-Port SRAMs.

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Appendix

Migration from FLEx18 / FLEx36 / FLEx72 to FullFlex

Power Supply

The FLEx18 / FLEx36 / FLEx72 Dual-Ports operate on a 3.3 V core and I/O voltage, while the FullFlex Dual-Ports support a selectable 1.5 V or 1.8 V core voltage. The power supply pins to be noted during the migration from the FLEx18 / FLEx36 / FLEx72 Dual-Ports to the FullFlex Dual-Ports are:

VCORE: The Flex72 family of Dual-Ports does not use VCORE, and these pins are internally NC. FullFlex requires these VCORE pins to be connected to either 1.5 V or 1.8 V. The VCORE pins draw no current in the FLEx18 / FLEx36 / FLEx72 Dual-Ports, while in the FullFlex Dual-Ports, VCORE will draw a current of up to 800 mA (core and I/Os are powered by different power supplies).

VTTL: Defined as the LVTTL power supply, these pins should be connected to a 3.3 V or 2.5 V. The TAP operates using JEDEC-standard 3.3 V or 2.5 V I/O logic levels depending on the VTTL power supply.

To take advantage of the port standard selection options on the Dual-Ports, appropriate I/O power supplies and reference voltages need to be provided as outlined in Table 3.

VDDIO: I/O power supply.

VREF: HSTL reference output of 0.75 V. This pin should be left DNU if the HSTL I/O standard is not used.

Table 3. I/O Reference Voltage

IO STD	VDDIO			Vref		
	Min	Typ	Max	Min	Typ	Max
3.3 V LVTTL	3 V	3.3 V	3.6 V	NA	NA	NA
2.5 V CMOS	2.3 V	2.5 V	2.7 V	NA	NA	NA
1.8 V CMOS	1.7 V	1.8 V	1.9 V	NA	NA	NA
HSTL	1.4 V	1.5 V	1.9 V	0.68 V	0.80 V	0.95 V

For more information on the power supply pins in the FullFlex and FLEx18 / FLEx36 / FLEx72 dual ports, refer to the device datasheets.

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Selection of I/O Standards

In order to ensure proper migration (3.3 V to 3.3 V LVTTL I/Os), both PORTSTD1 and PORTSTD0 need to be tied LOW, as the FLEx18 / FLEx36 / FLEx72 Dual-Ports are 3.3 V LVTTL only devices. VDDIO and VTTL balls in the FLEx18 / FLEx36 / FLEx72 Dual-Ports must also be connected to a 3.3 V LVTTL power supply.

484 – BGA Pkg Pin	Pin Type	FLEx72 Pin Name	FLEx72 Datasheet Note	FullFlex Pin Name	Recommended Ball Connection for Easier Migration to FullFlex	Corresponding FullFlex Function/Mode
D10	Input	$PORTSTD0_L$	For FullFlex use only. Tie to V_{SS}	$PORTSTD0_L$	Low	3.3 V LVTTL
W13	Input	$PORTSTD0_R$	For FullFlex use only. Tie to V_{SS}	$PORTSTD0_R$	Low	3.3 V LVTTL
D14	Input	$PORTSTD1_L$	For FullFlex use only. Tie to V_{SS}	$PORTSTD1_L$	Low	3.3 V LVTTL
W9	Input	$PORTSTD1_R$	For FullFlex use only. Tie to V_{SS}	$PORTSTD1_R$	Low	3.3 V LVTTL

Selectable Pipeline and Flow-Through Modes

Flow-through or pipeline mode is selectable through the $\overline{FTSEL}$ ball. Tie this ball HIGH for pipeline mode and LOW for flow-through mode. FullFlex and FLEx18 / FLEx36 / FLEx72 Dual-Ports provide two pipeline stages in the pipelined mode of operation.

Since the FLEx18 / FLEx36 / FLEx72 Dual-Ports only operate in pipeline mode, $\overline{FTSEL}$ should be tied HIGH to ensure seamless migration.

484 – BGA Pkg Pin	Pin Type	FLEx72 Pin Name	FLEx72 Datasheet Note	FullFlex Pin Name	Recommended Ball Connection for Easier Migration to FullFlex	Corresponding FullFlex Function/Mode
V3	Input	$FTSEL_L$	For FullFlex use only. Tie to VDDIO	$FTSEL_L$	High	Pipelined mode
V20	Input	$FTSEL_R$	For FullFlex use only. Tie to VDDIO	$FTSEL_R$	High	Pipelined mode

Speed Improvement

484 – BGA Pkg Pin	Pin Type	FLEx72 Pin Name	FLEx72 Datasheet Note	FullFlex Pin Name	Recommended Ball Connection for Easier Migration to FullFlex	Corresponding FullFlex Function/Mode
D9	Input	$LOWSPD_L$	For FullFlex use only. Tie to V_{SS}	$LOWSPD_L$	Assert / De-assert based on speed of operation	Refer to the datasheet for details on operation
W14	Input	$LOWSPD_R$	For FullFlex use only. Tie to V_{SS}	$LOWSPD_R$		
J3	Output	$READY_L$	For FullFlex use only. Leave unconnected	$READY_L$	Connected	
J20	Output	$READY_R$	For FullFlex use only. Leave unconnected	$READY_R$		

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Burst Counters

To ensure seamless migration, users should disable (tie to HIGH) RET and WRP for the FLEx18 / FLEx36 / FLEx72 Dual-Ports.

484 – BGA Pkg Pin	Pin Type	FLEx72 Pin Name	FLEx72 Datasheet Note	FullFlex Pin Name	Recommended Ball Connection for Easier Migration to FullFlex	Corresponding FullFlex Function/Mode
G3	Input	RET_L	For FullFlex use only. Tie to VDDIO	RET_L	High	Disable Retransmit
G20	Input	RET_R	For FullFlexuse only. Tie to VDDIO	RET_R	High	Disable Retransmit
H3	Input	WRP_L	For FullFlex use only. Tie to VDDIO	WRP_L	High	Disable counter wrap
H20	Input	WRP_R	For FullFlex use only. Tie to VDDIO	WRP_R	High	Disable counter wrap

Note that the CYD18S72V devices do not support the burst counter feature. The corresponding counter control pins should be configured in counter load mode to allow for easy migration. That is, CNTRST and CNT/MSK need to be HIGH, whereas CNTEN and ADS should be LOW

484 – BGA Pkg Pin	Pin Type	FLEx72 Pin Name	FLEx72 Datasheet Note	FullFlex Pin Name	Recommended Ball Connection for Easier Migration to FullFlex	Corresponding FullFlex Function/Mode
P3	Input	CNT/MSK_L	Not Applicable. Tie to VDDIO	CNT/MSK_L	High	Counter Load
P20	Input	CNT/MSK_R	Not Applicable. Tie to VDDIO	CNT/MSK_R	High	Counter Load
R3	Input	$CNTEN_L$	Not Applicable. Tie to V_{SS}	$CNTEN_L$	Low	Counter Load
R20	Input	$CNTEN_R$	Not Applicable. Tie to V_{SS}	$CNTEN_R$	Low	Counter Load
D13	Output	$CNTINT_L$	Not Applicable. Should not be connected	$CNTINT_L$	Unconnected	
W10	Output	$CNTINT_R$	Not Applicable. Should not be connected	$CNTINT_R$	Unconnected	
T3	Input	$CNTRST_L$	Not Applicable. Tie to VDDIO	$CNTRST_L$	High	Counter Load
T20	Input	$CNTRST_R$	Not Applicable. Tie to VDDIO	$CNTRST_R$	High	Counter Load

VIM

To ensure seamless migration, the ZQ balls for the FLEx18 / FLEx36 / FLEx72 Dual-Ports should be left unconnected, as shown in the FLEx18 / FLEx36 / FLEx72 datasheets.

484 – BGA Pkg Pin	Pin Type	FLEx72 Pin Name	FLEx72 Datasheet Note	FullFlex Pin Name	Recommended Ball Connection for Easier Migration to FullFlex	Corresponding Function/Mode
D11	Input	NC	For FullFlex use only. Leave UNCONNECTED	$ZQ0_L$	Unconnected	Disable VIM feature
W12	Input	NC	For FullFlex use only. Leave UNCONNECTED	$ZQ0_R$	Unconnected	Disable VIM feature
K3	Input	NC	For FullFlex use only. Leave UNCONNECTED	$ZQ1_L$	Unconnected	Disable VIM feature
K20	Input	NC	For FullFlex use only. Leave UNCONNECTED	$ZQ1_R$	Unconnected	Disable VIM feature

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CollisionDetection

484 – BGA Pkg Pin	Pin Type	FLEx72 Pin Name	FLEx72 Datasheet Note	FullFlex Pin Name	Recommended Ball Connection for Easier Migration to FullFlex	Corresponding FullFlex Function/Mode
D12	Output	$BUSY_L$	For FullFlex use only. Leave UNCONNECTED	$BUSY_L$ BUSYL	Unconnected	
W11	Output	$BUSY_R$	For FullFlex use only. Leave UNCONNECTED	$BUSY_R$ BUSYR	Unconnected	

Echo Clocks

To plan for the migration from FLEx18 / FLEx36 / FLEx72 Dual-Ports to FullFlex Dual-Ports, CQEN should be tied LOW to disable the Echo Clocks. This is also documented in the FLEx18 / FLEx36 / FLEx72 Dual-Port datasheets.

484 – BGA Pkg Pin	Pin Type	FLEx72 Pin Name	FLEx72 Datasheet Note	FullFlex Pin Name	Recommended Ball Connection for Easier Migration to FullFlex	Corresponding FullFlex Function/Mode
U4	Input	REV_L	For FullFlex use only. Tie to V_{SS}	$CQEN_L$	Low	Disable Echo Clocks
U19	Input	REV_R	For FullFlex use only. Tie to V_{SS}	$CQEN_R$	Low	Disable Echo Clocks
W6	Output	NC	For FullFlex use only. Leave UNCONNECTED	$CQ0_L$	Unconnected	
W7	Output	NC	For FullFlex use only. Leave UNCONNECTED	$CQ0_L$	Unconnected	
W16	Output	NC	For FullFlex use only. Leave UNCONNECTED	$CQ0_R$	Unconnected	
W17	Output	NC	For FullFlex use only. Leave UNCONNECTED	$CQ0_R$	Unconnected	
D6	Output	NC	For FullFlex use only. Leave UNCONNECTED	$CQ1_L$	Unconnected	
D7	Output	NC	For FullFlex use only. Leave UNCONNECTED	$CQ1_L$	Unconnected	
D16	Output	NC	For FullFlex use only. Leave UNCONNECTED	$CQ1_R$	Unconnected	
D17	Output	NC	For FullFlex use only. Leave UNCONNECTED	$CQ1_R$	Unconnected	

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Document History

Document Title: Migrating from Cypress FLEx18 / FLEx36® / FLEx72™ Dual-Port SRAMs to FullFlex Dual-Port SRAMs - AN5042

Document Number: 001-41239

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1540705	ADMU	10/03/2007	New spec.
*A	3089657	ADMU	11/18/2010	Removed information (pin configuration diagrams, features offered, frequency details) about parts which are obsolete - CYD18S36V, CYD04S72V, CYD09S72V, CYD09S36V and CYD09S18V. Changed maximum operating frequency from 167 MHz to 200 MHz. Changed speed from 250 MHz to 200 MHz. Removed information about selectable echo delay from feature list and the echo clock description.
*B	3197727	ADMU	03/16/2011	Updated the title, abstract, and links.
*C	3882654	ADMU	01/24/2013	Updated document as per template and major content update throughout the document.
*D	4219392	ADMU	12/13/2013	Obsolete document. Completing Sunset Review.

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