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Spec No: 001-14799

Spec Title: INTERFACING CYPRESS MOBL(R) ASYNCHRONOUS DUAL-PORT TO TI OMAP1710 MULTIMEDIA PROCESSOR - AN5036

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Interfacing Cypress MoBL(R) Asynchronous Dual-Port to TI OMAP1710 Multimedia Processor

Author: Hingkwan Huen
Associated Project: Yes
Associated Part Family: MoBL® Dual Port
Software Version: NA
Related Application Notes: AN5055, AN5074, AN5056

If you have a question, or need help with this application note, contact the author at hkh@cypress.com

Systems using a TI OMAP1710 Multimedia Processor can easily benefit from the performance and flexibility of a Cypress Dual-Port. As one of the industry's lowest power consuming Dual-Ports, designing in the Cypress MoBL Dual-Port allows the customer to interconnect multiple processors in a system, where power is of the most concern, and without having to compromise in performance.

Introduction

The Texas Instruments OMAP1710 Multimedia Processor is a low-power, highly-integrated hardware and software platform designed to meet the application processing needs of next-generation embedded devices.

The OMAP™ platform enables OEMs and ODMs to quickly bring to market devices featuring rich user interfaces, high-processing performance, and long battery life through the maximum flexibility of a fully-integrated mixed-processor solution.

The OMAP1710 is primarily targeted at mobile communications applications using WLAN802.11x, Bluetooth, GSM, GPRS, EDGE, CDMA and other proprietary wireless standards. The processor provides video and image processing (MPEG, JPEG, etc.), advanced speech/audio processing, graphics and video acceleration, generalized web access and data processing.

The OMAP1710 Multimedia Processor supports External Memory Interface (EMIF) that readily connects to Cypress asynchronous Dual-Ports. This application note describes the wiring, EMIF register settings, and other design considerations for connecting the OMAP1710 Multimedia Processor to the 1/4-Mb Cypress MoBL® Dual-Port (CYDM256A16-55). The same design can be used in interfacing the OMAP1710 Multimedia Processor to other Cypress MoBL Dual-Ports in the x16 configuration, such as the CYDM128A16 and CYDM064A16.

TI External Memory Interface (EMIF)

The Texas Instruments OMAP1710 Multimedia Processor supports two types of external memory interfaces: EMIFF and EMIFS. EMIFF is primarily used to gluelessly interface the processor with SDRAMs, while the EMIFS is used to interface to asynchronous and synchronous burst memories, such as NAND/NOR flashes and asynchronous SRAM. The EMIFS is a 16-bit memory interface, and it can be configured to gluelessly interface to Cypress's low-power MoBL Dual-Ports.

The Cypress MoBL Dual-Port CYDM256A16 has a standard asynchronous SRAM interface. Table 1 lists the signal connections between the OMAP1710's EMIFS and Cypress MoBL Dual-Port CYDM256A16. This is a 1.8 V LVCMOS interface.

Table 1. EMIFS & CYDM256A16 Signal Equivalents

OMAP1710 EMIFS Signal (I/O)		CYDM256A16 Signal (I/O)		Function
FLASH.CSx	O	CE	I	Chip select
FLASH.WE	O	R/W	I	Write enable
FLASH.OE	O	OE	I	Output enable
FLASH.A[14:1]	O	A[13:0]	I	Address
FLASH.D[15:0]	I/O	I/O[15:0]	I/O	Data
FLASH.BE[1]	O	UB	I	Upper byte enable
FLASH.BE[0]	O	LB	I	Lower byte enable

Wiring Diagram

Figure 1 below shows the physical wiring between the OMAP1710 Multimedia Processor and the MoBL Dual-Port CYDM256A16. Either port of the Dual-Port may be used.

Figure 1. Wiring Diagram of OMAP1710 to CYDM256A16

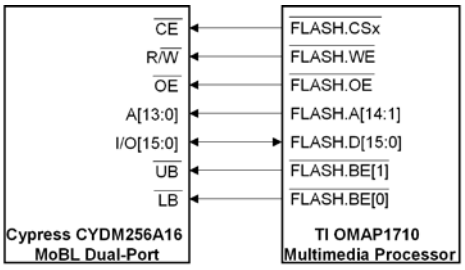


Table 2 shows the list of EMIF and MoBL Dual-Port pins that are not required for the memory interface (optional).

Table 2. Default Signal

CYDM256A16 Signal		OMAP1710 EMIFS Signal	
SEM	V_{DD}	FLASH.A[25:15]	NC
INT	NC	FLASH.CLK	NC
BUSY	NC	FLASH.RDY	V_{DD}
IRR[1:0]	V_{SS}	FLASH.ADV	NC
ODR[4:0]	NC	FLASH.BAA	NC
SFEN	V_{DD}	FLASH.RP	NC
M/S	V_{DD}	FLASH.WP	NC

To setup the EMIFS to properly interface to the Cypress MoBL Dual-Port, the following EMIFS registers need to be configured, while the rest of the register settings can be left in their default states. EMIFS Register Settings shows the required EMIFS register settings.

Table 3.EMIFS Register Settings

Field	Value	Description
EMIFS_CCSx: Chip-Select Configuration Register		
BTWST	0000b	Idle cycle # for bus turnaround and CS high-pulse-width timing
MAD	0b	Non-multiplexed protocol
BW	0b	Data bus is 16 bits wide
RDMODE	000b	Read mode setting - async.
WELEN	0010b	Pulse length during write access
WRWST	0000b	Wait states cycle number for write
RDWST	0011b	Wait states cycle number for read
FCLKDIV	01b	TC_CK divider for REF_CLK (REF_CLK ≤ 50MHz)
EMIFS_DWS: Dynamic Wait States Control Register		
WRRDYMASK_CSx	1b	FLASH.RDY signal is masked
Full handshake enable for CSx	1b	Non-full-handshaking
EMIFS_ACSx: Adv. Chip-Select Configuration Register		
OEHOLD	0000b	# of cycles from OE to CS (high)
OESETUP	0000b	# of cycles from CS to OE (low)

To arrive at the register settings shown above, assume the system clock TC_CK runs at 100 MHz; a 50-MHz REF_CLK is derived by dividing the system clock by two (FCLKDIV = 01b). Please note that this setting may vary depending on the speed of the desired memory interface as well as the speed of the system clock. Given most timing parameters of the OMAP processor are specified with a range of guaranteed values, the timing analysis below will use the worst case values, and the register settings takes into account the timing margin required for successful operations. The following section provides a brief explanation for each of the register settings.

EMIFS_CCSx - Chip-Select Configuration Register

BTWST—No wait states are needed to interface to the Cypress MoBL Dual-Port family.

MAD—Cypress MoBL Dual-Ports do not support multiplexed address and data bus; therefore, this field needs to be disabled.

BW—The memory interface to CYDM256A16 is 16-bit wide.

RDMODE—The Cypress MoBL Dual-Port family supports asynchronous reads.

WELEN—With a REF_CLK period of 20 ns, and referring to Figure 2-13 in the TI OMAP1710 Technical Reference Manual, the write pulse is given by P = (WELEN + 1)*REF_CLK. In order to fulfill the data setup time of the Cypress MoBL Dual-Port, WELEN needs to be 2 to provide enough margin for a successful write.

WRWST—Similar to WELEN, referring to Figure 2-13 in the TI OMAP1710 Technical Reference Manual, the duration of N = (WRWST + 1)*REF_CLK. In order to satisfy the timing requirement, setting WRWST to 0 can provide enough timing margin for a successful write.

RDWST—Refer to Figure 2-3 of the Technical Reference Manual, the duration of the chip select assertion N = (RDWST + 2)*REF_CLK. RDWST = 3 is required to provide enough margin for a successful read.

FCLKDIV—The EMIFS reference clock REF_CLK runs up to 50MHz. Assuming the system clock TC_CK runs at 100MHz, and for the sake of demonstrating a timing analysis, FCLKDIV needs to be 01b, which divides the frequency of TC_CK by two.

EMIFS_DWS - Dynamic Wait States Control Register

WRRDYMASK_CSx—Since full-handshaking mode is not supported by the Cypress MoBL Dual-Port family, FLASH.RDY is masked and not monitored by the processor.

Full handshake enable for CSx—Since full-handshaking mode is not supported by the Cypress MoBL Dual-Port family, this feature needs to be disabled.

EMIFS_ACSx - Adv. Chip-Select Configuration Register

OEHOLD—Initiating proper read operations with Cypress MoBL Dual-Ports requires OEHOLD to be 0b.

OESETUP—Initiating proper read operations with Cypress MoBL Dual-Ports requires OESETUP to be 0b.

EMIFS control and configurations can be done dynamically. EMIFS ensures that a new CS configuration takes effect only when no access is requested (CS idle). To prevent inconsistency and critical behavior, the EMIFS configuration must be done by MPU software while other masters are inactive.

For more information about EMIFS register settings, please see OMAP1710 *Multimedia Processor Technical*

Reference Manual, TI literature number SWPU071B, September 2004.

Timing Considerations

This section of the application note provides a sample timing analysis of read and write operations with the OMAP1710 Multimedia Processor and MoBL Dual-Port CYDM256A16-55.

Read Operation

With an internal reference clock of 50 MHz (20-ns period), the register setting required to initiate proper read operation is shown in EMIFS Register Settings. RDWST, which defines the number of waitstates inserted, needs to be 3 REF_CLK cycle. This essentially extends the chip select enable duration to 5 x REF_CLK = 100 ns. shows the timing details of a read operation between the OMAP1710 and MoBL Dual-Port.

The signal names for the OMAP processor and the MoBL Dual-Port are shown on the left. Timing parameters for the OMAP1710 are shown with an uppercase T while parameters for the MoBL Dual-Port are shown with a lowercase t. Please refer to for timing parameter definitions.

Table 4. **Read Timing Parameters**

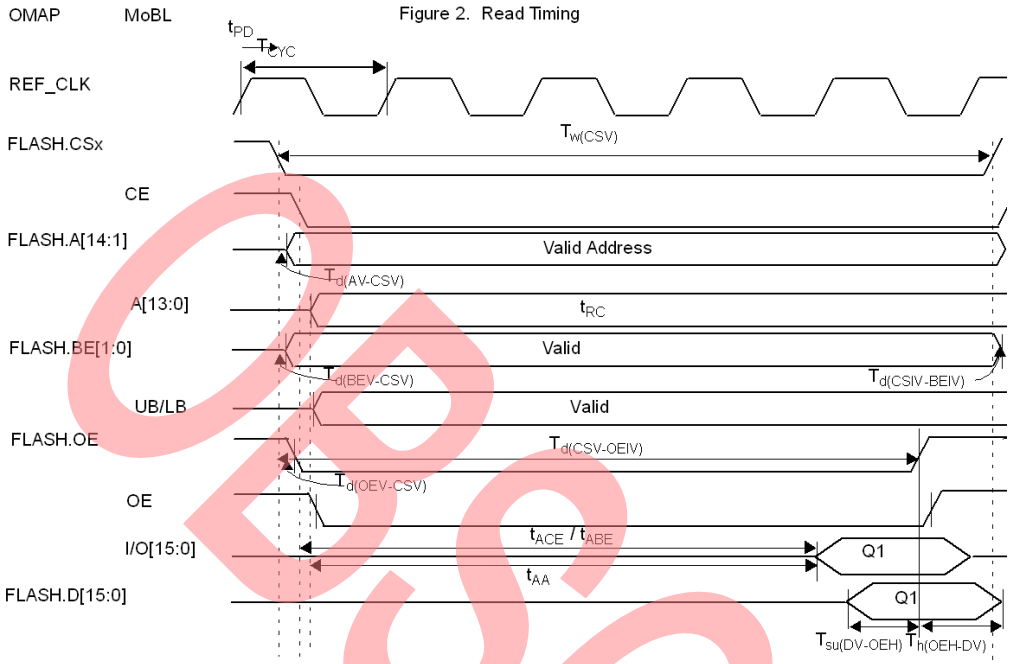
Symbol	Part	Description	Min (ns)	Max (ns)
t_{PD}	PCB	Board propagation delay	1	
T_{CYC}	OMAP	REF_CLK period	20	
$T_{W(CSV)}$	OMAP	FLASH.CSx low duration	98	102
$T_{d(AV-CSV)}$	OMAP	Delay, Address valid to FLASH.CSx low	–4	6
$T_{d(BEV-CSV)}$	OMAP	Delay, FLASH.BEx valid to FLASH.CSx low	–5	2
$T_{d(CSIV-BEIV)}$	OMAP	Delay, FLASH.CSx high to FLASH.BEx invalid	–2	5
$T_{d(OEV-CSV)}$	OMAP	Delay, FLASH.OE low to FLASH.CSx low	–1	5
$T_{d(CSV-OEIV)}$	OMAP	Delay, FLASH.CSx low to FLASH.OE high	95	98
$T_{su(DV-OEH)}$	OMAP	Set-up, read data valid before FLASH.OE high	15	-
$T_{h(OEH-DV)}$	OMAP	Hold, read data valid after FLASH.OE high	–14	-
t_{RC}	DP	Read cycle time	55	-
t_{ABE}	DP	Bye enable access time	-	55
t_{ACE}	DP	CE low to data valid	-	55
t_{AA}	DP	Address to data value	-	55
t_{OHA}	DP	Output hold from address change	5	-

The following timing analysis is based on the timing parameters for the OMAP1710 EMIFS running at 50 MHz and Cypress MoBL Dual-Port CYDM256A16-55.

Propagation Delay

Propagation delay (t_{PD}) is the board flight time between the OMAP1710 Multimedia Processor and the MoBL Dual-Port. This delay is important to take into account. A 3-inch FR-4 strip-line generates 0.528-ns delay (176-ps/inch delay) between the OMAP and the Dual-Port. The board propagation delay will vary for different board designs, and as a conservative assumption, 1 ns is used for this application note. Assume all signals going from OMAP1710 to the MoBL Dual-Port to have the same trace length and thus the same propagation delay. The only propagation delay that will be added is for the data coming back from the Dual-Port to the OMAP processor during a read operation.

Figure 2. Read Timing



Worst Case Analysis

Since most timing parameters are specified with a range of guaranteed values, it is possible to perform a worst case timing analysis using the tightest timing budget provided by the data sheets of the two devices. Referring to Figure 2, the worst parameters are shown in Table 5.

Table 5. Worst Case Timing Parameters for Read

Symbol	Worst Case (ns)	Explanation
$T_{W(CSV)}$	98	Shortest CE period
$T_{d(AV-CSV)}$	–4	Slowest address assertion
$T_{d(BEV-CSV)}$	–5	Slowest BE assertion
$T_{d(CSIV-BEIV)}$	–2	Shortest BE assertion
$T_{d(OEV-CSV)}$	–1	Slowest OE assertion
$T_{d(CSV-OEIV)}$	95	Shortest OE assertion
$T_{su(DV-OEH)}$	15	Minimum set-up
$T_{h(OEH-DV)}$	–14	Minimum hold
t_{RC}	55	Minimum read cycle
t_{ABE}	55	Slowest access time
t_{ACE}	55	Slowest access time
t_{AA}	55	Slowest access time
t_{OHA}	5	Minimum hold time

Address

The read cycle timing window needs to be at least t_{RC} as required by the MoBL Dual-Port, meaning the address needs to be valid for at least 55 ns. Since all control signals are asserted with reference to FLASH.CSx of the OMAP processor, the worst case valid address assertion happens $T_{d(AV-CSV)}$ (4 ns) after FLASH.CSx assertion. According to the OMAP documentations, the address line does not get deasserted until after the FLASH.CSx gets deasserted, thus a valid address will hold for at least $T_{w(CSV)} + T_{d(AV-CSV)}$ = 98 ns – 4 ns = 94 ns, which satisfies the 55-ns requirement of the MoBL Dual-Port.

Byte Enables and Output Enable

Similar to the address assertion, the byte and output enables are both asserted by the OMAP processor with reference to the FLASH.CSx signal. The worse case here is when byte enables are asserted $T_{d(BEV-CSV)}$ (5 ns) after the assertion of the FLASH.CSx signal. Applying the same concept, output enable becomes available $T_{d(OEV-CSV)}$ (1 ns) after the assertion of the FLASH.CSx signal. This satisfies timing as the data is read out from the Dual-Port at a much later time and the margin is sufficient for the given timing window

Data

The data is read from the MoBL Dual-Port with a certain access time after the address (t_{AA}), output enable (t_{DOE}), and chip or byte enables (t_{ACE} or t_{ABE}) become valid. In this case, since the chip enable signal acts as a reference to all other control signals driven by the OMAP processor, and $t_{AA} = t_{ABE} = t_{ACE}$ (55 ns), the slowest control signals to become valid are the byte enables. Thus, the MoBL Dual-Port will provide the data $T_{d(BEV-CSV)} + t_{ABE}$ = 5 ns + 55 ns = 60 ns after the assertion of *FLASH.CSx*. The data will propagate back to the OMAP processor and this incurs another 2 ns of propagation delay to the overall timing. That is, the data will arrive at the OMAP1710 processor 62 ns after the initial assertion of FLASH.CSx ($t_{PD} \times 2$ = 2 ns, because data needs to propagate back to the OMAP1710). This data will then hold for t_{OHA} (5 ns) after the address change

The minimum read data set-up time required by OMAP1710 is defined by $T_{su(DV-OEH)}$, which references to the time before FLASH.OE is deasserted. According to the worst case parameters, the FLASH.OE signal will be asserted for at least 95 ns after the assertion of FLASH.CSx. With the data coming back to the OMAP1710 62 ns after FLASH.CSx asserts low, $T_{su(DV-OEH)}$ + 62 ns = 15 ns + 62 ns = 77 ns $\leq$ 95 ns, which satisfies the 15-ns minimum set-up time. In terms of hold time, data needs to hold for $T_{h(OEH-DV)}$ after the deassertion of FLASH.OE (–14 ns). Since the Dual-Port data is held valid for t_{OHA} (5 ns) after the address change (same time as the deassertion of FLASH.CSx), the data hold time is easily satisfied.

Write Operation

Similar to the read operation, the write operation runs on the same internal EMIFS reference clock of 50 MHz. Please note that all write operations initiated by the OMAP1710 processor will be R/W (FLASH.WE) controlled, since the deassertion of the FLASH.WE signal happens $T_{d(WEIV-CSIV)}$ before the deassertion of FLASH.CSx.

The register setting required to initiate proper write operation is shown in EMIFS Register Settings. WRWST is set to 0b, as no wait state is required. On the other hand, WELEN is set to 2b to satisfy the minimum write pulse length of t_{PWE} (40 ns). Table 6 shows the timing details of a write operation between the OMAP1710 and MoBL Dual-Port

The timing diagram in Table 6 demonstrates a write operation between the OMAP1710 Multimedia Processor and the MoBL Dual-Port. The following analysis is based on the timing parameters for the Cypress CYDM256A16-55 Dual-Port. Table 6 lists the parameters as specified by the data sheets of the two devices.

Table 6. Write Timing Parameters

Symbol	Part	Description	Min (ns)	Max (ns)
t_{PD}	PCB	Board propagation delay	1	
T_{CYC}	OMAP	REF_CLK period	20	
$T_{W(CSV)}$	OMAP	FLASH.CSx low duration	94	106
$T_{d(AV-CSV)}$	OMAP	Delay, Address valid to FLASH.CSx low	–4	6
$T_{d(BEV-CSV)}$	OMAP	Delay, FLASH.BEx valid to FLASH.CSx low	–5	2
$T_{d(CSIV-BEIV)}$	OMAP	Delay, FLASH.CSx high to FLASH.BEx invalid	–2	5
Td(CSV-WEV)	OMAP	Delay, FLASH.CSx low to FLASH.WE low	16	22
$T_{d(WEIV-CSIV)}$	OMAP	Delay, FLASH.WE high to FLASH.CSx high	16	23
$T_{d(DV-CSV)}$	OMAP	Delay, data bus valid to FLASH.CSx low	1	9
$T_{d(DIV-CSIV)}$	OMAP	Delay, data bus invalid to FLASH.CSx high	0	9
t_{WC}	DP	Write cycle time	55	-
t_{AW}	DP	Address valid to write end	45	-
t_{PWE}	DP	Write pulse width	40	-
t_{SD}	DP	Data set-up to write end	30	-
t_{HD}	DP	Data hold from write end	0	-

The following sample timing analysis is based on the timing parameters for the OMAP1710 EMIFS running at 50 MHz and Cypress MoBL Dual-Port CYDM256A16-55.

Worst Case Analysis

Similar to the read operation, the same type of analysis is performed for the write operation. The worst case parameters are shown in Table 7.

Table 7. Worst Case Timing Parameters for Write.

Symbol	Worst Case (ns)	Explanation
$T_{W(CSV)}$	94	Shortest CE period
$T_{d(AV-CSV)}$	–4	Slowest address assertion
$T_{d(BEV-CSV)}$	–5	Slowest BE assertion
$T_{d(CSIV-BEIV)}$	–2	Shortest BE assertion
$T_{d(CSV-WEV)}$	22	Slowest WE assertion
$T_{d(WEIV-CSIV)}$	23	Shortest WE period
$T_{d(DV-CSV)}$	1	Slowest data valid
$T_{d(DIV-CSIV)}$	9	Shortest data valid period
t_{WC}	55	Minimum write cycle
t_{AW}	45	Minimum address enable to write end
t_{PWE}	40	Minimum write pulse width
t_{SD}	30	Minimum data setup time
t_{HD}	0	Minimum data hold time

Address

The write cycle timing window needs to be at least t_{WC} as required by the MoBL Dual-Port, meaning the address needs to be valid for at least 55 ns. Since all control signals are asserted with reference to FLASH.CSx of the OMAP processor, the worst case valid address assertion happens $T_{d(AV-CSV)}$ (4 ns) after FLASH.CSx assertion. According to the OMAP documentations, the address line does not get deasserted until after the FLASH.CSx gets deasserted, thus a valid address will hold for at least $T_{w(CSV)} + T_{d(AV-CSV)}$ = 94 ns – 4 ns = 90 ns, which satisfies the 55-ns requirement of the MoBL Dual-Port.

Byte Enables

Similar to the address assertion, the byte enables are asserted by the OMAP processor with reference to the FLASH.CSx signal. The worst case is when the byte enables are asserted $T_{d(BEV-CSV)}$ (5 ns) after the assertion of the FLASH.CSx signal. This; however, does not impact the write operation, as the data is written into the Dual-Port at a much later time (when FLASH.WE is deasserted).

Data

The data is written into the MoBL Dual-Port on the rising edge of the R/W signal, and this needs to satisfy both the minimum address valid to R/W deassertion time (t_{AW}) and the minimum write pulse width (t_{PWE}) requirements. The minimum t_{AW} required from the Dual-Port is 45 ns and the EMIFS supplies $T_{W(CSV)} – T_{d(WEIV-CSIV)}$ = 94 ns – 23 ns = 71 ns, which satisfies the 45-ns requirement. On the other hand, the minimum pulse width is satisfied, because $T_{W(CSV)} – T_{d(WEIV-CSIV)} – T_{d(CSV-WEV)}$ = 94 ns – 23 ns – 22 ns = 49 ns, which also satisfies the minimum t_{PWE} of 40 ns.

The minimum write set-up and hold time required by the MoBL Dual-Port is defined by t_{SD} and t_{HD}, respectively. These parameters are in reference to the time before and after the deassertion of the R/W signal. According to the worst case parameters, the data will be valid $T_{d(DV-CSV)}$ with reference to the assertion of FLASH.CSx and becomes invalid $T_{d(DIV-CSIV)}$ with reference to the deassertion of FLASH.CSx. This satisfies the t_{SD} set-up time, as the available set-up time is $T_{W(CSV)} – T_{d(WEIV-CSIV)}$ = 94 ns – 23 ns = 71 ns $\geq$ 30 ns, and the available hold time is $T_{d(WEIV-CSIV)}$ = 23 ns $\geq$ 0 ns.

Conclusion

Systems using a TI OMAP1710 Multimedia Processor can easily benefit from the performance and flexibility of a Cypress Dual-Port. As one of the industry's lowest power consuming Dual-Ports, designing in the Cypress MoBL Dual-Port allows the customer to interconnect multiple processors in a system, where power is of the most concern, and without having to compromise in performance. In addition, as this application note has shown, the interface between the TI OMAP1710 and Cypress MoBL Dual-Ports does not require any glue logic, which will save valuable board spaces

For further information, please visit the Cypress web site at www.cypress.com. The web site also provides the latest data sheets, models, and any related documentation.

References

1. Cypress Semiconductor, CYDM256A16, CYDM128A16, CYDM064A16, CYDM128A08, CYDM064A08 1.8V 4K/8K/16K x16 and 8K/16K x8 MoBL® Dual-Port Static RAM Data sheet, January 2005.
2. Texas Instruments, OMAP1710 Multimedia Processor Data Manual, Literature Number SWPS015, March 2004.
3. Texas Instruments, OMAP1710 Multimedia Processor Technical Reference Manual, Literature Number SWPU071B, September 2004.

Additional Resources

a. Interfacing Cypress MoBL(R) Dual-Port to TI OMAP5912 Application Processor - AN5055.

b. Interfacing Cypress MoBL(R) Asynchronous Dual-Port to TI OMAP2420 Multimedia Processor - AN5056.

c. Implementing Interprocessor Using Cypress MoBL(R) Dual-ports and the Milbox Register - AN5074.

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**	483207	ODC	04/25/2007	New Spec.
*A	3164700	ODC	02/07/2011	Updated as per template Added Additional Resources heading and provided links to application notes. Added Document History Page
*B	3243575	ODC	05/06/2011	Hyperlink added to AN5055, AN5074, and AN5056. Layout Guidelines section renames as Wiring Diagram Additional Resources information updated.
*C	3607156	AASI	05/02/2012	Converted from FrameMaker to docx.
*D	4460895	RSKV	07/30/2014	Obsolete document.

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