Please note that Cypress is an Infineon Technologies Company.
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

THIS SPEC IS OBSOLETE

Spec No: 001-42081

Spec Title: INTERFACING CYPRESS MOBL(R) DUAL-PORT TO INTEL(R) PXA272 EMBEDDED PROCESSOR - AN5035

Sunset Owner: MARK FU (MARF)

Replaced by: NONE

Interfacing Cypress MoBL® Dual Port to Intel® PXA272 Embedded Processor

AN5035

Author: Danny Tseng
Associated Project: None
Associated Part Family: MoBL® Dual Port
Software Version: None
Associated Application Notes: AN5036, AN5055, AN5056, AN5074

Application Note Abstract

AN5035 describes how to interface the PXA272 applications processor to the CYDM256A16 MoBL dual port

Introduction

The PXA272 embedded processor of the Intel® PCA processor family is an integrated system-on-a-chip microprocessor for high performance, dynamic and low-power portable handheld and handset devices.

The Intel PXA272 processor includes a memory interface that gives designers more flexibility as it supports a variety of external memory types.

CYDM256A16 is an asynchronous MoBL® dual port memory from Cypress Semiconductor. It has a 256-Kbit shared memory array with two 16-bit data buses. The shared memory structure allows independent access from both ports to 32K address locations. The device is available in –35 and –55 speed grades in both commercial and industrial temperature ranges. Internal arbitration logic is also available to decide which port gets access when both ports try to access the same memory location at the same time.

The MoBL dual port can act as an interconnect between two processing elements that share data while operating at different speeds. This application note describes how to interface the CYDM256A16 to the Intel PXA272.

External Memory Interface (EMI)

The Intel PXA272's external memory interface is a 16/32-bit interface and it can be configured to gluelessly interface to Cypress low-power MoBL dual ports.

The Cypress MoBL dual port CYDM256A16 has a standard asynchronous SRAM interface. Table 1 lists the signal connections between Intel PXA272 and Cypress MoBL dual port CYDM256A16.

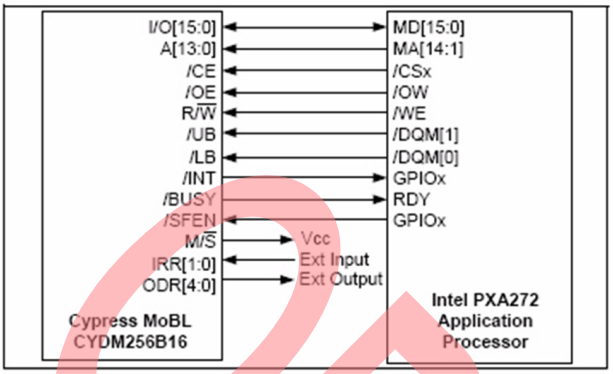
Table 1. PXA272 & CYDM256A16 Signal Equivalents

PXA272 Signal (I/O)		CYDM256A16 Signal (I/O)		Function
CSx	O	CE	I	Chip select
WE	O	R/W	I	Write enable
OE	O	OE	I	Output enable
MA[14:0]	O	A[14:0]	I	Address
MD[15:0]	I/O	DQ[15:0]	I/O	Data
DQM[1]	O	UB	I	Upper byte enable
DQM[0]	O	LB	I	Lower byte enable
RDY	I	BUSY	I/O	Busy signal
GPIOx	I	INT	O	Mailbox interrupt
GPIOx	O	SFEN	I	Special function enable
External devices	I	ODR[4:0]	O	Output drive register
External devices	O	IRR[1:0]	I	Input read register
		M/S	I	Master/Slave Select: pulled up to V_{CC}

Layout Guidelines

Figure 1 below shows the physical wiring between the PXA272 processor and the MoBL dual port CYDM256A16. Either port of the MoBL dual port may be used. Table 2 shows the list of unused PXA272 EMI pins.

Figure 1. Wiring Diagram of PXA272 to CYDM256A16



Voltage Compatibility

Table 2. Unused Intel PXA272 Signals

MA[25:15]	NC
CLK	NC

Cypress MoBL dual ports have operating voltages of 1.8 V, 2.5 V, and 3.0 V, while the Intel PXA272 supports 1.8 V, 2.5 V and 3.3 V I/O supply voltages. Thus, the Cypress MoBL dual ports are compatible with the Intel processor PXA272 when both devices operate at the same voltage.

PXA272 Register Settings

In order to properly interface the PXA272 to the Cypress MoBL dual port, the MSCx register of the processor needs to be configured, while the rest of the registers can be left in their default settings. Table 2 shows the recommended MSCx register setting, assuming the PXA272 processor is running at 520 MHz and connected to the CYDM256A16-55. The same analysis can be used to interface the processor to dual ports with the –40 speed grade.

Table 3. MSCx Register Settings

Field	Value	Description
RTx	001b	Type of memory: SRAM
RBW	1b	Data bus width: 16 bits
RDF	1111b	ROM/SRAM delay first access: 30* Clock pulse equivalent of processor
RDN	1111b	ROM/SRAM delay next access: 30* clock pulse equivalent of processor
RRR	101b	ROM/SRAM Recovery Time
RBUFF	0b	Fast/Slow device: Slow Device

Timing Considerations

This section of the application note provides a sample timing analysis of read and write operations with the PXA272 processor and MoBL Dual-Port CYDM256A16-55. Assume that the system clock of the processor runs at the maximum frequency of 520 MHz. Please note that the register setting may vary depending on the speed of the desired memory as well as the system clock frequency (refer to PXA27x processor family developers manual for detail).

Read Operation

With an internal reference clock of 520 MHz (1.923-ns clock period), the register settings required to set up proper read operations are shown in Table 2. RDF (ROM delay first access), which defines the number of wait states inserted in a read cycle, needs to be 30 times the REF_CLK clock cycle. This essentially extends the chip select enable duration of a read cycle to 30 x REF_CLK = 57.7ns. Figure 2 shows the timing details of a read operation between the PXA272 and MoBL Dual-Port.

To initiate a read operation, the shortest read cycle needs to be at least t_{RC}. The processor will also need to wait for the maximum of t_{AA}, t_{ABE} and t_{ACE} for the data to propagate back from the MoBL Dual-Port. The CYDM256A16-55 MoBL dual port has a t_{RC}= 55 ns, t_{AA} = 45ns and t_{ABE} = 45 ns.

Read access time for the SRAM controller is configured through the RDF field of MSCx register. Referring to the Intel documentation:

(RDFx+2)*(Time period of processor clock) ≥ Read Cycle time of the MoBL dual port.

=> RDFx ≥ ((Read cycle time of MoBL dual port/time period of processor clock) – 2.

=> RDFx ≥ (55ns/1.923) – 2 = 28.6 – 2 = 26.6.

=> RDFx ≥ 26.6

Considering the worst case, the decoded value of RDF should be set to 30 for extra timing margin (RDF="1111").

Subsequent read operation:

Before starting a subsequent MoBL dual port read, the processor should wait for at least t_{HZCE} = 20ns (max). To achieve this, we need to set the RRRx (ROM/SRAM recovery time) field of MSCx register. Referring to the Intel documentation:

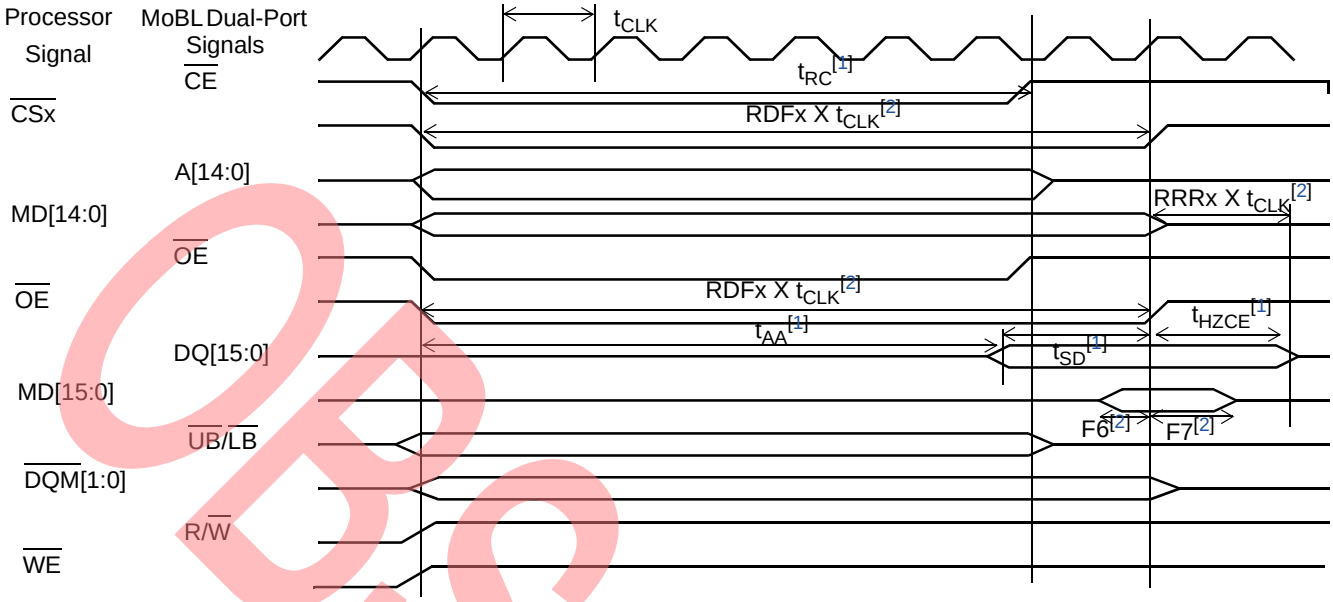
t_{OFF} ≥ (RRRx*2+1)*Processor clock period.

=> RRRx ≥ ((tOFF/Processor clock period) – 1)/2

=> RRRx ≥ ((20/1.923) – 1)/2 = 4.700

Considering the worst case, the decoded value of RRR should be set to 5 for extra timing margin (RRR="101").

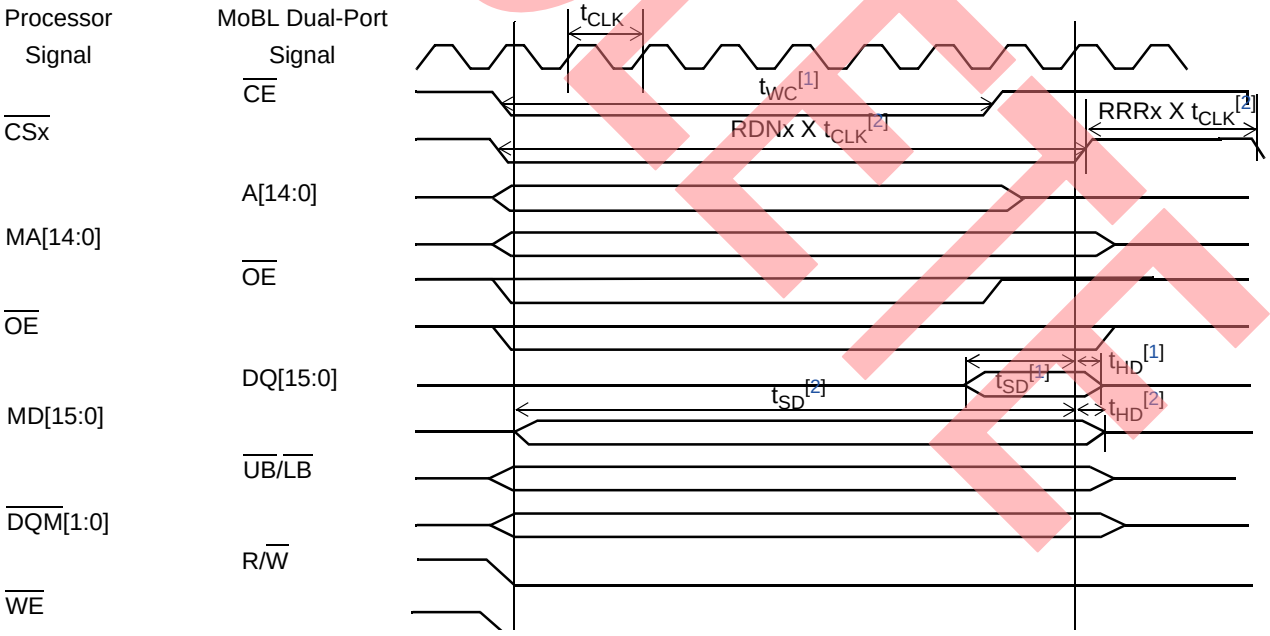
Figure 2. Read Cycle



Write Operation

Figure 3 shows the timing detail of a write operation between the PXA272 processor and the MoBL dual port. In order to write into the MoBL dual port, the minimum write cycle needs to be at least t_{WC}, while t_{AW}, t_{SD}, t_{HD}, t_{SA}, t_{HA} and t_{SCE} also need to be satisfied. Since $t_{SA} = t_{HD} = t_{HA} = 0$, these parameters should always be satisfied. With t_{WC}= 55 ns and $t_{AW} = t_{SCE}$ = 45 ns, the processor has to assert the write cycle for at least 55 ns for a correct write operation.

Figure 3. rite Cycle



Notes
1. Required by the MoBL Dual-Port for proper read.
2. Provided by the Processor.

The write cycle time for the SRAM controller is configured through the RDNx (ROM delay next access) field of MSCx register. According to Intel documentation:

RDNx + 1 = number of CLK_MEMs $\overline{WE}$ is asserted for write access.

=> RDNx $\geq$ (Write cycle time/ time period of clock) – 1.

=> RDNx $\geq$ (55 ns/1.923 ns) – 1 = 28.6 – 1 = 27.6.

Considering the worst case, the decoded value of RDN should be set to 30 for extra timing margin (RDN="1111").

Data Bus Switching

For CYDM256A16, t_{HD} = 0 ns.

Before starting the next MoBL dual port write, the processor should wait for at least t_{HD}. Since MoBL dual ports do not support burst mode, timing will always be satisfied by the processor if the MSCx register is configured with the values listed in Table 3.

Configuring the Memory Controller for PXA272

As discussed above, the memory controller must be configured to interface to the MoBL dual port. Apart from the timing parameters, the data width and type of memory are also configured in the MSCx register. According to Table 3, using $\overline{CS1}$, the upper 16 bits of the MSC0 (address 0x4800008) is set to "0101-1111-1111-1001".

The memory space of the PXA272 processor is divided into 6 slots: CS[5:0]. The MoBl dual port can connect to any of the chip selects. Table 4 shows the memory address space for each memory slot.

Table 4. Address Space of PXA272 Processor

Chip Select	Size	Function
CS0	32 MB	Memory space for async. device
CS1–CS5	64 MB	Memory space for async. device

Table 5 shows the timing parameter values required by the MoBL dual port and the ones provided by the Intel PXA272 processor with the memory controller configuration described previously.

Table 5. Timing Compatibility Table after Configuration

Operation	Parameter	Dual Port CYDM16A256	Relation	Processor PXA272
Read	t_{RC}	55ns	RDFx= "1111"	57.9 ns
Read	t_{SA}	0ns	–	Always satisfied
Read	t_{OHA}	5ns	–	Always satisfied
Read	t_{ACE}	55ns	RDFx= "1111"	57.9 ns
Read	t_{DOE}	30ns	–	Always satisfied
Read	t_{HZCE}	20ns	RRRx= "101"	25 ns
Read	t_{ABE}	55ns	RDFx= "1111"	57.9 ns
Write	t_{WC}	55ns	RDNx= "1111"	57.9 ns
Write	t_{HA}	0ns	–	Always satisfied
Write	t_{SA}	0ns	–	Always satisfied
Write	t_{SCE}	25ns	RRRx= "101"	25 ns
Write	t_{AW}	45ns	RDNx= "1111"	57.9 ns
Write	t_{SD}	30ns	–	Always satisfied
Write	t_{HD}	0ns	–	Always satisfied

Summary

Systems using a Intel PXA272 processor can easily benefit from the performance and flexibility of a Cypress dual port. As one of the industry's lowest power dual ports, designing in the Cypress MoBL dual port allows the customer to interconnect multiple processors in a system, where power is the most important concern, without having to compromise with performance. As this application note has shown, the Intel PXA272 can interface to the Cypress MoBL dual port seamlessly.

For further information, please visit the Cypress web site at www.cypress.com. The web site also provides the latest data sheets, models, and any related documentation.

References

1. Cypress Semiconductor, CYDM256A16, CYDM128A16, CYDM064A16, CYDM128A08, CYDM064A08 1.8 V, 2.5 V, 3.3 V 4 K/8 K/16 K x16 and 8 K/16 K x8 MoBL® Dual-Port Static RAM Data sheet, January 2005.
2. Intel Inc., PXA272 Processor Design Guide, Literature Number 280000101.pdf.
3. Intel inc., PXA27x Processor Family Developers Manual 2800002.pdf.

Document History Page

Document Title: Interfacing Cypress MoBL® Dual Port to Intel® PXA272 Embedded Processor - AN5035
Document Number: 001-42081

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1597683	HKH	10/11/2007	new spec.
*A	3366000	HKH	09/09/2011	Added Application Note Abstract Added Document History Page
*B	4636701	MARF	1/23/2015	Obsolete spec.

In March of 2007, Cypress recataloged all of its Application Notes using a new documentation number and revision code. This new documentation number and revision code (001-xxxxx, beginning with rev. **), located in the footer of the document, will be used in all subsequent revisions.

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone: 408-943-2600
Fax: 408-943-4730
http://www.cypress.com