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Spec No: 001-14864

Spec Title: USING VARIABLE IMPEDANCE MATCHING WITH THE FULLFLEX(TM) DUAL PORTS - AN5026

Sunset Owner: Sheetal Chennapnoor (SMCH)

Replaced By: 001-92810.

Using Variable Impedance Matching with the FullFlex™ Dual Ports

AN5026

Associated Project: No
Associated Part Family: FullFlex™ Dual ports
Software Version: Not applicable
Associated Application Notes: None

Abstract

Cypress's FullFlex™ Family of dual port SRAMs provide a Variable Impedance Matching (VIM) feature, which allows the system designer to set the I/O driver impedance to match the trace impedance without many resistors. The functionality, usage, and advantages of the Variable Impedance Matching (VIM) feature are discussed in this application note.

Introduction

Transmission line effects are a common problem with high-speed digital design. Impedance mismatches between PCB traces and the on-board devices result in signal reflection and ringing. This causes degradation in signal integrity, dramatically decreasing a system's ability to transmit and receive correct data. To solve this problem, designers place discrete terminating resistors on each of the on-board traces. These resistors calibrate the impedance of the devices' I/Os to match the impedance of the board traces. However, this imposes a PCB design challenge, as new devices have a high number of I/Os. Placing terminating resistors reasonably close to the I/Os is challenging and necessitates a lot of board space. In fact, extra board layers are often required for this purpose. This increases design difficulty, design time, and board cost. System reliability is also an issue, since discrete components that can potentially fail increases. Cypress's FullFlex™ Family of Dual-Port SRAMs allow the system designer to set the I/O driver impedance to match the trace impedance without many resistors.

Variable Impedance Matching

Each output port of the FullFlex™ dual port contains Variable Impedance Matching (VIM) circuitry that automatically sets the output impedance, with the exception of the JTAG pins. This section details how the VIM circuitry improves signal integrity, board reliability, and independence of change in operating conditions. It also reduces costs.

Optimal Signal Integrity: A major challenge for designers is optimizing signal integrity. Impedance mismatches cause signals to be reflected. The reflected signals interfere with the transmission of new data causing the data to be incorrect. Historically, the solution was to add terminating resistors to each on-board trace. These resistors need to be in close proximity to the outputs. A distance of more than approximately 0.5 inch causes stub reflection. With the VIM circuit, the termination is done at the die, completely eliminating stub reflection. The circuitry ensures that there are no impedance mismatches between the traces and the devices. Optimal signal integrity also maximizes I/O bandwidth.

Increase In System Reliability: When implementing the traditional solution to transmission line effects, component failure is an important design consideration. The larger number of components creates a higher probability of system failure. The VIM circuitry reduces the number of discrete components the board complexity. As a result, reliability is increased.

Reduction in Board Space and Costs: One terminating resistor is needed per trace on the board. These resistors require a lot of board space; hence the board cost increases. The PCB design challenge and development time is a function of the number of terminating resistors. The design may also require additional board layers. The VIM circuitry reduces the complexity of the board as well as the board space requirement.

Decrease In Vulnerability to Voltage and Temperature Changes: The traditional solution of using many resistors to transmission line effects is vulnerable to voltage and temperature changes since the output impedance varies greatly over the range of operating voltages and temperatures, causing impedance mismatches. The VIM circuitry updates the dual-port's output impedance every 1024 clock cycles. Since the output impedance is

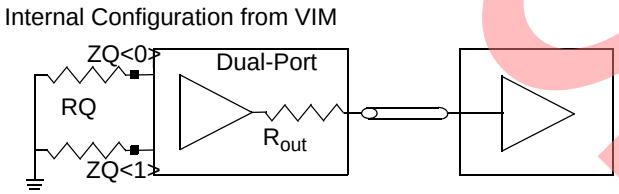
continuously updated to account for changes in voltage and temperature, the system's vulnerability to these environmental changes is decreased.

Variable Impedance Matching Feature

This section will describe the functionality and how to use the the VIM feature.

Each output port of the FullFlex™ dual port contains an independent VIM circuitry, as described in the previous section. To automatically set the output impedance, each port contains two inputs for this circuitry, ZQ<1:0>. The system designer connects a calibrating resistor (RQ) between each ZQ and ground. RQ must be five times (5×) the value of the needed line impedance driven by the dual-port. It must also have a value between 100 Ω and 275 Ω, with a 2% tolerance and a temperature coefficient of 200 ppm/°C, to guarantee a resulting output line impedance R_{out} of 20 Ω to 55 Ω with a 15% tolerance. If RQ is outside of this range, VIM is disabled. *Figure 1* below graphically represents the result of the VIM circuitry feature. Note the figure only displays the input and output of one port.

Figure 1. Internal Dual-Port Configuration due to VIM Feature. Each trace is terminated at the die.



The VIM circuitry resets when $\overline{MRST}$ is asserted, resetting the entire dual-port. When $\overline{MRST}$ is deasserted, the VIM circuitry begins to match the output line impedance to 0.2 × RQ. It reaches its final value before the $\overline{READY}$ pin is asserted, confirming that the device is ready for normal operation. This process is completed within 1024 cycles of the respective clock for each port. Then, the output impedance is adjusted every 1024 clock cycles to account for drifts in voltages and changes in temperature. If the clock is suspended (stopped), the VIM retains its last setting until the clock is restarted.

The board designer can choose to disable VIM by connecting the ZQ pin to the VDD pin or leaving it "no connect" while the $\overline{MRST}$ is still asserted. The output driver is configured to minimum impedance when VIM circuitry is disabled.

Table 1 below summarizes all of the VIM features available to the FullFlex™ dual port.

Table 1. VIM Features for FullFlex™ dual port

ZQ Connection	Output Configuration
RQ = (100 Ω to 275 Ω) to VSS	Output driver impedance = (RQ/5) ± 15% at V_{out} = VDDQ/2
ZQ pin tied to VDD or left floating	$R_{out} \leq$ 20 Ω ± 15% at V_{out} = VDDQ/2

Conclusion

Most systems can easily benefit from the performance and flexibility of a Variable Impedance Matching circuitry. As this application note has shown, VIM eliminates the transmission line effect, improving signal integrity, I/O bandwidth and system reliability without requiring excessive board space.

For further information, please visit the Cypress web site at www.cypress.com. The web site also provides the latest data sheets, models, and any related documentation.

Document History

Document Title: Using Variable Impedance Matching with the FullFlex™ Dual Ports - AN5026
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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	993720	AJU	04/19/2007	Existing Application Note in the web - Added Spec No. and new disclaimer and also updated the copyright date Please post in the web- overwrite the existing AN5026 file
*A	3121056	ADMU	01/20/2011	Updated Template. Changed reference name: Flex-E to FullFlex Changed maximum value of RQ from 350 Ω to 275 Ω in Variable Impedance Matching Feature. Changed maximum value of Rout from 75 Ω to 55 Ω in Variable Impedance Matching Feature.
*B	3250457	ADMU	05/17/2011	Modified abstract.
*C	4401045	ADMU	06/06/2014	Obsolete document. Content moved into a white paper, 001-92810.

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