

**Please note that Cypress is an Infineon Technologies Company.**

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

**Continuity of document content**

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

**Continuity of ordering part numbers**

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.



THIS SPEC IS OBSOLETE

Spec No: 001-14864

Spec Title: USING VARIABLE IMPEDANCE MATCHING  
WITH THE FULLFLEX(TM) DUAL PORTS -  
AN5026

Sunset Owner: Sheetal Chennapoor (SMCH)

Replaced By: 001-92810.

## AN5026

**Associated Project:** No  
**Associated Part Family:** FullFlex™ Dual ports  
**Software Version:** Not applicable  
**Associated Application Notes:** None

### Abstract

Cypress's FullFlex™ Family of dual port SRAMs provide a Variable Impedance Matching (VIM) feature, which allows the system designer to set the I/O driver impedance to match the trace impedance without many resistors. The functionality, usage, and advantages of the Variable Impedance Matching (VIM) feature are discussed in this application note.

### Introduction

Transmission line effects are a common problem with high-speed digital design. Impedance mismatches between PCB traces and the on-board devices result in signal reflection and ringing. This causes degradation in signal integrity, dramatically decreasing a system's ability to transmit and receive correct data. To solve this problem, designers place discrete terminating resistors on each of the on-board traces. These resistors calibrate the impedance of the devices' I/Os to match the impedance of the board traces. However, this imposes a PCB design challenge, as new devices have a high number of I/Os. Placing terminating resistors reasonably close to the I/Os is challenging and necessitates a lot of board space. In fact, extra board layers are often required for this purpose. This increases design difficulty, design time, and board cost. System reliability is also an issue, since discrete components that can potentially fail increases. Cypress's FullFlex™ Family of Dual-Port SRAMs allow the system designer to set the I/O driver impedance to match the trace impedance without many resistors.

### Variable Impedance Matching

Each output port of the FullFlex™ dual port contains Variable Impedance Matching (VIM) circuitry that automatically sets the output impedance, with the exception of the JTAG pins. This section details how the VIM circuitry improves signal integrity, board reliability, and independence of change in operating conditions. It also reduces costs.

**Optimal Signal Integrity:** A major challenge for designers is optimizing signal integrity. Impedance mismatches cause signals to be reflected. The reflected signals interfere with the transmission of new data causing the data to be incorrect.

Historically, the solution was to add terminating resistors to each on-board trace. These resistors need to be in close proximity to the outputs. A distance of more than approximately 0.5 inch causes stub reflection. With the VIM circuit, the termination is done at the die, completely eliminating stub reflection. The circuitry ensures that there are no impedance mismatches between the traces and the devices. Optimal signal integrity also maximizes I/O bandwidth.

**Increase In System Reliability:** When implementing the traditional solution to transmission line effects, component failure is an important design consideration. The larger number of components creates a higher probability of system failure. The VIM circuitry reduces the number of discrete components the board complexity. As a result, reliability is increased.

**Reduction In Board Space and Costs:** One terminating resistor is needed per trace on the board. These resistors require a lot of board space; hence the board cost increases. The PCB design challenge and development time is a function of the number of terminating resistors. The design may also require additional board layers. The VIM circuitry reduces the complexity of the board as well as the board space requirement.

**Decrease In Vulnerability to Voltage and Temperature Changes:** The traditional solution of using many resistors to transmission line effects is vulnerable to voltage and temperature changes since the output impedance varies greatly over the range of operating voltages and temperatures, causing impedance mismatches. The VIM circuitry updates the dual-port's output impedance every 1024 clock cycles. Since the output impedance is

continuously updated to account for changes in voltage and temperature, the system's vulnerability to these environmental changes is decreased.

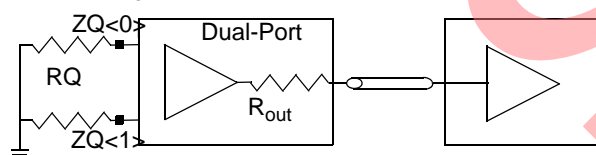
## Variable Impedance Matching Feature

This section will describe the functionality and how to use the the VIM feature.

Each output port of the FullFlex™ dual port contains an independent VIM circuitry, as described in the previous section. To automatically set the output impedance, each port contains two inputs for this circuitry,  $ZQ<1:0>$ . The system designer connects a calibrating resistor ( $RQ$ ) between each  $ZQ$  and ground.  $RQ$  must be five times ( $5\times$ ) the value of the needed line impedance driven by the dual-port. It must also have a value between  $100\ \Omega$  and  $275\ \Omega$ , with a 2% tolerance and a temperature coefficient of  $200\ \text{ppm}/^\circ\text{C}$ , to guarantee a resulting output line impedance  $R_{out}$  of  $20\ \Omega$  to  $55\ \Omega$  with a 15% tolerance. If  $RQ$  is outside of this range, VIM is disabled. Figure 1 below graphically represents the result of the VIM circuitry feature. Note the figure only displays the input and output of one port.

**Figure 1. Internal Dual-Port Configuration due to VIM Feature. Each trace is terminated at the die.**

Internal Configuration from VIM



The VIM circuitry resets when  $\overline{MRST}$  is asserted, resetting the entire dual-port. When  $\overline{MRST}$  is deasserted, the VIM circuitry begins to match the output line impedance to  $0.2 \times RQ$ . It reaches its final value before the  $\overline{READY}$  pin is asserted, confirming that the device is ready for normal operation. This process is completed within 1024 cycles of the respective clock for each port. Then, the output impedance is adjusted every 1024 clock cycles to account for drifts in voltages and changes in temperature. If the clock is suspended (stopped), the VIM retains its last setting until the clock is restarted.

The board designer can choose to disable VIM by connecting the  $ZQ$  pin to the  $VDD$  pin or leaving it "no connect" while the  $\overline{MRST}$  is still asserted. The output driver is configured to minimum impedance when VIM circuitry is disabled.

Table 1 below summarizes all of the VIM features available to the FullFlex™ dual port.

**Table 1. VIM Features for FullFlex™ dual port**

ZQ Connection	Output Configuration
$RQ = (100\ \Omega \text{ to } 275\ \Omega) \text{ to VSS}$	Output driver impedance = $(RQ/5) \pm 15\%$ at $V_{out} = VDDQ/2$
$ZQ$ pin tied to $VDD$ or left floating	$R_{out} \leq 20\ \Omega \pm 15\%$ at $V_{out} = VDDQ/2$

## Conclusion

Most systems can easily benefit from the performance and flexibility of a Variable Impedance Matching circuitry. As this application note has shown, VIM eliminates the transmission line effect, improving signal integrity, I/O bandwidth and system reliability without requiring excessive board space.

For further information, please visit the Cypress web site at [www.cypress.com](http://www.cypress.com). The web site also provides the latest data sheets, models, and any related documentation.

## Document History

**Document Title:** Using Variable Impedance Matching with the FullFlex™ Dual Ports - AN5026

**Document Number:** 001-14864

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	993720	AJU	04/19/2007	Existing Application Note in the web - Added Spec No. and new disclaimer and also updated the copyright date Please post in the web- overwrite the existing AN5026 file
*A	3121056	ADMU	01/20/2011	Updated Template. Changed reference name: Flex-E to FullFlex Changed maximum value of RQ from 350 $\Omega$ to 275 $\Omega$ in <a href="#">Variable Impedance Matching Feature</a> . Changed maximum value of Rout from 75 $\Omega$ to 55 $\Omega$ in <a href="#">Variable Impedance Matching Feature</a> .
*B	3250457	ADMU	05/17/2011	Modified abstract.
*C	4401045	ADMU	06/06/2014	Obsolete document. Content moved into a white paper, 001-92810.

FullFlex is a trademark of Cypress Semiconductor Corporation. All other product and company names mentioned in this document are the trademarks of their respective holders.

Cypress Semiconductor  
198 Champion Court  
San Jose, CA 95134-1709  
Phone: 408-943-2600  
Fax: 408-943-4730  
<http://www.cypress.com>

© Cypress Semiconductor Corporation, 2005-2014. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

This Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.