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THIS SPEC IS OBSOLETE

Spec No: 001-16630

Spec Title: STAR-1000 FREQUENTLY ASKED QUESTIONS-AN5014

Sunset Owner: Evelyn Beard (EYB)

Replaced by: None

CYPRESS PERFORM

STAR-1000 Frequently Asked Questions

AN5014

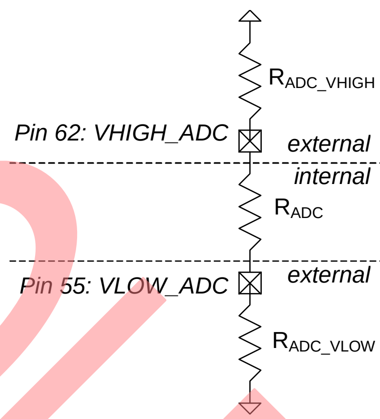
1. Do the internal bias resistor values depend on temperature?

Yes, the internal bias resistor value depends on the temperature of the sensor die due to the temperature dependency of the poly sheet resistance. This is most important for the ADC input range because this range is set with a resistor ladder of two external resistors (VLOW_ADC and VHIGH_ADC) and the internal ADC. The internal ADC resistor value increases approximately 4.4 Ω/°C with increasing temperature.

Table 1. R_{ADC} as Function of Temperature

Temp. [°C]	R_{ADC} [Ω]
–40	850
+23	1150
+85	1400

Figure 1. ADC Ladder Resistor Setting



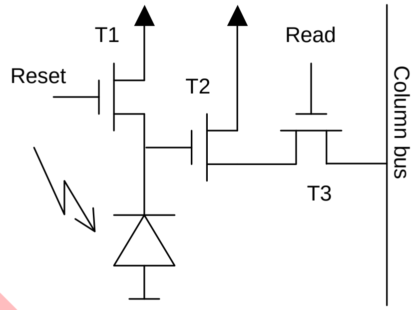
2. Does the STAR-1000 suffer from an incomplete reset (image lag)?

With the default settings in the data sheets the STAR-1000 suffers from image lag mainly visible at higher gains. Image lag is defined as an incomplete reset of the previous frame; therefore, saturated parts in the previous frame are not completely reset to the dark level at the beginning of the current frame.

This image lag is the image lag associated with "soft reset" operation. This means in the 3T pixel, both the supply (=VDDA) and VRES are equal (5V). During reset, the reset MOSFET is in weak inversion and will only asymptotically reach equilibrium—in the absence of current. Response to small excursions of this equilibrium happens with large time constants.

This can be solved by a bias current operating the pixels in "hard reset." This is accomplished by not allowing the reset MOSFET to go in weak inversion; this is done by, for example, turning the VDDA down to about 3.0 V to 3.5 V or by turning VDDA down to 4 V and VRES up to 5.5 V. If VRES – VDDA < Vth, the reset MOSFET is not in linear regime during reset, but in weak inversion, thus causing the image lag as it behaves as a current source with long time constant. If VRES – VDDA > Vth, the reset MOSFET is in linear regime during reset and acts as an (±) ideal switch. The value VDDA is the highest (starting) voltage on the photodiode. By light or by dark current, the voltage on the photodiode gradually drops.

Figure 2. Pixel Schematic with T1 as Reset MOSFET



The pixel's (highest) output voltage is (VRES – Vth – Vth) or (VDDA – Vth), whichever is lower. This explains the fact that the voltage range can change a little bit in hard reset mode (of course, the voltage that you see at the sensor output goes through some additional stages).

In the “soft reset” mode, the STAR-1000 electro-voltaic response curve is nonlinear in the dark region. When the pixel is biased in “hard reset”, this issue is solved and the response is completely linear.

With the “hard reset” setting, each pixel is always reset to exactly the same value (VDDA) independent of the actual photocurrent. Therefore, this setting eliminates several reset issues that occur with “soft reset” (for instance pixels that are reset to a dark level higher than the normal dark level). The “hard reset” setting resets each pixel to the same value for each frame independent of the pixel value from the previous frame.

3. Is the STAR-1000 sensor compatible with 3.3 V logic levels?

The digital inputs and outputs are actually designed to receive 3.3 V logic signals, even when the digital power supply (VDDD) is +5 V. The threshold levels on all digital inputs are:

VIH, rising edge: 1.8 V

VIH, falling edge: 1.3 V

When the digital output buffers of the ADC (VDD_DIG_OUT) are supplied with 3.3 V, the complete device is 3.3 V-compatible while all other supplies are supplied with 5 V.

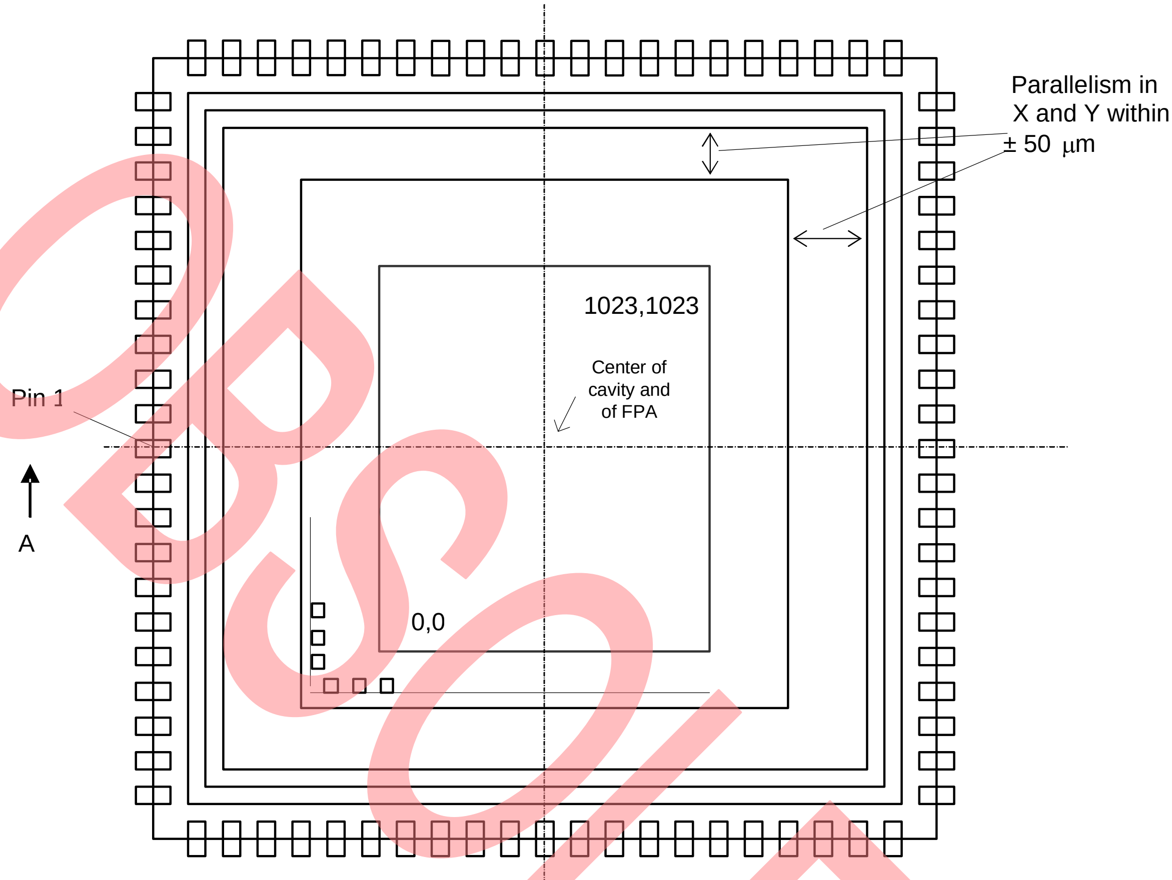
4. Can the on-chip multiplexer also be used to digitize other analog input signals?

The internal multiplexer has four analog inputs (A_IN1, A_IN2, A_IN3, and the pixel array output). By using the selection bits A_SEL0 and A_SEL1, one of the four inputs is selected and can be connected to the input of the internal ADC. However, because the three additional inputs (A_IN1, A_IN2, and A_IN3) have a fairly low bandwidth, only DC-signals (for instance of a temperature module) can be digitized with the internal ADC.

5. Where is pixel 0,0 located in the package?

The STAR-1000 sensor is bonded in an 84-pin JLCC package (see data sheets p31 paragraph 6.1 for a detailed package drawing). The centre of the pixel array is placed in the centre of the ceramic package. Pixel 0,0 is located on the bottom left corner in Figure 3.

Figure 3. Die Placement of STAR-1000 Sensor



6. How is the frame rate of the STAR-1000 calculated?

Due to the pseudo random addressing of the STAR-1000, the frame rate depends on the resolution of the region of interest (ROI) that is read out.

Frame period = (Nr. Lines × (RBT + pixel period × Nr. Pixels))

with: Nr. Lines: Number of Lines read out each frame (Y)

Nr. Pixels: Number of pixels read out each line (X)

RBT: Row Blanking Time = 2.3 µs (typical)

Pixel period: 1/12 MHz = 83.3 ns (typical)

Example: read out time of the full resolution at nominal speed (12 MHz pixel rate):

=> Frame period = (1024 × (2.3 µs + 83.3 ns × 1024)) = 89.7 ms => 11 fps.

7. Is it possible to reduce power consumption of the STAR-1000?

Although there is no standby pin on the STAR-1000 sensor, it is still possible to reduce the power consumption. There are two ways to do this. Firstly, implement a kind of standby mode because not all applications need to acquire images all the time. Secondly, reduce the pixel rate (< 12 MHz), but acquire images continuously. Or thirdly combine the first two solutions (lower pixel rate in combination with a standby mode).

The first way to reduce the overall power consumption is to implement a type of standby mode without powering down the whole sensor. The internal ADC has the highest power consumption (it consumes 65% of the total power consumption); in standby mode, the power consumption is reduced to 35% of the normal power consumption by switching off (0 V) the analog ADC supply (VDD_ADC_ANA) during standby. All other supplies should still be supplied with their nominal power level (5 V) and all timing signals should be pulsed continuously during the 'standby' period.

Table 2. Overview Supply Settings for Reduced Power Consumption

Supply Name	Normal Level	'Standby' Level
VDDA	5 V	5 V
VDDD	5 V	5 V
VDD_ADC_ANA	5 V	0 V
VDD_ADC_DIG	5 V	5 V
VDD_DIG_OUT	5 V/3.3 V	5 V/3.3 V
Power consumption	**100%**	**35%**

Note that this power reduction method needs a controllable power supply level for VDD_ADC_ANA (pin 53, 64). The level of this power supply must be switched between 5 V (nominal) and 0 V (standby). After 'standby' when the level of VDD_ADC_ANA is switched back from 0 V to 5 V, it takes at least 1 ms before the STAR-1000 sensor is back in normal operation condition.

The second way to reduce power consumption is to reduce the pixel rate of the STAR-1000 sensor. Lower pixel rate allows higher bias resistor values on some bias nodes, which reduces the bias current and thus the power consumption. Table 3 compares a nominal setting of the bias resistors (12 MHz pixel rate) and bias setting optimized for 3 MHz.

Table 3. Bias Resistor Settings Optimized for Different Pixel Rates

Bias Resistor	Nominal Value (12 MHz)	Optimized Value (3 MHz)
NBIAS_ARRAY	1 M	1 M
NBIAS_DEC	100 k	100 k
NBIAS_OAMP	100 k	400 k
NBIAS_ANA	100 k	400 k
NBAIS_ANA2	100 k	100 k
PBIASDIG2	20 k	20 k
PBIAS	20 k	80 k

The bias settings for other pixel rate frequencies can be recalculated accordingly.

To reduce the power consumption further, combine the two methods (reduced pixel rate and 'standby' period).

8. Does the STAR-1000 have special startup behavior?

Due to the random addressing shift registers of the STAR-1000, the sensor needs to be clocked with the appropriate timing signals immediately after power-on and as long as the sensor is powered on. After power-up, the sensor is in an undefined state. To put the chip in a defined state, the control signals need to be asserted as soon as possible, that is, LD_Y for the Yshift-register and both LD_X and CLK_X for the X shift-register. The address signals, especially CLK_X, should be clocked continuously. If CLK_X is not clocked continuously, the value from the X shift-register will leak and several columns may be selected at once forcing a high current through the columns. This high current causes exceeding power consumption and can damage the sensor.

Document History

Document Title: STAR-1000 Frequently Asked Questions - AN5014
Document Number: 001-16630

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1200303	YIS	See ECN	New application note
*A	3146041	NPA	01/18/2011	Removed table of contents and added document history table
*B	4112285	MTA	9/03/13	Obsolete specs

In March of 2007, Cypress recataloged all of its Application Notes using a new documentation number and revision code. This new documentation number and revision code (001-xxxxx, beginning with rev. **), located in the footer of the document, will be used in all subsequent revisions

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