AN49576

Interfacing ADMUX SRAM Processors to West Bridge® Antioch™

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Associated Project: No
Associated Part Family: CYWB0124AB
Software Version: Antioch™ SDK Version 1.3.2
Related Application Notes: None

Cypress West Bridge® Antioch™ provides High-Speed USB peripheral and mass storage control capabilities to the host processor through its host Processor-port (P-port). This application note presents a physical interconnect example of interfacing a host processor with an address data multiplexed (ADMUX) SRAM interface to Antioch, using Antioch's Pseudo-CRAM P-port interface.

Contents

1 Introduction

The rapid growth of the mobile and embedded device market demands new features and capabilities such as High-Speed USB connectivity and support for the latest mass storage devices. However, the system processor cannot keep in pace with the high speed evolution of new technologies and standards. Cypress West Bridge® Antioch™ (CYBW0124AB) device is the solution to this discrepancy. It is designed to enable handset designers easily add new functionalities in their designs.

When Antioch is integrated into a system, its Processor-port (P-port) interface is used to connect to the system bus of the host processor. The P-port on Antioch supports a conventional interface similar to a SRAM that is compatible with many commonly used embedded processors.

This application note discusses how a system processor can interface to Antioch through Antioch's P-port interface. A host processor with an ADMUX SRAM memory interface is used as an example.

Note that West Bridge Astoria™ natively supports an ADMUX SRAM interface. Further information can be found in the West Bridge Astoria datasheet.

2 West Bridge® Antioch™ Overview

The West Bridge family of controllers uses robust Simultaneous Link to Independent Multimedia (SLIM™) architecture. This provides simultaneous and independent data paths between the processor and USB, USB and mass storage, and processor and mass storage. Antioch is the first device in the West Bridge device family available to the market.

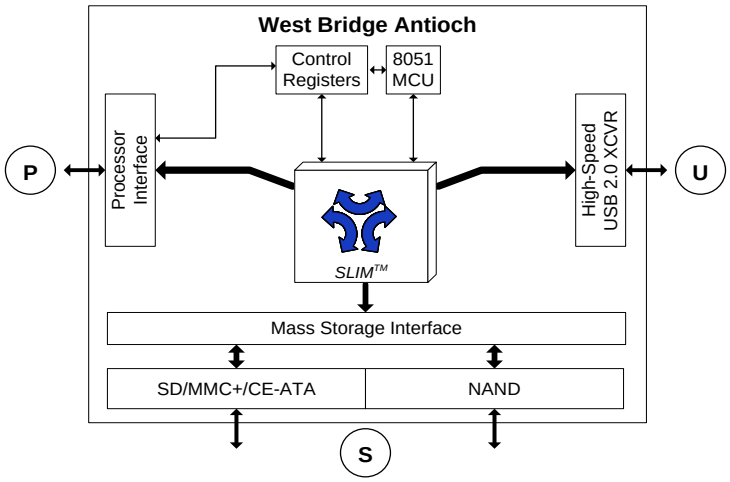
As shown in Figure 1, Antioch has three independent ports: the Processor-port (P-port), the USB-port (U-port), and the mass Storage-port (S-port).

The P-port of Antioch is a conventional interface similar to a SRAM that enables synchronous and asynchronous access to endpoint buffers and configuration registers.

The U-port is a High-Speed USB peripheral interface with a built in transceiver that enables independent U⇔P and U⇔S data transfers with optimal performance.

The S-port can be configured to simultaneously interface with multiple mass storage devices such as 8 or 16-bit raw SLC NAND, controlled NAND, SD/MMC/MMC+, and CE-ATA devices.

Figure 1. West Bridge Antioch Block Diagram



For a full description of Antioch's features, see West Bridge Antioch CYWB0124AB device datasheet.

3 Antioch P-Port Interface

The P-port interface of Antioch is similar to a SRAM interface designed for a simple connection with embedded host processors. Table 1 lists the Antioch P-port signals that need to be considered when connecting to a processor with ADMUX SRAM memory interface.

Table 1. Antioch P-Port Interface Signals

P-port Signal Name	I/O	Function	Comments
CLK	I	Interface Clock Input	Maximum frequency is 33 MHz in synchronous mode. This pin is not needed in asynchronous mode. This pin is not available for WLCSP package.
CE#	I	Chip Enable	
A[7:0]	I	Address Bus	A0 is 16-bit aligned address.
DQ[15:0]	IO	Data Bus	
ADV#	I	Address Latch Enable	
OE#	I	Read Enable	
WE#	I	Write Enable	
INT#	O	Antioch Device Interrupt	
DRQ#	O	DMA Request	This pin is optional if the processor GPIO resource is limited.
DACK#	I	DMA Acknowledgement	This pin is optional if the processor GPIO resource is limited.

Antioch P-port supports both synchronous and asynchronous modes. The operating mode is selected based on the P-port interface configuration register and is default in asynchronous mode.

Note that the CLK pin is not available in wafer level chip scale package (WLCSP). In that case, P-port of Antioch in WLCSP only supports asynchronous accesses.

4 Interface to ADMUX SRAM

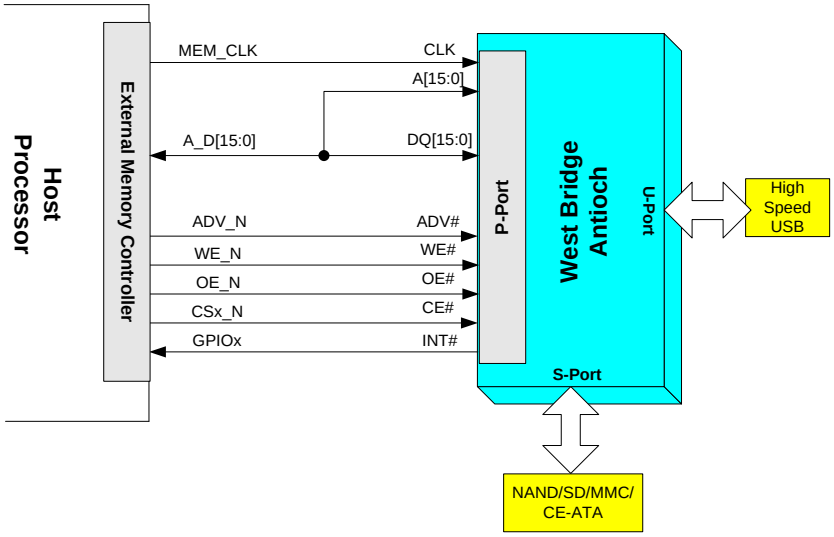
An ADMUX SRAM interface is compatible with Antioch's P-port interface, although its native mode of operation multiplexes address and data lines on the same I/O bus. When connecting Antioch's P-port with dedicated address and data buses to a multiplexed address and data interface, note the following:

- In data phase of the access cycle, data bus also drives the Antioch's address bus. This may latch incorrect address for subsequent access cycles. This is not the case for Antioch, because it enables distinct address cycle when ADV# signal is at logic low. As long as the processor waveform meets timing for address latch cycle (namely tAVS, tAVH and tVP), the value driven on Antioch's address bus during the data phase is ignored.
- During a read operation, the address lines may still be driven by the processor when data is already available from Antioch. This causes bus contention when both the processor and Antioch are trying to drive on the same bus. Avoid this situation by ensuring proper register configuration of the processor's external memory controller.

The timing analysis presented in subsequent sections of this application note covers these two cases.

Most processors' external memory controller enables seamless connection to Antioch's P-port. Figure 2 shows a connection example between a host processor with ADMUX SRAM interface and Antioch.

Figure 2. Connection Example of a Host Processor with Antioch's P-Port



5 Host Processor External Memory Controller Configuration

5.1 Clocking

For both asynchronous and synchronous modes, all external memory control signals are referenced to an internal reference clock (HCLK). The maximum frequency (minimum period) is defined by software, and HCLK is a fractional multiple of the TCXO frequency created by an internal PLL. The control of the circuitry is determined by feature #defines within the software. Assuming the following specifications for HCLK:

Typical HCLK frequency = 48 MHz

That is, HCLK period = 21 ns

In the synchronous mode, the active I/O clock derived from HCLK is output on the CLK pin. This application note assumes that the frequencies of HCLK and CLK are the same. In asynchronous mode, the CLK pin is driven inactive low, although the clock signal is still used as an internal reference to program the different control signals. This application note focuses on asynchronous single access mode of operation.

5.2 Register Configurations

To correctly interface a sample host processor with ADMUX SRAM interface to Antioch, two main memory controller registers must be configured: Fast_CSn_CFG1 and Slow_CSn_CFG0.

Table 2 shows the relevant bit fields for both registers. These registers define the interface timing for the Antioch device.

Table 2. Memory Controller Register Definitions

Register Name	Bit	Symbol	Field	Description	Recommended Value
Fast_CSn_CFG1	5	ah	ADDR_HOLD_ENA	The address is held for an extra cycle to meet hold time requirements with ADV_N. Upon reset, this bit initializes to 0.	0b1
Fast_CSn_CFG1	17:16	aor	ADV_OE_RECOVERY	This bit field indicates the number of cycles elapsed before an OE_N assertion. The reference is with respect to the cycle in which AVD_N is asserted. For example, a value of 2 implies 2 cycles between ADV_N deassertion and OE_N assertion. Reset value is 0x00.	0b01
Slow_CSn_CFG0	27:24	h	WR_HOLD	Write hold. This field specifies the length of the third segment of a write transfer. For example, in a single write transfer, this corresponds to the period from the time that WE_N goes high to the time that CS_N goes high. Power-on default is 0x0.	0b0001
Fast_CSn_CFG1	27:24	h	RD_HOLD	Read hold. This field applies to ANY read transfers that are not caused by the ID_fetch command. It specifies the length of the first segment of the read transfer. For example, in a single read transfer, this corresponds to the period from the time CS_N goes low to the time OE_N goes low. Power-on default is 0x0.	0b0001
Slow_CSn_CFG0	7:4	w	WR_WAIT	These bits determine the number of waitstates incurred in every write access. If BURST_WR_ENA is set (1): * The first access to a page mode memory incurs WR_DELTA + (WR_WAIT + 1) cycles. * Subsequent accesses to a page mode memory incur WAIT_WR + 1 cycles. Reset value is 0x00.	0b0010
Slow _CSn_CFG0	3:0	w	RD_WAIT	These bits determine the number of waitstates incurred in every read access. If PAGE_RD_ENA or BURST_RD_ENA is set (1): * The first access to a page incurs RD_DELTA + (RD_WAIT + 1) cycles. * Subsequent accesses incur WAIT_RD + 1 cycles. Reset value is 0x00	0b0011
Slow _CSn_CFG0	23:16	i	WR_DELTA	Initial latency write. These bits determine the number of extra (delta) cycles inserted in the first write access to a page or burst memory. Upon reset, the delta cycles are inserted in every access to the memory. If CS0 is enabled for Burst accesses, the delta cycles are inserted only in the first access to memory. A minimum value of 1 must be programmed on this bit field. Reset value is 0x0F.	0x0

Register Name	Bit	Symbol	Field	Description	Recommended Value
Slow_CSn_CFG0	15:18	i	RD_DELTA	Initial latency read. These bits determine the number of extra (delta) cycles inserted in the first read access to a page or burst memory. Upon reset, the delta cycles are inserted in every access to the memory. If CS0 is enabled for Page or Burst accesses, the delta cycles are inserted only in the first access to memory. Reset value is 0x0C.	0x0
Slow _CSn_CFG0	31:28	r	RECOVERY	Recovery. This bit field determines how many recovery cycles are inserted from the time the current chip-select is deasserted after a read access to the assertion of the next chip-select. This provides more data recovery time and avoids bus contention. A recovery cycle is an extra cycle inserted in the beginning of the data phase of the next transfer. The chip-select and read and write enable signals are delayed after the recovery cycles. The recovery cycles are inserted under the following conditions: CASE 1: Chip-select turnover 1. The following chip-select signal is different from the current one. 2. The current access to the external memory is a read. CASE 2: Read followed by a write on the same chip-select. 1. The following chip-select signal is the same as the current one. 2. The current access is a read, and the following access is a write. The maximum number of programmable values to this bit field is 15 for 15 cycles of recovery time. Program 0 if the device speed is fast enough (or bus clock speed is slow enough) to eliminate the need for a recovery cycle. The configuration of the bit field is per chip-select basis so you can program device dependent information to the bit field of the configuration register for each chip-select. For a bus-sized transfer, this bit field only affects the first. Reset value is 0x03.	0x0001

Note: Recommended value is set based on timing analysis listed in Table 5 on page 8.

5.3 Timing Analysis and Recommendations

This section provides a timing analysis summary between the sample host processor and Antioch. Table 3 lists the interface timing specifications. Specification values are converted in terms of timing register values for easier calculation of the recommended final program values.

Table 4 lists the Antioch P-port interface timing specifications defined in the Antioch device datasheet.

An accurate one-to-one comparison is necessary between the actual host processor interface and Antioch P-port waveforms. This application note provides an example of this analysis. Figure 3 and Figure 4 show two cases that highlight all the required timings.

Table 5 lists the compatible timing parameters and calculations for the required register configurations. The precautions needed for connecting dedicated address and data buses to a multiplexed address and data interface are described in the timing analysis and avoided with the suggested register settings.

To determine throughput and optimization of the interface with a particular processor, contact your local Cypress sales representative.

Table 3. Memory Controller Interface Timing Specifications

Memory Controller Parameter	Description	Sample Processor Specification	
		Min (ns)	Max (ns)
Write Cycle			
t(csvw)	Write cycle chip-select active	(w+i+h+1)T+/-da	-
t(csw)	Chip-select active to write active	T+/-da	-
t(cswdv)	Chip-select active to data valid	T+/-da	-
t(w)	Write active	(w+i)T+/-da	-
t(wcs)	Write inactive to chip-select inactive	(h)T+/-da	-
t(avw)	Write cycle address valid	(1+ah)T+/-da	-
t(ws)	Write cycle data setup	(w+i)T+/-da	-
t(wh)	Write data hold	(h)T+/-da	-
Read Cycle			
t(avr)	Read cycle address valid	(1+ah)T+/-da	-
t(r)	Read active	(w+i)T+/-da	-
t(csvr)	Read cycle chip-select active	(w+i+1)T+/-da	-
t(csr)	Chip-select active to read active	(1+aor)T+/-da	-
t(csi)	Chip-select inactive	(r)T+/-da	-
t(oeh)	Read inactive to chip-select inactive	(h)T+/-da	-
t(rh)	Read-data hold	0	-
t(rs)	Read-data setup	20	-

Note: T = HCLK Period, that is, 21 ns.

Note: da = 3 ns. This parameter defines the skew measured with respect to two signals.

Table 4. Antioch P-Port Interface Timing Specifications

Antioch Parameter	Description	Antioch Specification	
		Min (ns)	Max (ns)
tAVS	Address Valid to ADV# High	5	-
tAVH	ADV# High to Address Hold	2	-
tCVS	CE# Low Setup to ADV# High	5	-
tVP	ADV# Low Pulse Width	7.5	-
tEA	CE# Low to Data Valid	-	30
tOE	OE# Low to Data Valid	-	22.5
tOLZ	OE# Low to Data Low-Z	3	-
tOHZ	OE# High to Data High-Z	0	22.5
tWP	WE# Low Pulse Width	22	-
tWPH	WE# High Pulse Width	10	-

Antioch Parameter	Description	Antioch Specification	
		Min (ns)	Max (ns)
tCW	CE# Low to Write End	30	-
tAW	Address Valid to Write End	30	
tDW	Data Setup	18	
tDH	Data Hold	0	

Figure 3. Asynchronous Single Read Timing (Antioch versus Sample Processor)

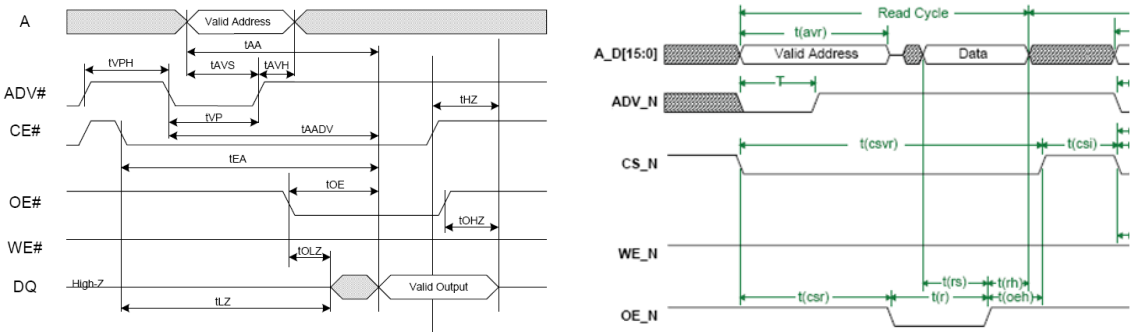


Figure 4. Asynchronous Single Write Timing (Antioch versus Sample Processor)

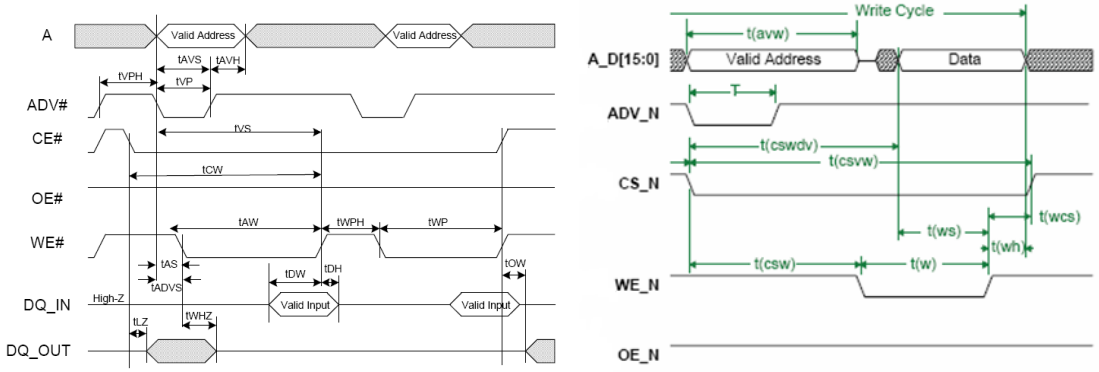


Table 5. Antioch and Sample Processor Timing Analysis and Calculations

Timing	Antioch Name	Description	Sample Processor Parameter	Recommended Configuration
Read Parameters	tEA - tOE+ OE# Low pulse + tOHZ	Read Cycle Time	t(csvr)+t(csi)	tEA-tOE+t(r)+tOHZ < t(csvr)+t(csi) => 30-22.5+(w+i)*T+da+22.5 < (w+i+1)*T-da +r*T-da => 30<(r+1)*T-3*da => 30<(r+1)*21-9 => r = 1
	tEA -tOE	CE# Low to OE# Low	t(csr)	tEA-tOE < (1+aor)*T-da => 30-22.5 < (1+aor)*21-3 => aor = 0 However, aor must increase to 1 to avoid contention.
	OE# Low pulse- tOE + 2*board_delay	DQ output setup to OE# High	t(rs)	t(r)-tOE+2*1 > t(rs) => (w+i)*T-da - 22.5 +2 > 20 => (w+i)*21-3-22.5+2>20 => i = 0; w = 3
	tOHZ + 2*board_delay	OE# High to DQ Hold	t(rh)	tOHZ+2*1 > 0 Condition always met.
Write Parameters	tWPH + tWP	Write Cycle Time	t(csvw)	tWPH+tWP < (w+i+h+1)*T-da => 22+10 < (w+i+h+1)*21-3 => i=0; w=2; h=1
	tCW - tAW	CE# Low to WE# Low	t(csw)	tCW-tAW < T-da => 30-30 < 21-3; Condition always met.
	tAW	WE# Low pulse width	t(w)	tAW < (w+i)*T-da => 30 < (w+i)*21-3 => i=0; w=2
	tDW	DQ input setup	t(ws)	tDW < (w+i)*T-da => 18 < (w+i)*21-3 => i=0; w=2
	tDH	DQ input hold	t(wh)	tDH < h*T-da => 0 < h*21-3 => h=1
Common for both Read and Write	tAVS	Address valid to ADV# High	T (i.e. 1 HCLK Cycle)	HCLK=21ns; tAVS=5ns; Condition always met.
	tAVH	ADV# High to Address hold	t(avr) - T	tAVH < (1+ah)*T-da-T => 2 < (1+ah)*21-3-21 => ah = 1
	tCVS	CE# Low to ADV# HIGH	T (i.e. 1 HCLK Cycle)	HCLK=21ns; tCVS=5ns; Condition always met.
	tVP	ADV# Low Pulse Width	T (i.e. 1 HCLK Cycle)	HCLK=21ns; tVP=7.5ns; Condition always met.

Note: Assume board delay of 1 ns.

Note: It requires t(csr) - tOLZ >= t(avr) to avoid data contention during read operation. That is, (1+aor)*T-da-3>= (1+ah)*T+da, based on calculation ah=1 and aor=0, which fails the condition. The aor value must increase by one cycle to avoid contention.

6 Summary

West Bridge Antioch can easily interconnect with host processors through ADMUX SRAM memory interface. The timing analysis described in this application note lists the modes of operation supported with Antioch. The Antioch feature set is a perfect solution for host processors to enable new High-Speed USB peripheral connectivity and storage control options for the latest mass storage devices. It also completely offloads the processor from the USB mass storage access, resulting in higher performance and more efficient system design.

7 Additional Resources

- West Bridge® Antioch Advance Datasheet
- West Bridge® Astoria Advance Datasheet

Document History

Document Title: AN49576 - Interfacing ADMUX SRAM Processors to West Bridge® Antioch™

Document Number: 001-49576

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2590750	HKH	10/16/2008	New Application Note.
*A	3183676	ANOP	02/25/2011	Added a note in Introduction section. Added Additional Resources section.
*B	3426442	AASI	10/31/2011	Updated to new template. Completing Sunset Review.
*C	4556630	PRJI	10/30/2014	Updated to new template. Completing Sunset Review.
*D	4823648	MDDD	07/04/2015	Updated the hyperlinks Updated template
*E	5839372	RUPA	08/01/2017	Updated Cypress logo and Copyright information.

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