# AN49081

## Requirements for Input Clock to West Bridge® Devices

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AN49081 addresses the requirements for the input clock to West Bridge® devices that includes Antioch™, Astoria™, and TX3LP18. The conversion of phase noise specifications into equivalent RMS jitter is also discussed.

## Introduction

This document addresses the input clock requirements for three devices in the West Bridge® family of products: Antioch, Astoria, and TX3LP18. The computation of equivalent RMS jitter from phase noise characteristics is also discussed.

The West Bridge® Antioch™ and Astoria™ devices are peripheral controllers that support High-Speed USB and mass storage access. These controllers provide access from both a processor interface and a High-Speed USB interface to peripherals that include SD, MMC/MMC+, CE-ATA, SDIO, and NAND.

The MoBL-USB™ TX3LP18 is a low voltage High-Speed USB 2.0 ULPI Transceiver.

The three devices have the same requirements for the input clock, which are discussed in this application note.

## Input Clock Requirements

The three West Bridge devices each support a subset (four) of the following input frequencies: 13 MHz, 19.2 MHz, 24 MHz, 26 MHz, 38.4 MHz, and 48 MHz.

The critical requirements for the input clock to these West Bridge devices are:

- Phase noise requirements
- Maximum frequency deviation
- Maximum rise and fall time
- Square wave signal

Table 1 lists the specifications for these requirements.

Table 1. Input Clock Specifications for West Bridge Devices

| Parameter | Description | Specification | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Phase noise | 100 Hz Offset | - | -75 | dBc/Hz |
| | 1 kHz Offset | - | -104 | dBc/Hz |
| | 10 kHz Offset | - | -120 | dBc/Hz |
| | 100 kHz Offset | - | -128 | dBc/Hz |
| | 1 MHz Offset | - | -130 | dBc/Hz |
| Maximum frequency deviation | | - | 150 | ppm |
| Duty cycle | | 30 | 70 | % |
| Overshoot | | - | 3 | % |
| Undershoot | | - | -3 | % |
| Rise time | | - | 3 | ns |
| Fall time | | - | 3 | ns |

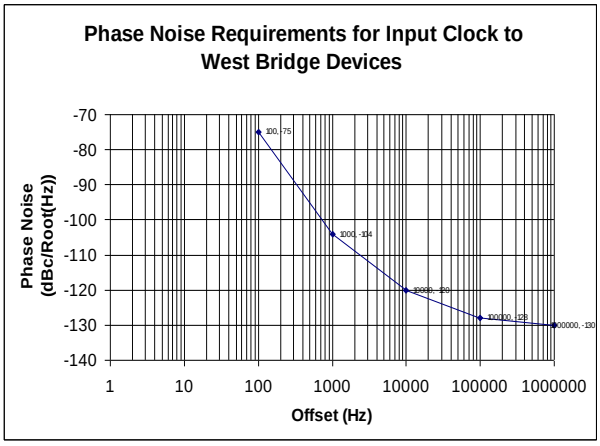
An input clock supplied to a West Bridge device must meet the requirements specified in Table 1.

Some clock manufacturers specify RMS jitter rather than phase noise characteristics. Phase noise characteristics may be directly converted into the equivalent RMS jitter. This is explained in the next section.

## Computation of RMS Jitter from Phase Noise

The phase noise specifications in Table 1 are precise measurements for the input clock quality. The equivalent RMS jitter requirement can be derived from the phase noise specifications. The input noise specifications listed in Table 1 are converted into a graph in Figure 1.

Figure 1. Phase Noise Requirements for Input Clock to West Bridge Devices




The RMS jitter that can be tolerated is a function of the area under the curve that is shown in Figure 1.

$$RMSJ_{per}\vdots_{f_1 to f_2} = \frac{1}{2\pi fc}\sqrt{2\int_{f_1}^{f_2} 10^{\frac{L(f)}{10}}\,df} \quad \text{Equation 1}$$

In Equation 1:

L(f) = Phase Noise Spectrum

$J_{per}$ = Period Jitter

$f_1$-$f_2$ is the frequency band of interest.

Since the frequency axis of the phase noise spectrum shown in Figure 1 is in log scale, the RMS period jitter is approximated as a piecewise linear function of L(f) that is summed up from a provided curve as shown in the same figure.

The RMS jitter is derived from the following equations:

$$RMSJ_{per} = \frac{1}{2\pi fc}\sqrt{2\sum_{i=1}^{K-1} 10^{\frac{b_i}{10}} f_i^{-\frac{a_i}{10}} \int_{f_i}^{f_{i+1}} f^{\frac{a_i}{10}}\,df} \quad \text{Equation 2}$$

or

$$RMSJ_{per} = \frac{1}{2\pi fc}\sqrt{2\sum_{i=1}^{K-1} 10^{\frac{b_i}{10}} f_i^{-\frac{a_i}{10}}\left[\frac{a_i}{10}+1\right]^{-1}\left[f_{i+1}^{\frac{a_i}{10}+1} - f_i^{\frac{a_i}{10}+1}\right]} \quad \text{Equation 3}$$

In Equation 2 and Equation 3:

$$a_i = (L(f_{i+1}) - L(f_i))/(\log(f_{i+1}) - \log(f_i)) \quad \text{Equation 4}$$

$$b_i = L(f_i) \quad \text{Equation 5}$$

In these equations, $L(f_i)$ is the value of the phase noise spectrum at any frequency, and $f_i$. $a_i$ is the slope of the phase noise spectrum between frequencies $f_i$ and $f_{i+1}$. From Equation 1 to Equation 5, RMS jitter is calculated from the phase noise spectrum plot.

## RMS Jitter Requirements

The internal PLL of the West Bridge devices is sensitive to phase noise over the frequency range of 100 Hz to 5 MHz. By integrating the piecewise linear form of the input phase noise characteristics over the frequency range of 100 Hz to 5 MHz, the equivalent RMS jitter requirements are obtained. The RMS jitter requirement for the different input frequencies is calculated and listed in Table 2.

Table 2. Maximum RMS Jitter for Valid Input Frequencies

| Number | Input Freq (MHz) | Maximum RMS Jitter (ps) |
|---|---|---|
| 1 | 13 | 25.81 |
| 2 | 19.2 | 17.47 |
| 3 | 24 | 13.98 |
| 4 | 26 | 12.90 |
| 5 | 38.4 | 8.74 |
| 6 | 48 | 6.99 |

## Summary

This application note addresses the requirements of the input clock to West Bridge devices Antioch, Astoria, and TX3LP18. The conversion from phase noise to equivalent RMS jitter is also discussed. This conversion is applied to the input phase noise specification. The equivalent RMS jitter numbers are derived for all input clock frequencies.

## Document History

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| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 2571675 | OSG / AESA | 09/27/2008 | New application note. |
| *A | 3412955 | HBM | 10/18/2011 | Updated to new template.<br>Completing Sunset Review. |
| *B | 4556107 | PRVE | 10/30/2014 | Updated to new template.<br>Completing Sunset Review. |
| *C | 5839085 | AESATP12 | 07/31/2017 | Updated logo and copyright. |

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