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Spec No: 001-48903

Spec Title: AN48903 - EXTERNAL EEPROM FIRMWARE LOAD FOR WEST BRIDGE(R) ASTORIA(TM)

Sunset Owner: Rama Sai Krishna Vakkantula (RSKV)

Replaced By: NONE

External EEPROM Firmware Load for West Bridge® Astoria™

AN48903

Author: Kevin Reed
Associated Project: No
Associated Part Family: CYWB0224ABM, CYWB0224ABS
Software Version: None
Associated Application Notes: None

Abstract

West Bridge® Astoria™ is a USB mass storage control device. It contains three main ports: Processor Interface (P-port), Mass Storage Support (S-port), and USB Interface (U-port). AN48903 discusses how to load the Astoria firmware using an external EEPROM.

Introduction

The West Bridge® Astoria™ device (CYWB0224ABM/ CYWB0224ABS) is a peripheral controller that supports High Speed USB and mass storage access. Astoria provides access from both a processor interface and a High Speed USB (HS-USB) interface to peripherals such as SD, MMC/MMC+, CE-ATA, and NAND. It also supports interleaving accesses between the processor interface, the HS-USB, and storage-port (S-port). This enables the simultaneous transfer of data between both a processor and a USB host, and the mass storage peripherals.

The firmware for Astoria is usually loaded from the processor on the P-port. Alternatively, when the system requires Astoria to self boot, the firmware of West Bridge® Astoria™ can be loaded using an external EEPROM. For example, in a USB thumb drive (flash disk) application, Astoria must work standalone and boot from a USB Mass Storage Class (USBMSC) firmware. In this case, the USBMSC firmware is preprogrammed into the EEPROM and used to boot Astoria upon power up, without any connectivity to a system processor.

Astoria supports multiple Processor port (P-port) modes. The I2C EEPROM boot is supported in extended P-port modes of operation. The extended P-port modes supporting EEPROM boot are: SPI, PNAND (all 8 modes of PNAND), and Address Data Multiplexing (ADM). The following sections describe how to successfully conduct an EEPROM load of the Astoria firmware.

Astoria EEPROM Connection

Table 1. Sample EEPROM Parts

Bytes	EEPROM
4 K	24LC32
8 K	24LC64
16 K	24LC128
32 K	24LC256

1. Configure Astoria in one of the Extended Input Modes (EIM) listed in Table 2 on page 2. This activates the I2C interface (SCL and SDA pins) available on the P-port.
2. Connect the EEPROM to Astoria's I2C interface.
3. An external pull up resistor to PVDDQ is required on both the SCL and SDA lines. The typical recommended value is 2.2 KΩ.
4. Allow the SDA pin to disconnect from Astoria by adding a switch or jumper. This disables the EEPROM boot so that the EEPROM can be programmed in system. Ensure the pull up resistor is left on the Astoria side of this connection.
5. The EEPROM must function at the PVDDQ Voltage level (1.8 V, 2.5 V or 3.3 V).
6. Use EEPROM address pins A2, A1, and A0 to indicate that the EEPROM is double byte addressed (001).

Table 2: Extended Processor Port Interface Mode Options

EIM (Extended Interface Modes)						
TEST[2]	**TEST[1]**	**TEST[0]**	**A[7]**	**A[3]**	**A[2]**	**Modes**
0	1	0	1	0	0	PNAND Mode – Small Block Device
0	1	0	0	0	0	PNAND Mode – Large Block Device
0	1	0	1	1	0	SPI Mode
0	1	0	1	0	1	ADM Mode (Pseudo CRAM)

In System Programming of EEPROM

There are two options for programming an EEPROM. The EEPROM is preprogrammed and dropped into the system, or it is programmed in the system using Astoria's Debug mode.

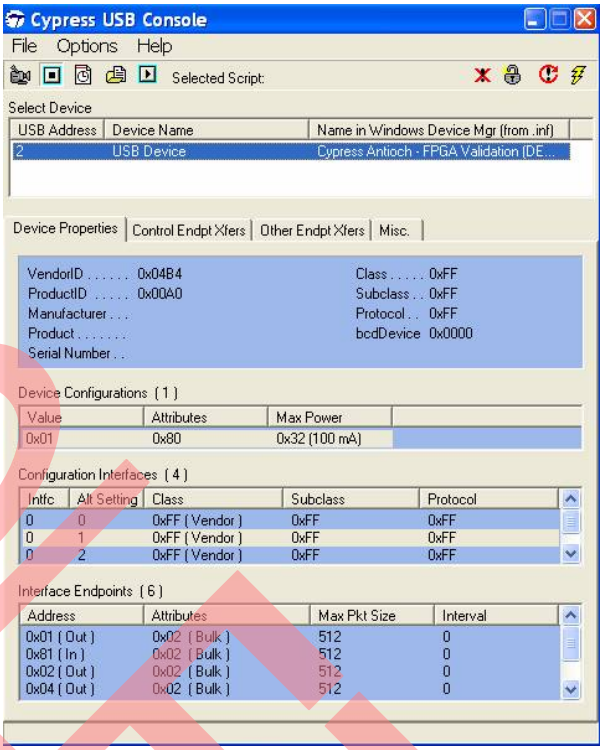
1. To use in system programming, the following components are required:

   - CYConsole.exe software tool
   - Valid firmware in .iic format for booting

   The firmware image is provided by Cypress. IIC format is a raw binary image of the firmware with an added Cypress proprietary header that configures the I2C boot loader. The CYConsole software is included on the Astoria Development Kit (DVK) CD and through Cypress's corporate website.

2. When Astoria is configured in one of the EIM modes, place Astoria in Debug by setting TEST[0] pin to High. The Debug mode enables Astoria's SIE to automatically enumerate through USB without firmware. This enables a firmware download.
3. Disconnect the SDA line from the EEPROM to Astoria.
4. Launch CYConsole utility.
5. Power on the Astoria board and connect USB cable to the host PC. Windows recognizes Cypress USB device. CYConsole recognizes a West Bridge USB Device. This is shown in Figure 1.

Figure 1. West Bridge USB Device Recognized



6. If the Hardware Update Wizard is displayed, follow these steps. This procedure is required only for first time connections.

   - Select "No, not this time".
   - Select "Install Hardware from specified location".
   - Use the file browser to find the folder containing the CYUSB.INF. This is available on the DVK CD in the USB_drivers folder.

7. After the Astoria USB device is recognized on the PC, reconnect the EEPROM SDA line to Astoria.
8. From the Options menu in CYConsole, choose "EZ USB Interface".
9. Click the LgEEPROM button. A file browser opens.
10. Navigate through the file browser to the location of your firmware file in .iic format and load the file. The CYConsole provides the status of the downloaded file. A successful EEPROM firmware load is shown in Figure 2 on page 3.

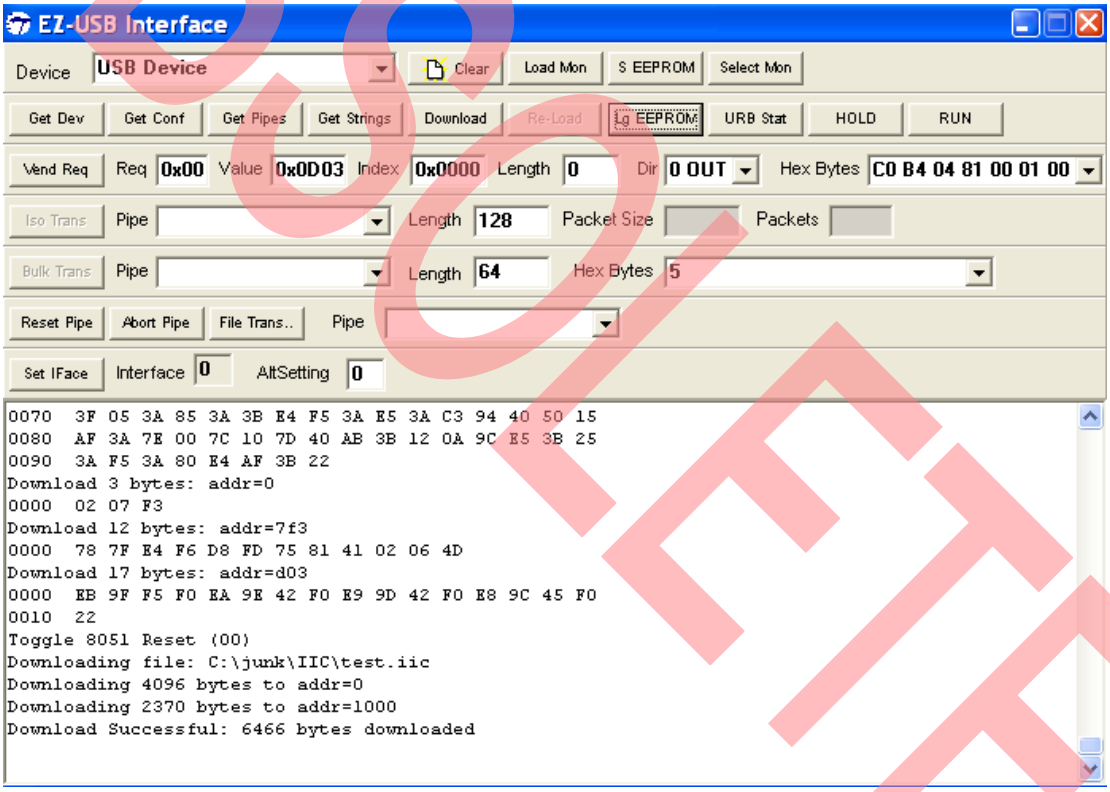
Booting from EEPROM

1. After the EEPROM is correctly loaded with the firmware, configure Astoria to boot from EEPROM. To enable the EEPROM boot mode, the Astoria P-port must be configured to one of the extended interface modes. If any other mode is selected, Astoria does not attempt to boot from EEPROM.
2. Ensure the EEPROM is connected to Astoria through both the SDA and SCL lines.
3. After Astoria is configured in one of the EIM and taken out of reset, it probes for an EEPROM on the I2C bus. If an EEPROM is present, Astoria expects 0xC2 in the first byte to indicate if there is firmware for the Astoria. If this byte is not found or if EEPROM is not correctly connected to the I2C bus, Astoria idles and waits for an alternative method of loading firmware.
4. The I2C bus frequency defaults to 100 kHz for compatibility and it can be configured to run at 400 kHz for devices that support the higher speed. The .iic file provided by Cypress includes header information for a 400 kHz configuration.
5. After Astoria receives the 0xC2 byte from the EEPROM, it automatically loads the firmware into the internal program memory. Astoria then executes the firmware loaded from the EEPROM.

Reprogramming EEPROM

To reprogram EEPROM, follow the steps provided in the section In System Programming of EEPROM on page 2.

Figure 2. Successful EEPROM Load



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Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2569256	KFR/AESA	09/24/2008	New application note.
*A	3353408	ODC	08/24/2011	No technical updates. Completing sunset review.
*B	4184440	RSKV	11/06/2013	Obsolete document.

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