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Spec Title: INTERFACING TI OMAPV1030 PROCESSOR TO CYPRESS WEST BRIDGE(R) ANTIOCH(TM) - AN47994

Sunset Owner: Dhanraj Rajput (DBIR)

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Interfacing TI OMAPV1030 Processor to Cypress West Bridge® Antioch™

AN47994

Author: Hingkwan Huen
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Application Note Abstract

Cypress West Bridge® Antioch™ device provides high speed USB peripheral and mass storage control capabilities to the system processor through its host processor port. This application note presents a system example of interfacing a TI OMAPV1030 baseband processor to an Antioch device, using Antioch's Pseudo-CRAM processor-port (P-port) interface.

Introduction

The rapid growth of the mobile and embedded device market demands new features and capabilities such as high speed USB connectivity and mass storage control with the latest memory types. However, the new technologies and standards evolve at a very fast rate that a system processor cannot keep up with. As a result, the Cypress West Bridge® Antioch™ (CYBW0124AB) device is designed to enable handset designers to easily add these new functionalities in their designs.

When Antioch is integrated into a system, its host processor interface (P-port) is used to connect to the system bus of the principal processor. The P-port of Antioch supports a conventional interface that is similar to SRAM. This is compatible with many commonly used embedded processors.

This application note uses the TI OMAPV1030 processor as an example to describe how a system processor can interface to Antioch through Antioch's P-port interface.

West Bridge Antioch Overview

The West Bridge family of controllers uses robust simultaneous link to independent multimedia (SLIM™) architecture, which provides simultaneous and independent data paths between the processor and USB, USB and mass storage, and the processor and mass storage. Antioch is the first device in the West Bridge device family that is available to the market.

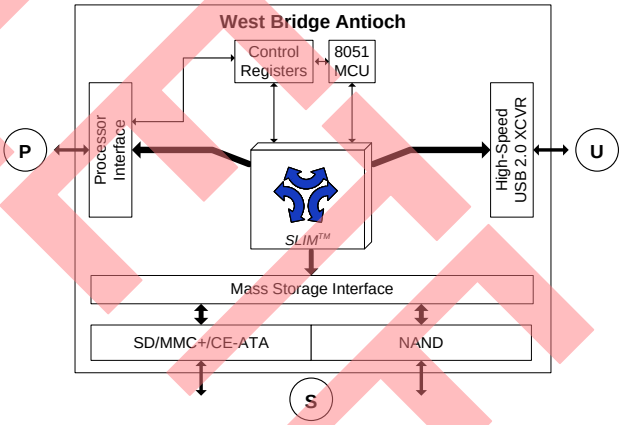
Antioch has three independent ports: the processor-port (P-port), the USB-port (U-port), and the mass storage-port (S-port). This is shown in Figure 1.

The P-port of Antioch is a conventional interface that is similar to SRAM. This interface allows synchronous and asynchronous access to endpoint buffers and configuration registers.

The U-port is a High-Speed USB peripheral interface with built in transceiver that allows independent U⇔P and U⇔S data transfer with optimal performance.

The S-port can be configured to simultaneously interface with multiple mass storage devices such as 8 or 16-bit SLC NAND, Managed NAND, SD/MMC/MMC+, and CE-ATA devices.

Figure 1. West Bridge Antioch Block Diagram



For a full description of Antioch features, refer to the West Bridge™ Antioch CYWB0124AB device data sheet.

Antioch P-Port Interface

The P-port interface of Antioch is similar to an SRAM interface and is designed for a simple connection with typical embedded processors. Table 1 lists the Antioch P-port signals that are considered when connecting to a TI OMAPV1030 processor.

Table 1. Antioch P-Port Interface Signals

P-Port Signal Name	IO	Function	Comments
CLK	I	Interface clock input	Maximum frequency is 33 MHz in synchronous mode. This pin is not needed in asynchronous mode. This pin is not available for WLCSP package.
CE#	I	Chip enable	-
A[7:0]	I	Address bus	A0 is 16-bit aligned address.
DQ[15:0]	IO	Data bus	-
ADV#	I	Address latch enable	-
OE#	I	Read enable	-
WE#	I	Write enable	-
INT#	O	Antioch device interrupt	-
DRQ#	O	DMA request	This pin is optional if the processor GPIO resource is limited.
DACK#	I	DMA acknowledgement	This pin is optional if the processor GPIO resource is limited.

Antioch P-port supports both synchronous and asynchronous modes. The operating mode is selected based on the P-port interface configuration register, which is default in asynchronous mode.

Note that the CLK pin is NOT available in wafer level chip scale package (WLCSP). In this case, the P-port of Antioch in WLCSP supports only asynchronous accesses.

Interface to OMAPV1030

The OMAPV1030 E-GPRS baseband processor belongs to the Texas Instruments OMAP-Vox processor family. It combines a communication engine, an application engine, and a digital signal processing (DSP) subsystem. The DSP subsystem delivers enhanced multimedia performance and communication capability for handset designers who want to develop a cost efficient GSM/GPRS/EDGE solution for mainstream wireless users.

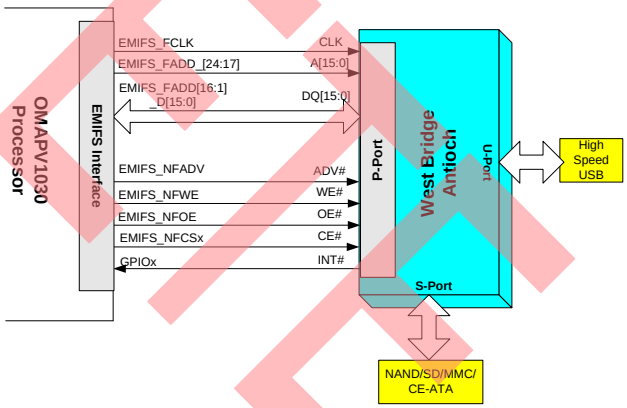
Among OMAPV1030's memory interfaces, the external memory interface slow (EMIFS) is used to manage 8 or 16-bit data access between external memories (for example, common flash, ROM, and SRAM) and the processor. The EMIFS interface is compatible with Antioch's P-port interface, although its native mode of operation multiplexes the lower 16-bit addresses with the data lines on the same IO bus. Upper address pins EMIFS_FADDR[24:17] are dedicated on the OMAPV1030, which can be used to interface with Antioch's address bus A[7:0]. Antioch's base address mapped to the processor's system bus must be properly converted before every Antioch endpoint buffer or register access. For example, assuming that the processor address is byte addressable, a 16-bit read access from EP8 (Antioch address 0x8) buffer must be similar to:

```
data_val = readw(ANTIOCH_BASE + (0x8 << 17) );
```

Among the four chip select pins of OMAPV1030 EMIFS, CS0 is dedicated to internal memory space and not available on the external interface. You can use three other chip selects, EMIFS_NFCS[3:1], for Antioch.

The OMAPV1030's embedded EMIFS interface allows seamless connection to Antioch's P-port. Figure 2 shows a connection example between the OMAPV1030 processor and Antioch.

Figure 2. Example of a Connection between OMAPV1030's EMIFS Interface and Antioch's P-Port



OMAPV1030 NFC Interface Configuration

Clocking

For asynchronous and synchronous modes, all EMIFS control signals are referenced to an internal EMIFS reference clock (REF_CLK). The REF_CLK is divided from the traffic controller (TC) clock by a programmable value in the FCLKDIV bit field of the EMIFS chip select configuration register (EMIFS_CSx_CONFIG). This application note uses:

Typical REF_CLK frequency = 65 MHz

That is, REF_CLK period = 15.4 ns

In the synchronous mode, the active EMIFS clock is output on the EMIFS_FCLK pin. In asynchronous mode, the EMIFS_FCLK pin is driven inactive low, although the clock signal is still used as an internal reference to program the different control signals.

The OMAPV1030 processor issues only linear, incrementing, and fixed size of 4 x 32-bit access bursts (or 8 x 16-bit bursts). Burst access is aligned on the burst size address boundary (that is, the burst LSB address A[3:0] always starts at 0b0000). This requires external devices operated in synchronous mode to have burst protocol programming to conform to the EMIFS burst protocol. The current Antioch software API does not support this feature yet. As a result, the EMIFS configurations and timing analysis provided in this application note only focuses on asynchronous single access mode of operation.

Register Configurations

To interface OMAPV1030 correctly to Antioch, two main EMIFS registers must be configured: the EMIFS Chip Select Configuration (EMIFS_CCSx), and the Advanced EMIFS Chip Select Configuration (EMIFS_ACSx) Registers.

Table 2 lists the EMIFS_CCSx Register bit definitions. Table 3 on page 4 lists the EMIFS_ACSx Register bit definitions. There is one set of EMIFS_CCSx and EMIFS_ACSx registers for each chip select. These registers define the EMIFS configurations and interface timing for the Antioch device.

Table 2. OMAPV1030 EMIFS_CCSx Register Definitions

Bit	Field	Description	Recommended Value
31	PGWSTEN	0: PGWST (Page mode wait states) is specified by bits 15:12. 1: PGWST (Page mode wait states) is specified by bits 30:27.	0b1
30:27	PGWST	When in asynchronous page mode, (PGWST + 1) * REF_CLK specifies the access time for accesses within a page (the delay between successive words within the page or in-page wait states).	0b0000
26:23	BTWST	Controls the idle time in between processor cycles. Control signals are de-asserted during this time. Idle time is (BTWST +1) * TC_CK.	0b0000
22	MAD	0b1 (Multiplexed protocol) is the only possible value for EMIFS_NFCS[3:1]	0b1
21	Reserved	Must be 0b0	0b0
20	BW	Controls the data bus width for this chip select. 0: 16-bit data bus 1: 32-bit data bus	0b0
19	Reserved	Must be 0b0	0b0
18:16	RDMODE	Read mode select 000: Mode 0 – Asynchronous read 001: Mode 1 – Page mode read. 4 words per page. 010: Mode 2 – Page mode read. 8 words per page. 011: Mode 3 – Page mode read. 16 words per page. 100: Mode 4 – Synchronous burst read. TI burst protocol compliant. 101: Mode 5 – Synchronous burst read. Intel Smart3 protocol compliant. 110: Reserved 111: Mode 7.Synchronous burst read (CS0 only)	0b000
15:12	PGWST/WELEN	Controls the wait-states cycle number between accesses in a page for asynchronous page mode. Controls the WE pulse length during a write access. When PGWSTEN is 0, this bit specifies both PGWST/WELEN. When PGWSTEN is 1, this bit specifies only WELEN.	0b0010
11:8	WRWST	Controls the wait-states cycle number for write operation	0b0000

Bit	Field	Description	Recommended Value
7:4	RDWST	Controls the wait-states cycle number for asynchronous read operation and the initial idle time for asynchronous read page mode and synchronous read mode.	0b0010
3	Reserved	Reserved. Writing to this bit has no effect; Reading it returns undefined value.	0b0
2	RT	Enables the read retimed protocol. This bit may be 1 only in RDMODE 4, 5, and 7. The system hangs if the retiming bit is set to other modes. 0: Non retimed protocol 1: Retimed protocol	0b0
1:0	FCLKDIV	In all modes of operation, all EMIFS to memory control signals and timing are referenced to REF_CLK. REF_CLK is divided from TC_CK (traffic controller clock) by the value contained in the FCLKDIV bit field. 00: REF_CLK = TC_CK divided by 1 01: REF_CLK = TC_CK divided by 2 10: REF_CLK = TC_CK divided by 4 11: REF_CLK = TC_CK divided by 6	Assuming TC_CK is 130 MHz; 0b01

Note
Recommended value is set based on the timing analysis listed in Table 6 on page 7.

Table 3. OMAPV1030 EMIFS_ACSx Register Definitions

Bit	Field	Description	Recommended Value
31:10	Reserved	Reserved. Must be written to 0 and read value must be considered undefined.	0
9	BTMODE	Enables extended BTWST usage. 0: Bus turn around control and RD to RD/WR same CS pulse width high control 1: Bus turn around control and RD/WR to RD/WR same CS pulse width high control. BTMODE 0 implies that in some cases, for example, burst write accesses, the chip select signal is not activated. In this example, BTMODE is configured to 1 for safest operation and to make sure that the chip select signal is deactivated between accesses.	0b1
8	ADVHOLD	Controls the ADV pulse width low. ADV pulse width equals (ADVHOLD + 1) * REF_CLK.	0b0
7:4	OEHOLD	Controls the time from OE high to CS high. (OEHOLD) * REF_CLK is the time from OE high to CS high. Note that because CS minimum pulse width is 2 * REF_CLK, OESETUP must be set so that (OESETUP + OEHOLD) is ≤ RDWST. If this rule is violated the processor produces a bad access completion.	0b0000
3:0	OESETUP	Controls the time from CS low to OE low. Time from CS low to OE low is (OESETUP) * REF_CLK. Note that because the CS minimum pulse width is 2 * REF_CLK, OESETUP must be set so that (OESETUP + OEHOLD) is ≤ RDWST. If this rule is violated the processor produces a bad access completion.	0b0001

Note
Recommended value is set based on timing analysis listed in Table 6 on page 7.

Timing Analysis and Recommendations

This section provides timing analysis summaries of OMAPV1030 and Antioch.

Table 4 shows the OMAPV1030 EMIFS interface timing specifications defined in the processor TRM. Specification values are converted in terms of timing register values for easier calculation of the recommended final program values.

Table 5 shows the Antioch P-port interface timing specifications defined in the Antioch device data sheet.

An accurate one-to-one comparison is necessary between OMAPV1030 EMIFS interface and Antioch P-port waveforms.

Figure 3 and Figure 4 show two cases that highlight all the required timings.

Table 6 on page 7 presents the compatible timing parameters and calculations for the required register configurations. Based on these calculations, the recommended OMAPV1030 EMIFS interface register settings are:

- EMIFS_CCSx = 0x80402021
- EMIFS_ACSx = 0x00000201

To determine the throughput and optimization of the interface with a particular processor and further information, contact your local Cypress sales representative.

Table 4. OMAPV1030 NFC Interface Timing Specifications

Symbol	OMAPV1030 Parameter	Description	OMAPV1030 Spec	
			Min (ns)	Max (ns)
F1	tw(CSV)	EMIFS_NFCSx low duration - Read operation	(RDWST+2)*REF_CLK -3	(RDWST+2)*REF_CLK -3
F17	td(CSV-OEV)	EMIFS_NFCSx low to EMIFS_NFOE low	OESETUP*REF_CLK -2	OESETUP*REF_CLK + 4
F4	td(CSV-OEIV)	EMIFS_NFCSx low to EMIFS_NFOE high	(RDWST-OEHOLD+2)* REF_CLK - 2	(RDWST-OEHOLD+2) * REF_CLK + 4
F5	tsu(DV-OEH)	Read data valid before EMIFS_NFOE high	+14	-
F6	th(OEH-DV)	Read data valid after EMIFS_NFOE high	0	-
F23	tw(CSV)	EMIFS_NFCSx low duration - Write operation	(WRWST+WELEN+3) * REF_CLK - 3	(WRWST+WELEN+3) * REF_CLK + 3
F25	tw(CSV-WEV)	EMIFS_NFCSx low to EMIFS_NFWE low	(WRWST+1) * REF_CLK - 2	(WRWST+1) * REF_CLK + 5
F27	tw(WEIV-CSIV)	EMIFS_NFWE high to EMIFS_NFCSx high	REF_CLK-5	REF_CLK+2
F30	td(DIV-CSIV)	Data bus invalid to EMIFS_NFCSx invalid	-2	+3
F3	td(CSV-ADIV)	EMIFS_NFCSx valid to EMIFS_NFADV high	(ADVHOLD+1)*REF_CLK-2	(ADVHOLD+1)*REF_CLK+2 2
F9	td(AV-CSV)	Address valid to EMIFS_NFCSx low	-4	+4
F12	td(ADV-CSV)	EMIFS_NFADV low to EMIFS_NFCSx low	-2	+2

Table 5. Antioch P-Port Interface Timing Specifications

Antioch Parameter	Description	Antioch Spec	
		Min (ns)	Max (ns)
tAVS	Address valid to ADV# high	5	
tAVH	ADV# high to address hold	2	
tCVS	CE# low setup to ADV# high	5	
tVP	ADV# low pulse width	7.5	
tEA	CE# low to data valid		30
tOE	OE# low to data valid		22.5
tOHZ	OE# high to data high-Z	0	22.5
tWP	WE# low pulse width	22	
tWPH	WE# high pulse width	10	
tCW	CE# low to write end	30	
tAW	Address valid to write end	30	
tDW	Data setup	18	

Antioch Parameter	Description	Antioch Spec	
tDH	Data hold	0	

Figure 3. Asynchronous Single Read Timing (Antioch vs. OMAPV1030)

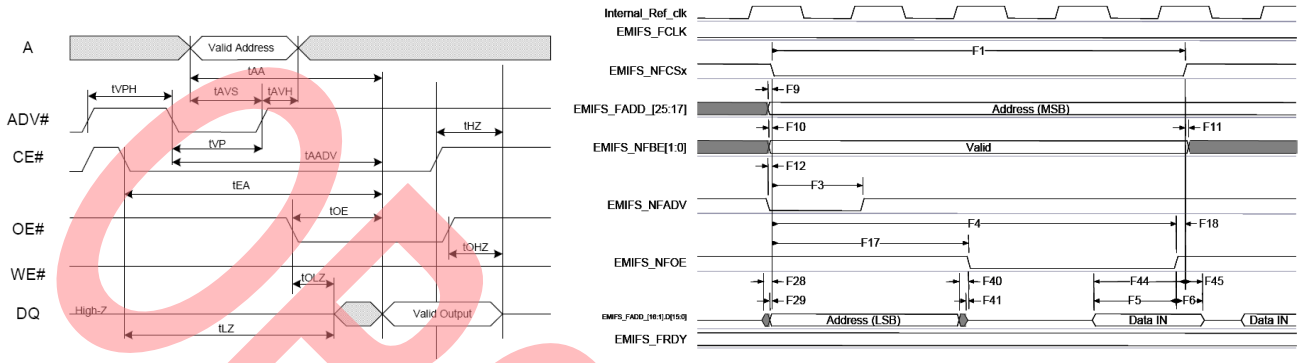


Figure 4. Asynchronous Single Write Timing (Antioch vs. OMAPV1030)

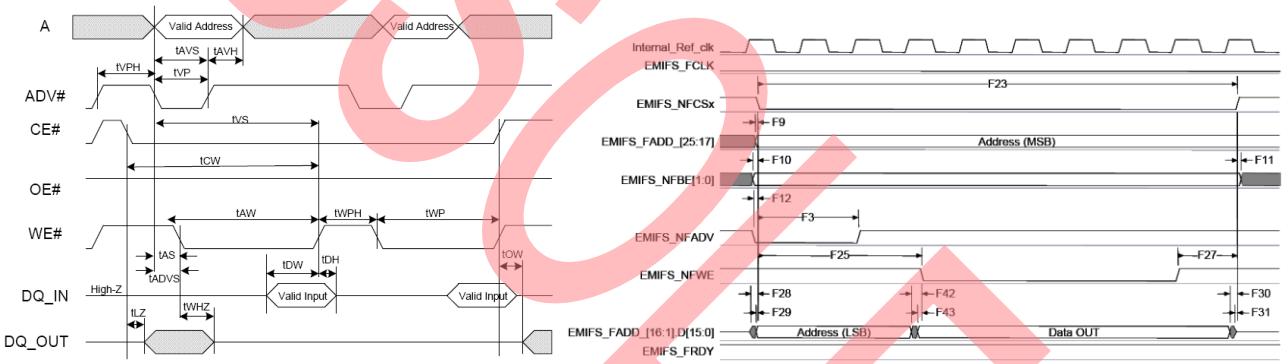


Table 6. Antioch and OMAPV1030 EMIFS Timing Analysis and Calculations

Timing	Antioch Name	Description	OMAPV1030 Parameter	Recommended Configuration
Read Parameters	tEA – tOE +OE# Low pulse + tOHZ	Read CE# low pulse width	tw(CSV) for read	Always met if (tEA-tOE) and tOHZ are met
	tEA -tOE	CE# low to OE# low	td(CSV-OEV)min	OESETUP*REF_CLK -2 > tEA-tOE OESETUP * 15.4 -2 > 30 - 22.5 => OESETUP = 1
	OE# Low pulse - tOE + 2*board_delay	DQ output setup to OE# high	tsu(DV-OEH)	((RDWST+2)*REF_CLK-3) - (OESETUP*REF_CLK+4) – tOE + 2*board_delay > 14 ((RDWST+2)*15.4-3)-(OESETUP*15.4+4)-22.5+2 > 14 => OESETUP = 1; RDWST = 2
	tOHZ + 2*board_delay	OE# high to DQ hold	th(OEH-DV)	Always met
Write Parameters	tWPH + tWP	write CE# low pulse width	tw(CSV)min for write	(WRWST+WELEN+3)*REF_CLK-3 > tWPH + tWP (WRWST+WELEN+3)*15.4-3 > 22+10 => WRWST = 0; WELEN = 0
	tCW - tAW	CE# low to WE# low	tw(CSV-WEV)min	(WRWST+1)*REF_CLK-2 > tCW-tAW (WRWST+1)*15.4-2 > 30 – 30 => WRWST = 0
	tAW	WE# low pulse width	tw(CSV)min - tw(CSV-WEV)max - tw(WEIV-CSIV)max	((WRWST+WELEN+3)*REF_CLK-3) – ((WRWST+1)*REF_CLK+5) – (REF_CLK+2) > 30 =>WRWST = 0; WELEN = 2
	tDW	DQ input setup	-	Always met if tAW is met
	tDH	DQ input hold	tw(WEIV-CSIV)min - td(DIV-CSIV)max	(REF_CLK-5) - (3) > tDH 15.4-5-5>0 Always met
Common for Read and Write	tAVS	Address valid to ADV# High	td(CSV-ADIV)min + td(AV-CSV)min	(ADVHOLD+1)*REF_CLK-2 - 4 > tAVS (ADVHOLD+1)*15.4-2-4 > 5 => ADVHOLD = 0
	tAVH	ADV# high to address hold	-	Always met because EMIFS is in multiplexed address/data mode
	tCVS	CE# low to ADV# high	td(CSV-ADIV)min	(ADVHOLD+1)*REF_CLK-2 > tCVS (ADVHOLD+1)*15.4-2>5 => ADVHOLD = 0
	tVP	ADV# low pulse width	td(CSV-ADIV)min + td(ADV-CSV)min	(ADVHOLD+1)*REF_CLK-2-2 > tVP (ADVHOLD+1)*15.4-4 > 7.5 => ADVHOLD = 0

Note
Assume a board delay of 1 ns.

Additional Resources

- Interfacing TI OMAPV1030 Processor to Astoria's Pseudo-NAND processor port - AN47864
- Schematic Review Checklist for West Bridge® Astoria™ - AN46860

Summary

Antioch can be effectively interconnected with TI OMAPV1030 baseband processor. The timing analysis described in this application note affirms the mode of operations supported with Antioch. The feature set provided by Antioch makes it a perfect fit for the OMAPV1030 processor to enable new high speed USB peripheral connectivity and storage control options to latest mass storage devices. It also completely off-loads the processor from the USB mass storage access, which results a higher performance and more efficient system design.

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**	2550148	HKH/AESA	08/08/2008	New application note.
*A	3323565	ODC	08/09/2011	Software version updated Added Associated Application Notes Added Additional Resources section.
*B	4108854	RSKV	08/30/2013	Obsolete application note

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